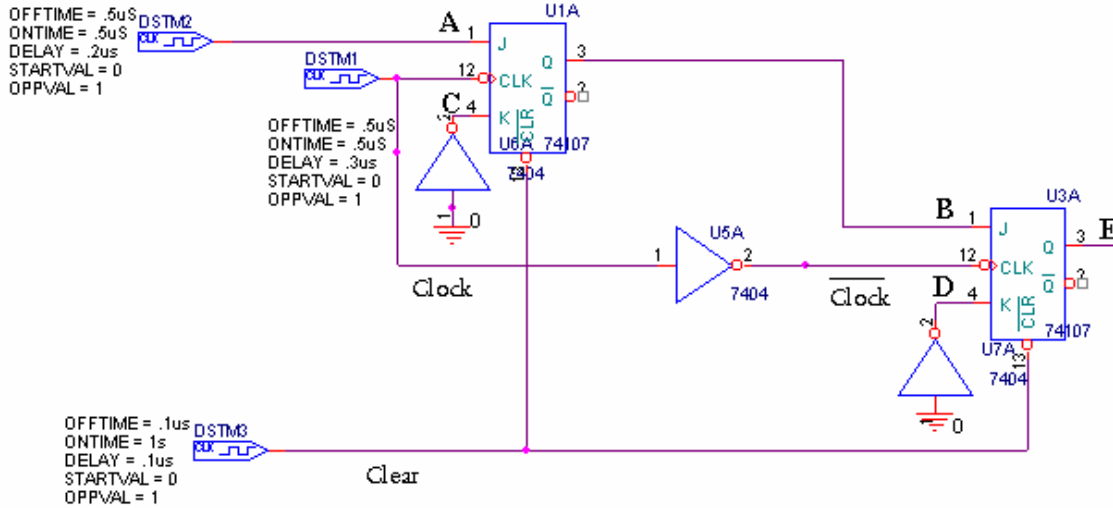
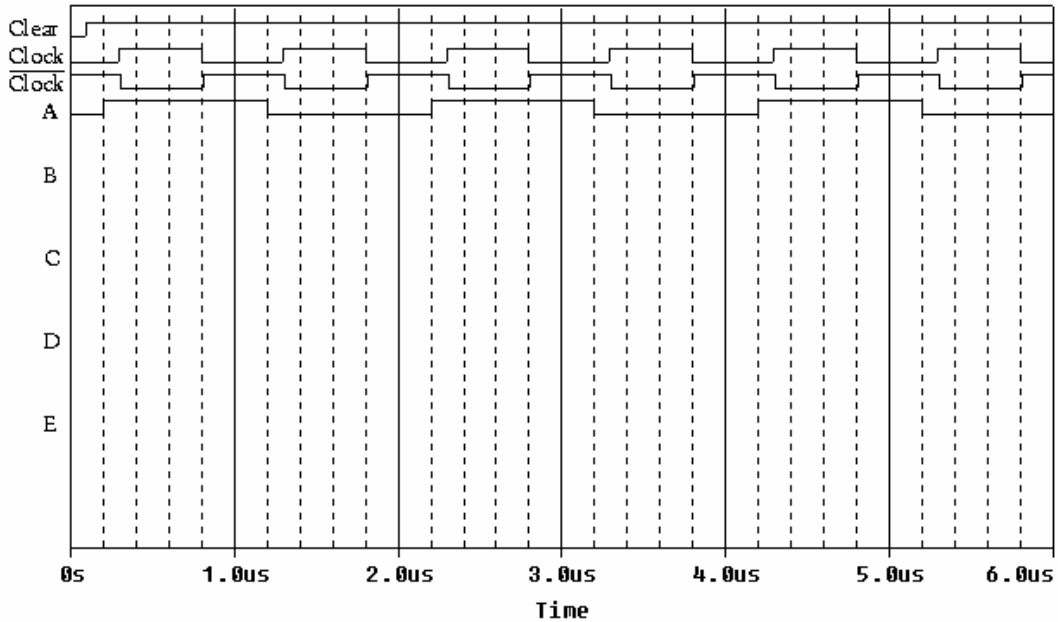


Sample Question: Flip Flops and Counters

The following is a diagram of a circuit from PSpice. The “Clear” signal initializes the flip flop. Therefore, once it goes high, the flip flop outputs $Q=0$ and $\bar{Q}=1$. The clock for the first flip flop is DSTM1 and the clock for the second flip flop is DSTM1 inverted. Remember that flip flops and counters trigger on the falling edge of the clock pulse.



a) The following figure shows the clear signal, the clocks and the input at A. Draw the traces at B, C, D and E.



b) If the clock for a counter (74393) was attached to signal A, what would the output look like after 3.0us. (Assume the counter has also been cleared, therefore $Q_A=0V$, $Q_B=0V$, $Q_C=0V$, $Q_D=0V$ at time 0s). Express your answer in volts.

$Q_A =$

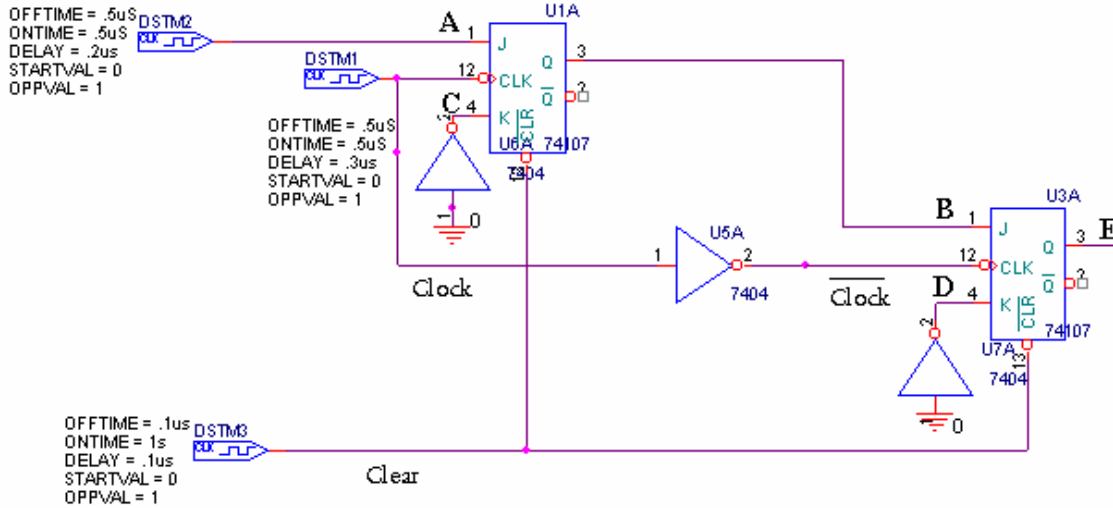
$Q_B =$

$Q_C =$

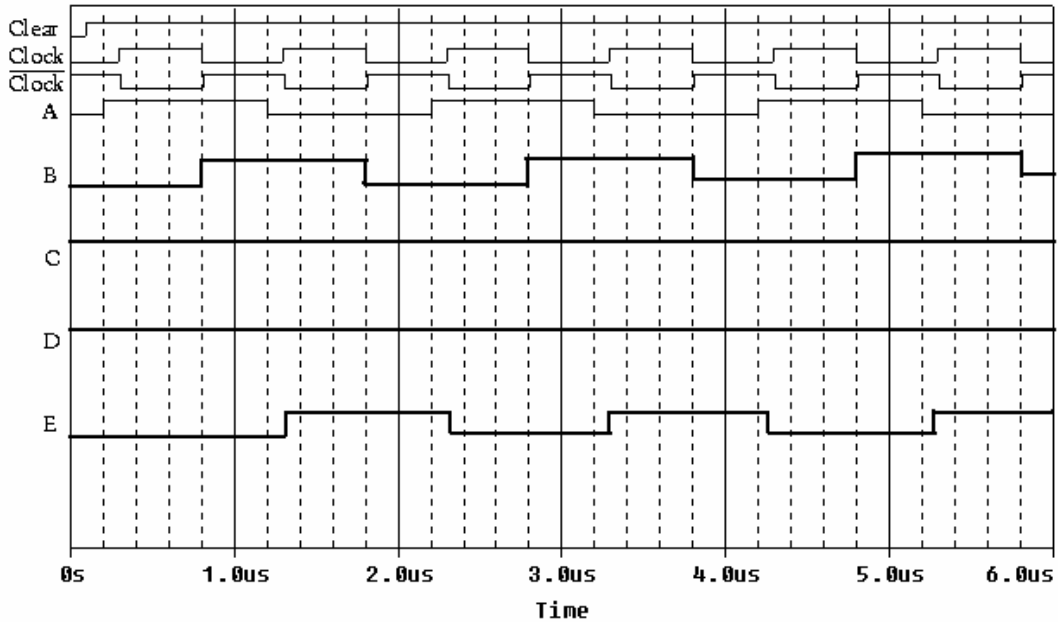
$Q_D =$

Sample Question: Flip Flops and Counters * ANSWER *****

The following is a diagram of a circuit from PSpice. The “Clear” signal initializes the flip flop. Therefore, once it goes high, the flip flop outputs $Q=0$ and $\bar{Q}=1$. The clock for the first flip flop is DSTM1 and the clock for the second flip flop is DSTM1 inverted. Remember that flip flops and counters trigger on the falling edge of the clock pulse.



a) The following figure shows the clear signal, the clocks and the input at A. Draw the traces at B, C, D and E.



[Some explanation: C and D are inverted from ground. This means they are always high. Note that the flip flops only change on the falling edges of the clock. The first flip flop will look at J and K when Clock goes down at 0.8 us. Since at that time A(=J) is high and C(=K) is high, the flip flop toggles and B goes high. The next time that Clock goes high to low at 1.8us, A is low and C is still high. This time, the flip flop should be equal to J(A) and B goes low again. This sequence continues for B. The signal at E changes on the falling edge of Clockbar(the inverted clock signal). Its inputs are J=B and K=5V. At 0.3us, B is low, so E stays low. At 1.3us, B is high, so E toggles to high. At 2.3us, B is low, so E goes low again. The sequence continues.]

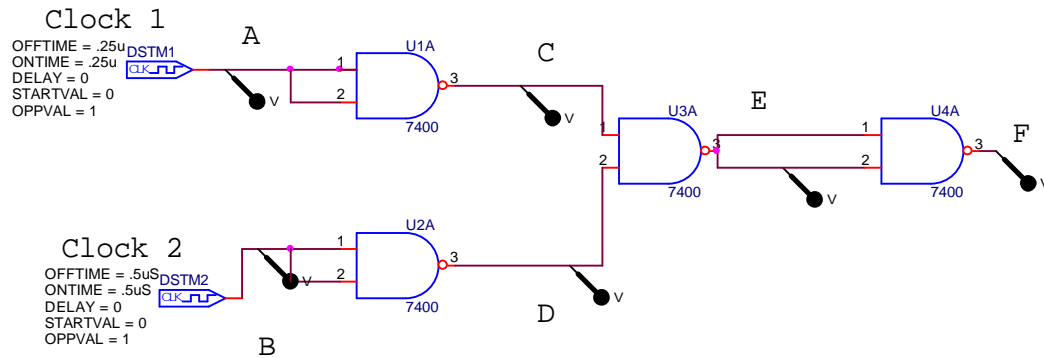
b) If the clock for a counter (74393) was attached to signal B, what would the output look like after 6.0us. (Assume the counter has also been cleared, therefore QA=0V, QB=0V, QC=0V, QD=0V at time 0s). Express your answer in volts.

$$QA = 5V \quad QB = 5V \quad QC = 0V \quad QD = 0V$$

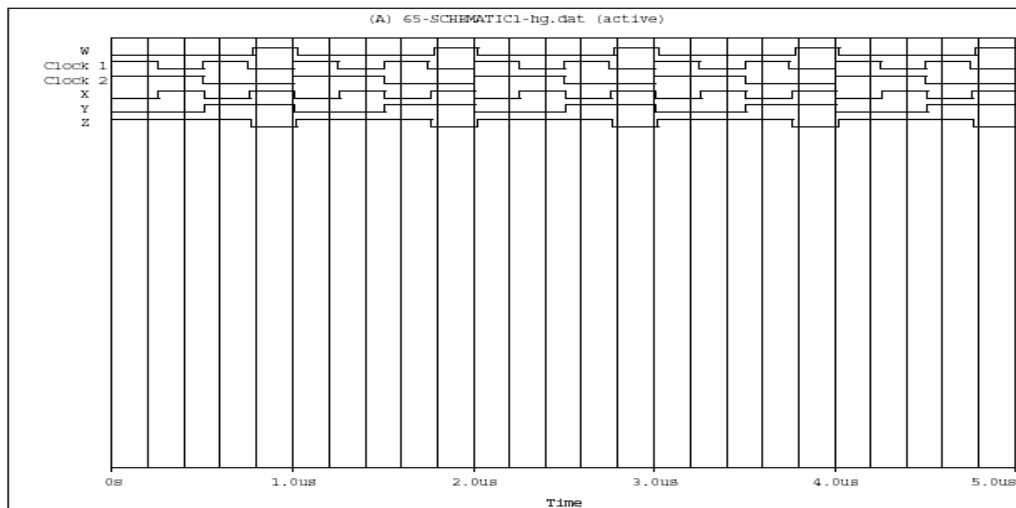
[Some explanation: The counter “counts” on the falling edge of the clock. Since B has three pulses since 0s, the counter should count up to three. In binary, that is 0011. Note that QA is the lowest order bit.]

Sample Question: Boolean Algebra

It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.



a. Identify which trace belongs to which point in the circuit.



b. Write a boolean expression for this circuit (Do not simplify).

a. Properties of Operations	b. Rules of Combination	c. DeMorgan's Laws
(a1) $A \cdot 0 = 0$	(b1) $A \cdot B = B \cdot A$	(c1) $\sim(A \cdot B) = \sim A + \sim B$
(a2) $A + 0 = A$	(b2) $A + B = B + A$	(c2) $\sim(A + B) = \sim A \cdot \sim B$
(a3) $A \cdot 1 = A$	(b3) $A \cdot (B+C) = (A \cdot B) + (A \cdot C)$	
(a4) $A + 1 = 1$	(b4) $A \cdot (B \cdot C) = (A \cdot B) \cdot C$	d. Other Rules
(a5) $A \cdot A = A$	(b5) $A + (B+C) = (A+B) + C$	(d1) $A \cdot B = \sim A \cdot \sim B + A \cdot \sim B$
(a6) $A + A = A$	(b6) $A + (A \cdot B) = A$	(d1) $A \text{ XOR } B = \sim A \text{ and } B + A \text{ and } \sim B$
(a7) $A \cdot \sim A = 0$	(b7) $A \cdot (A+B) = A$	(d2) $\sim(A \cdot B) = \sim A \cdot \sim B + A \cdot \sim B$
(a8) $A + \sim A = 1$	(b8) $A \cdot (\sim A + B) = A \cdot B$	(d2) $\sim(A \text{ XOR } B) = \sim A \text{ and } \sim B + A \text{ and } B$
(a9) $\sim(\sim A) = A$	(b9) $A + (\sim A \cdot B) = A + B$	
	(b10) $\sim A + (A \cdot B) = \sim A + B$	
	(b11) $\sim A + (A \cdot \sim B) = \sim A + \sim B$	

Note that the NOT operation is indicated here by \sim instead of as a bar over the letter.

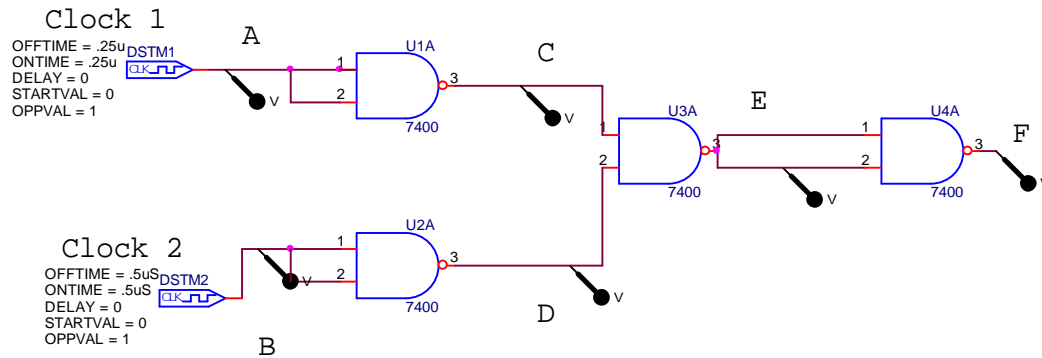
You are free to use either notation. You can indicate the rule by the letter.

[Note to students: Unfortunately, the PDF writer has trouble with the symbol font. In the above chart, the \cdot in sections a, b and c are AND symbols and the meaning of the \cdot in section d can be found in the restatement of the rule.]

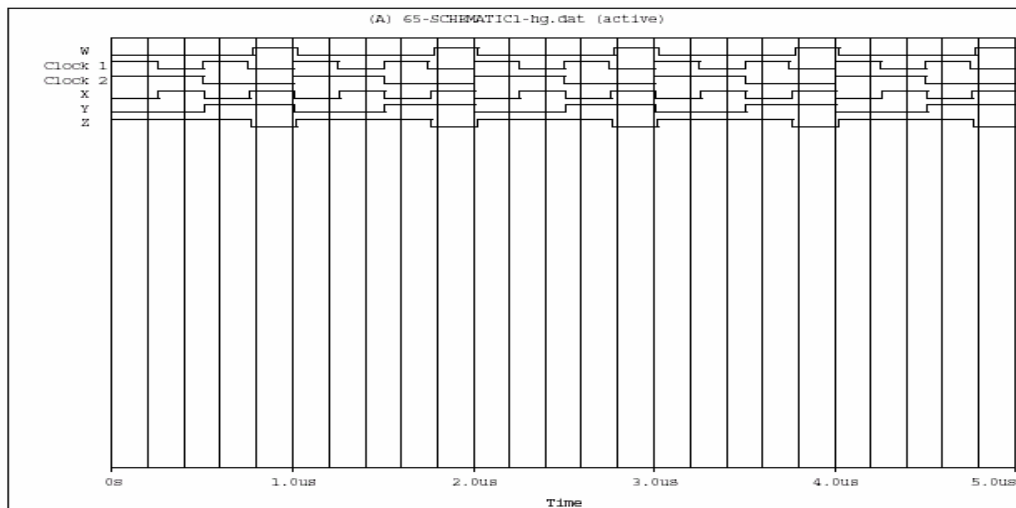
c. Using the Boolean Algebra rules shown above, prove that this combination of gates works as a NOR gate.

Sample Question: Boolean Algebra ** ANSWER **

It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.



a. Identify which trace belongs to which point in the circuit.



$A = \text{Clock1}; B = \text{Clock2}; C = \sim A = X; D = \sim B = Y; E = \sim(X \text{ and } Y) = Z; F = \sim E = W$

b) Write a boolean expression for this circuit (Do not simplify).

$$F = \sim[\sim(\sim A \text{ and } \sim B)]$$

a. Properties of Operations	b. Rules of Combination	c. DeMorgan's Laws
(a1) $A \cdot 0 = 0$	(b1) $A \cdot B = B \cdot A$	(c1) $\sim(A \cdot B) = \sim A + \sim B$
(a2) $A + 0 = A$	(b2) $A + B = B + A$	(c2) $\sim(A + B) = \sim A \cdot \sim B$
(a3) $A \cdot 1 = A$	(b3) $A \cdot (B+C) = (A \cdot B) + (A \cdot C)$	
(a4) $A + 1 = 1$	(b4) $A \cdot (B \cdot C) = (A \cdot B) \cdot C$	d. Other Rules
(a5) $A \cdot A = A$	(b5) $A + (B+C) = (A+B) + C$	(d1) $A \cdot B = \sim A \cdot \sim B + A \cdot \sim B$
(a6) $A + A = A$	(b6) $A + (A \cdot B) = A$	(d1) $A \text{ XOR } B = \sim A \text{ and } B + A \text{ and } \sim B$
(a7) $A \cdot \sim A = 0$	(b7) $A \cdot (A+B) = A$	(d2) $\sim(A \cdot B) = \sim A \cdot \sim B + A \cdot \sim B$
(a8) $A + \sim A = 1$	(b8) $A \cdot (\sim A + B) = A \cdot B$	(d2) $\sim(A \text{ XOR } B) = \sim A \text{ and } \sim B + A \text{ and } B$
(a9) $\sim(\sim A) = A$	(b9) $A + (\sim A \cdot B) = A + B$	
	(b10) $\sim A + (A \cdot B) = \sim A + B$	
	(b11) $\sim A + (A \cdot \sim B) = \sim A + \sim B$	

Note that the NOT operation is indicated here by \sim instead of as a bar over the letter.

You are free to use either notation. You can indicate the rule by the letter.

[Note to students: Unfortunately, the PDF writer has trouble with the symbol font. In the above chart, the \cdot in sections a, b and c are AND symbols and the meaning of the \cdot in section d can be found in the restatement of the rule.]

c. Using the Boolean Algebra rules shown above, prove that this combination of gates works as a NOR gate.

$$F = \sim[\sim(\sim A \text{ and } \sim B)]$$

$$F = \sim A \text{ and } \sim B$$

$$F = \sim(A \text{ or } B)$$

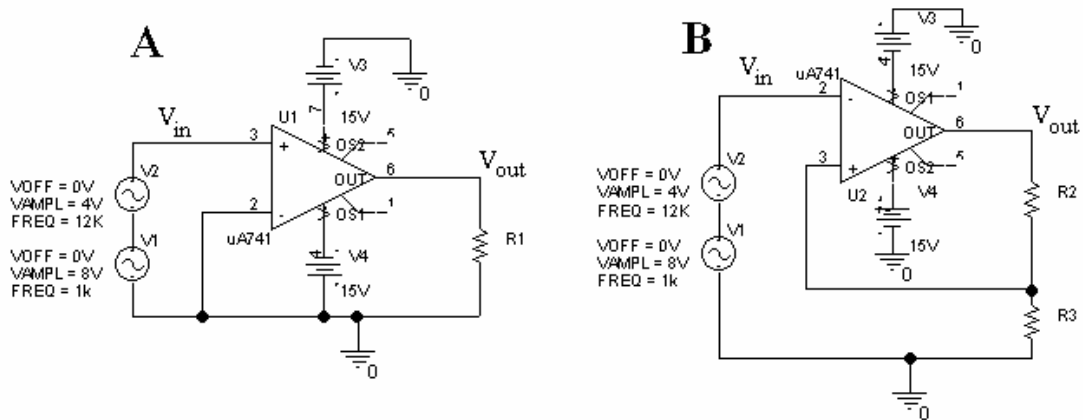
given

rule a9

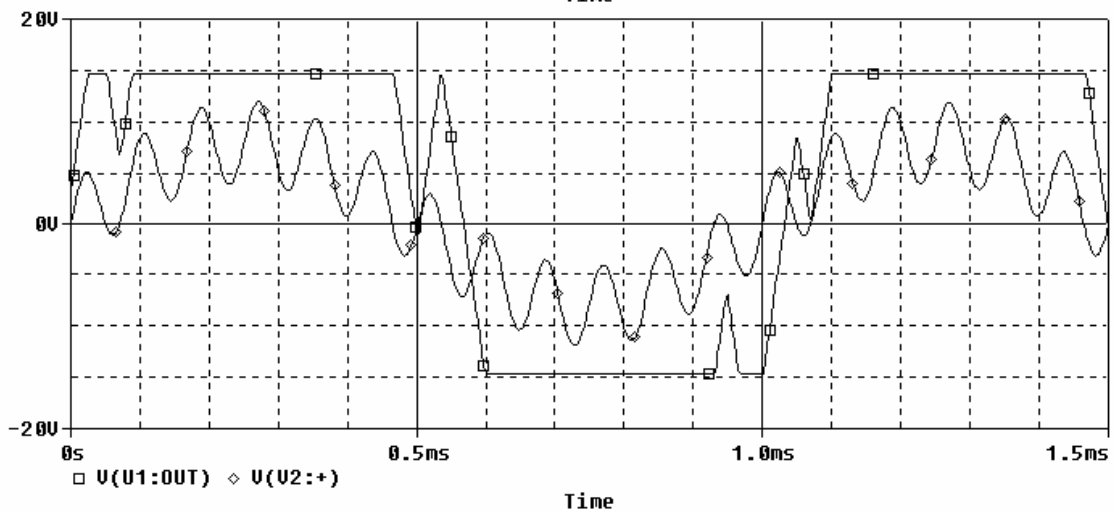
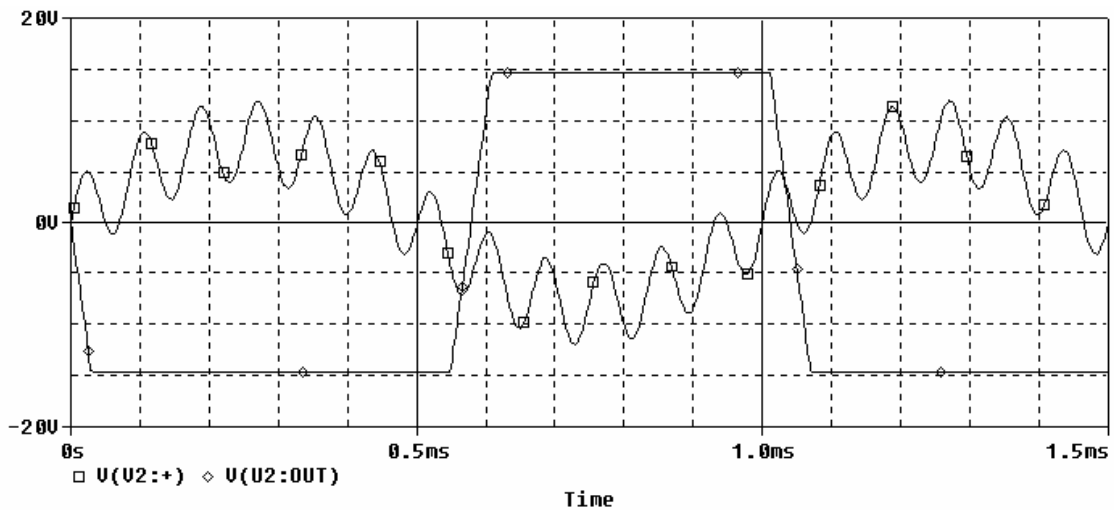
rule c2

This is a NOR gate.

Sample Question: Schmitt Trigger



a) Indicate which plot below goes with which circuit above (2 pts) AND indicate V_{in} and V_{out} on both plots (4 pts).



b) What is circuit A a model or example of ?

- a) an inverting amplifier
- b) a non-inverting amplifier
- c) a Schmitt trigger
- d) a comparator

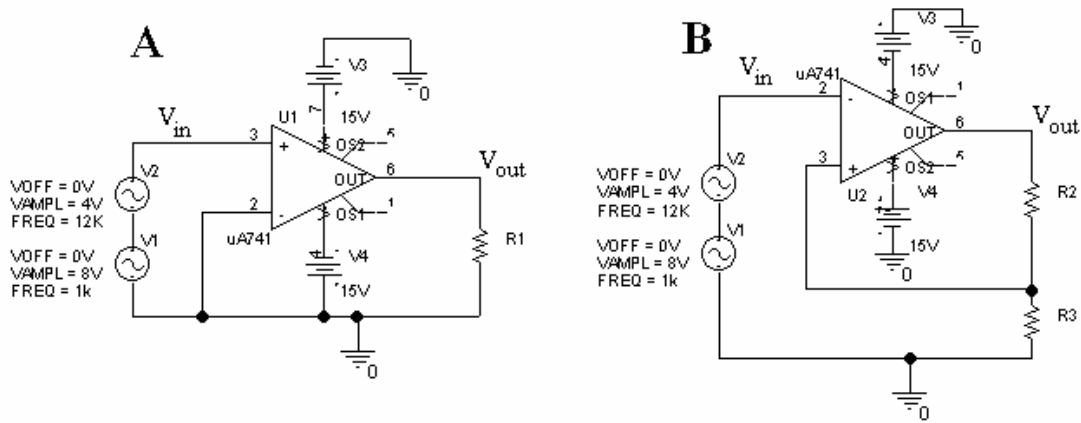
c) What is circuit B a model or example of ?

- a) an inverting amplifier
- b) a non-inverting amplifier
- c) a Schmitt trigger
- d) a comparator

e) What is the saturation range of the op-amp (in both circuits)?

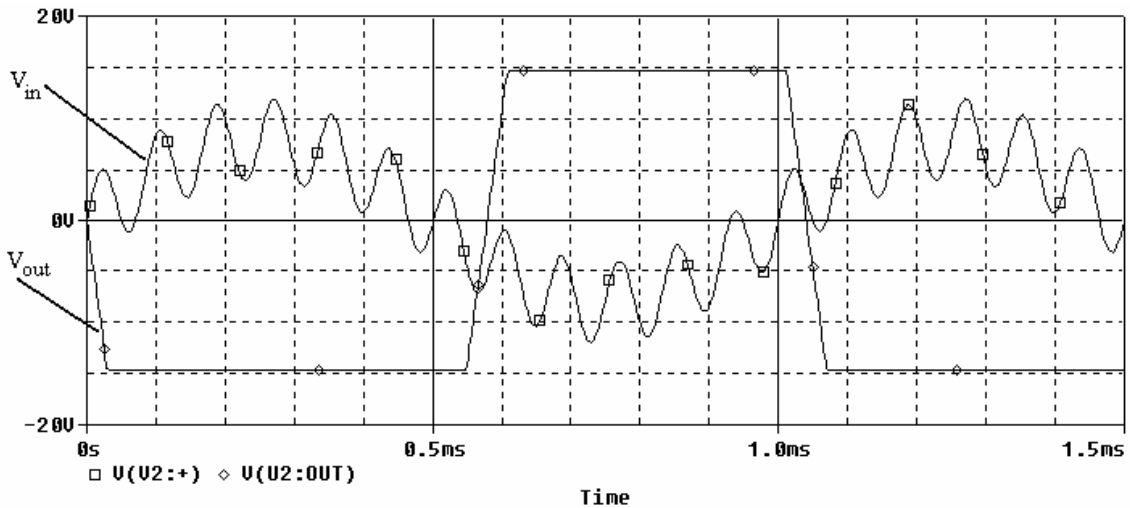
f) If R_2 is 10K ohms, then what does R_3 have to be in circuit B to give a hysteresis of 4 volts?

3) Schmitt Trigger (20 Points) **** ANSWER ****

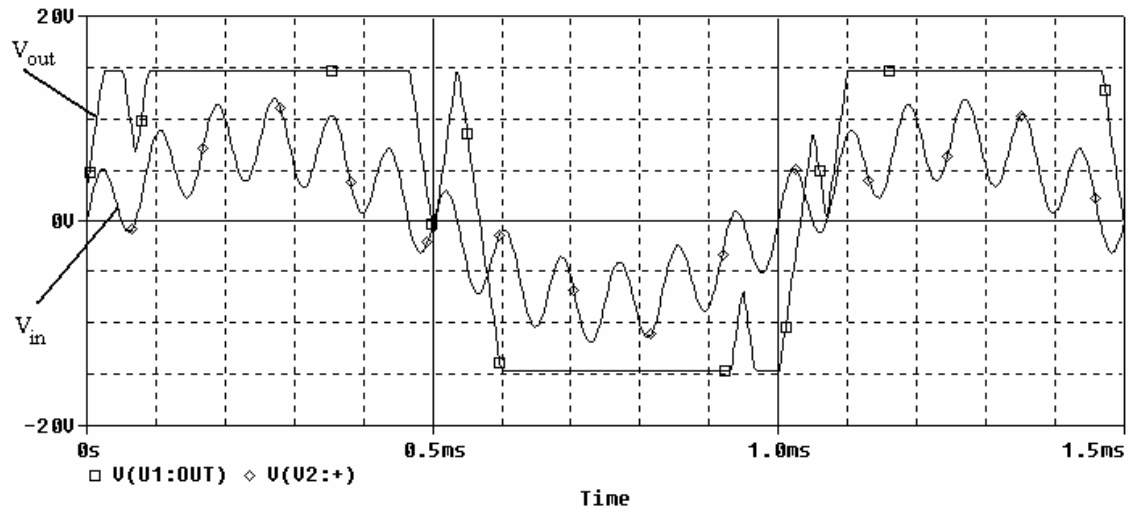


a) Indicate which plot below goes with which circuit above AND indicate V_{in} and V_{out} on both plots .

The one below is B



The one below is A



b) What is circuit A a model or example of ?

a) an inverting amplifier

b) a non-inverting amplifier

c) a Schmitt trigger

d) a comparator

c) What is circuit B a model or example of ?

a) an inverting amplifier

b) a non-inverting amplifier

c) a Schmitt trigger

d) a comparator

e) What is the saturation range of the op-amp (in both circuits)?

[From the plot, you can see that the op-amp saturates at between 14 and 15 volts when the positive is greater than the negative and between -14 and -15 volts when the negative is greater than the positive. Anything between (+15 to -15) and (+14 to -14) is acceptable. The value below is the actual value from PSpice for the above plots.]

Answer: +14.6 to -14.6 V

f) If R2 is 10K ohms, then what does R3 have to be in circuit B to give a hysteresis of 4 volts?

*[Recalling your notes and section 6.5 in Lunn, the hysteresis is determined by the relationship between the saturation voltage and the two resistors in the voltage divider in circuit B. If we let Vref be the voltage point between R2 and R3, then $V_{ref} = V_{out} * R3 / (R2 + R3)$. Since Vout toggles between +14.6V and -14.6V, we have two values for Vref:*

$$+V_{ref} = +14.6 * R3 / (R2 + R3) = +14.6 * R3 / (R3 + 10K)$$

$$-V_{ref} = -14.6 * R3 / (R2 + R3) = -14.6 * R3 / (R3 + 10K)$$

If we want a range of 4 volts between +Vref and -Vref, then +Vref must be 2V and -Vref must be -2V. (The hysteresis is centered around 0 volts.) Therefore we have,]

Answer:

$$2V = 14.6V * R3 / (R3 + 10K)$$

$$2R3 + 20K = 14.6R3$$

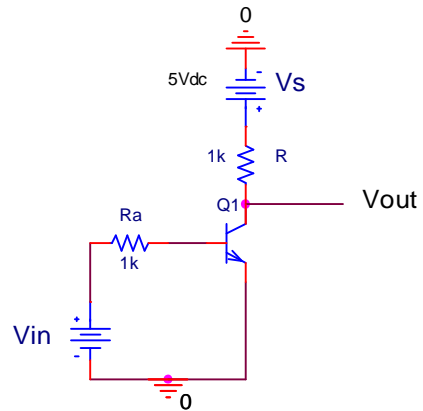
$$12.6R3 = 20K$$

$$R3 = 1587 \text{ ohms}$$

[Please note that in the first plot (circuit B) above, the hysteresis is not the same. If you look at the point at which Vout BEGINS to rise and fall, you can see that the hysteresis is between about +3 and -3 for a hysteresis of 6V. In the second plot (circuit A), the change in direction happens at zero because there is no hysteresis for a comparator.]

Sample Question: Transistors

Here is a simple transistor circuit.



a) Redraw the circuit when V_{in} is 0V. [Draw the transistor as a switch either open or closed.]

b) Redraw the circuit when V_{in} is 5V. [Draw the transistor as a switch either open or closed.]

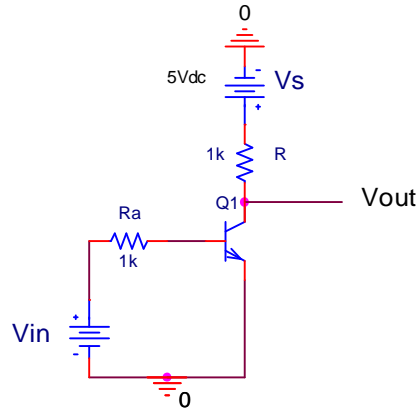
c) If V_{in} is the input, A, and V_{out} is the output, Y, then fill in the following truth table.

A	Y
0	
1	

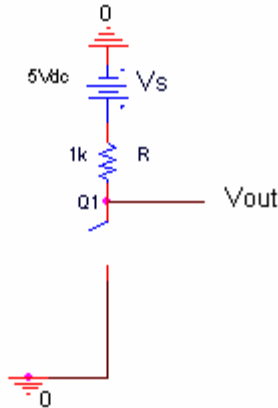
d) What kind of gate is this?

Sample Question: Transistors ** ANSWERS **

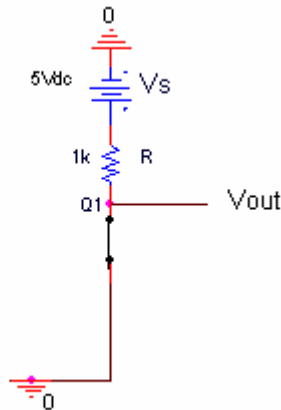
Here is a simple transistor circuit.



a) Redraw the circuit when V_{in} is 0V. [Draw the transistor as a switch either open or closed.]



b) Redraw the circuit when V_{in} is 5V. [Draw the transistor as a switch either open or closed.]



c) If V_{in} is the input, A, and V_{out} is the output, Y, then fill in the following truth table.

A	Y
0 (0V)	1 (5V)
1 (5V)	0 (0V)

d) What kind of gate is this?

NOT gate