Experiment 6
Electronic Switching

Purpose: In this experiment we will discuss ways in which analog devices can be used to create binary signals. Binary signals can take on only two states: high and low. The activities in this experiment show how we can use analog devices (such as op-amps and transistors) to create signals that take on only two states. This is the basis for the digital electronics components we will examine in experiment 7.

Equipment Required:

- HP 34401A Digital Multimeter
- HP 33120A 15 MHz Function / Arbitrary Waveform Generator
- HP E3631A Power Supply
- HP 54603B 2 Channel 60 MHz Oscilloscope

Helpful links for this experiment can be found on the links page for this course:
http://hibp.ecse.rpi.edu/~connor/education/EILinks.html#Exp6

Part A – Transistor Switches

Background

Transistors: A transistor, pictured in figure A-1, is an electrically controlled semiconductor switch. The switch connects the Collector to the Emitter. The signal at the Base closes and opens the switch.

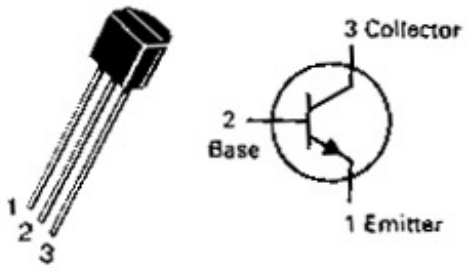

Figure A-1

In an ideal transistor model, the signal at the Base is not part of the circuit, it simply opens or closes the connection between the Collector and the Emitter. In an npn transistor like the one pictured, when the switch is open, no current flows from the Collector to the Emitter and, when the switch is closed, a current flows from the Collector to the Emitter. Hence, the transistor needs to be oriented in the circuit so that the Collector points towards the source and the Emitter points towards ground. Note that the arrow on the Emitter leg shows the direction of current flow. To get the switch to open, we place a low voltage at the base (less than about 0.7 volts). To get the switch to close, we place a high voltage at the Base (greater than about 0.7V). There are different kinds of transistors that have slightly different characteristics. In this course, we use the npn.

Transistors have three operating regions. When the base is low, the current is not allowed to flow from collector to emitter. This region is called the *cutoff region*. When the base is high, the current flows freely from collector to emitter. This is called the *saturation region*. There is also a third region that occurs when the input voltage to the base is around 0.7 volts. In this region, the transistor is changing state between allowing no current to flow and allowing all current to flow. At this time, the current between collector and emitter is proportional to the current at the base. The region is called the *active region.* Over this small range of voltages, the transistor can be used as a current amplifier.

Experiment

The Transistor

In this part of the experiment, we will use PSpice to look at the behavior of a transistor when it is being used as a switch.

- Using PSpice, set up the circuit shown in figure A-2. Note that there are two voltage sources. V1 controls the base voltage and V2 provides voltage at the collector so that current can flow when the switch is closed.

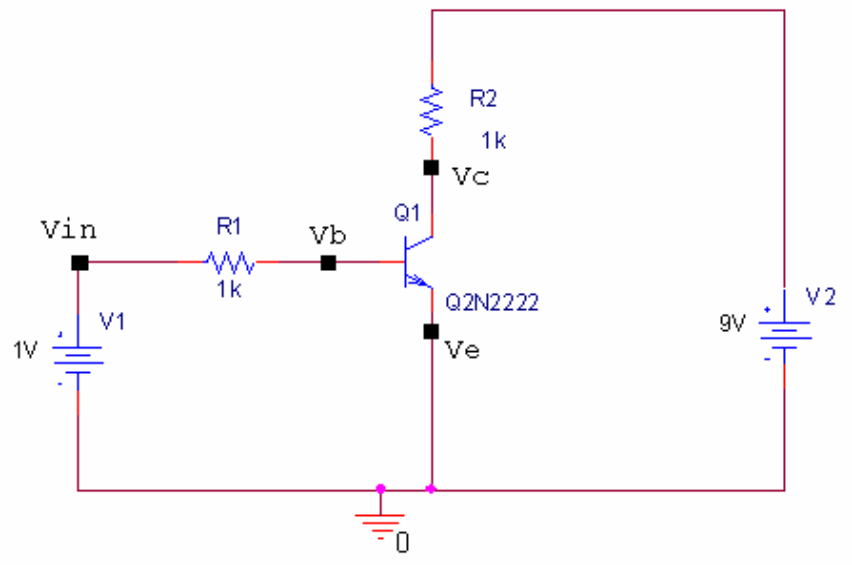

Figure A-2

- Run a DC sweep simulation.
  - Set up a DC SWEEP for V1 from 0.2 to 9 volts (step = 0.005V).
  - Place voltage markers at Vin, Vb, Vc and Ve.
  - The transistor Q1 is acting as a switch in the loop with resistor R2 and voltage V2. The voltage V1 and resistor R1 are used to turn the switch ON or OFF.
  - The transistor switch will not work exactly like an ideal, simple switch. However, it can be a good approximation to such a switch and, more importantly, it will switch states based on an applied voltage rather than a mechanical act (like turning a switch on and off). Identify on the plot where the transistor is in the cutoff region (OFF) and in the saturation region (ON).
  - Include this plot in your report.

- Now we will consider this switch in a configuration that switches the voltage across a load.
  - Add the resistor R3 as shown in figure A-3 to your circuit.
  - The transistor switch, when open, allows the maximum voltage to occur across R3. When the switch is closed, the voltage across R3 goes near zero.
  - Run your simulation again and print your output. Include this plot in your report.
  - What is a typical voltage across R3 when the switch is OFF? What is a typical voltage across R3 when the switch is ON? From what you know about voltage dividers, do you think that these values make sense?

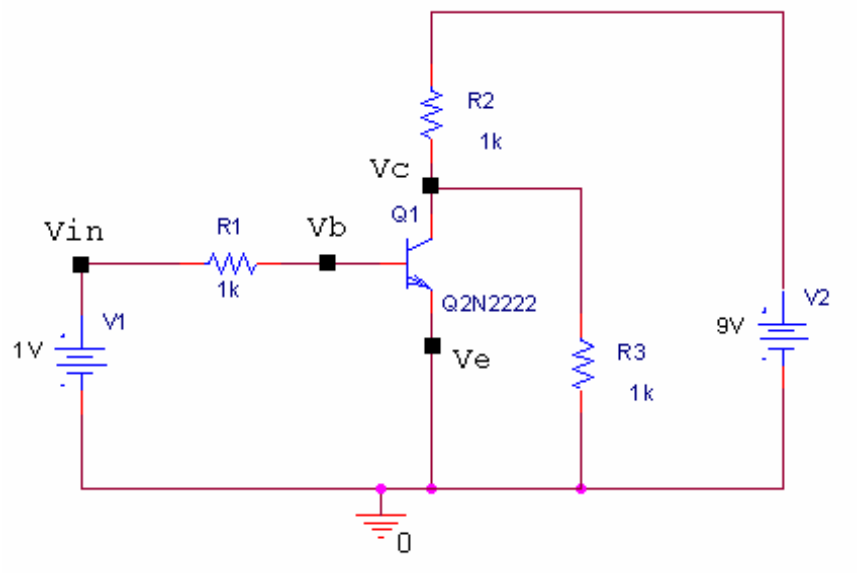

Figure A-3

- Now we want to take a closer look at the range of V1 for which the transistor is in the active region and the switch is neither ON nor OFF.
  - Remove the voltage markers from your circuit.
  - Place current markers on the collector, emitter, and base leads of the transistor.
  - Rerun your PROBE result but change the sweep for V1 to range from 0.2V to 0.9V.
  - Use traces to normalize all three currents by dividing them by the current at the base (IB(Q1)). Also, negate the normalized emitter current so that all three traces are positive.
  - You should be able to identify a small range of voltages for which the normalized magnitude of the collector and emitter currents are approximately constant at around 170 times the base current. Use the cursors to find this range. Indicate the range on your plot.
  - Print out the plot and include it with your report.
  - This is the active region for which the transistor circuit acts like a very good amplifier. Here it has a current gain of much more than 100. The gain is not a simple constant, nor is it as large as we can obtain with an op-amp.

Summary

By looking at the operation of a simple transistor circuit, we have seen that there is a set of input voltages for which it looks like a switch that is OFF, an amplifier, and a switch that is ON.

Part B – Comparators and Schmitt Triggers

Background

Comparators: An op-amp can be used to create a binary signal with only two states. An op-amp has an extremely high intrinsic gain (of about 10^6). With no negative feedback to stabilize its behavior, the output of an op-amp is this huge intrinsic gain multiplied by the difference between the two inputs. If the non-inverting input is slightly higher than the inverting input, the op-amp will saturate in the positive direction. If the inverting input is slightly higher than the non-inverting input, it will saturate negative. The op-amp with no feedback has two states, and therefore, it is a binary device. The value of the output is limited by V_{CC}. Thus, the output should go to about $+V_{CC}$ whenever the net input is positive and to $-V_{CC}$ whenever the net input is negative. The net input is determined by comparing the voltage at the positive (+) terminal to the voltage at the negative (-) terminal. When $V^+ > V^-$ then $V_{out} = V_{CC}$ and when $V^+ < V^-$ then $V_{out} = -V_{CC}$.

We call this op-amp configuration a comparator because its state is determined using a comparison of the two inputs. In this experiment, comparators are used to compare an input to some reference voltage, V_{ref}. If the net difference between the input and V_{ref} switches sign, then the comparator will switch state. A comparator can be inverting (when V_{ref} is connected to the non-inverting input) or non-inverting (when V_{ref} is connected to the inverting input).

Schmitt Triggers: Comparators do not give a reliable signal in the presence of noise because the output voltage swings between positive and negative whenever the net input crosses the reference voltage, V_{ref}. It would be more useful to have a comparator-type circuit that switches output state when the net input exceeds some finite threshold buffer around V_{ref} rather than the reference voltage itself. The Schmitt trigger makes this possible. In a Schmitt trigger, T_{upper} and T_{lower} are the upper and lower thresholds that define the buffer area around V_{ref}, and B_{upper} and B_{lower} are constants that define the size of the buffer area. The output of the trigger will switch when the input exceeds $T_{upper} = V_{ref} + B_{upper}$ or is less than $T_{lower} = V_{ref} - B_{lower}$. The size of the buffer area is called the *hysteresis* and it is given by $T_{upper} - T_{lower}$. We can model a Schmitt trigger using an op-amp circuit. In this model, the two thresholds, T_{upper} and T_{lower}, are determined using a voltage divider in the *positive* feedback path of the Schmitt trigger model. Because Schmitt triggers use feedback from the output to create the hysteresis, they are always inverting.

Experiment

The Comparator
First we will examine the behavior of a simple comparator that changes state when the input goes above or below a constant voltage.

- Build the circuit in figure B-1 PSpice.

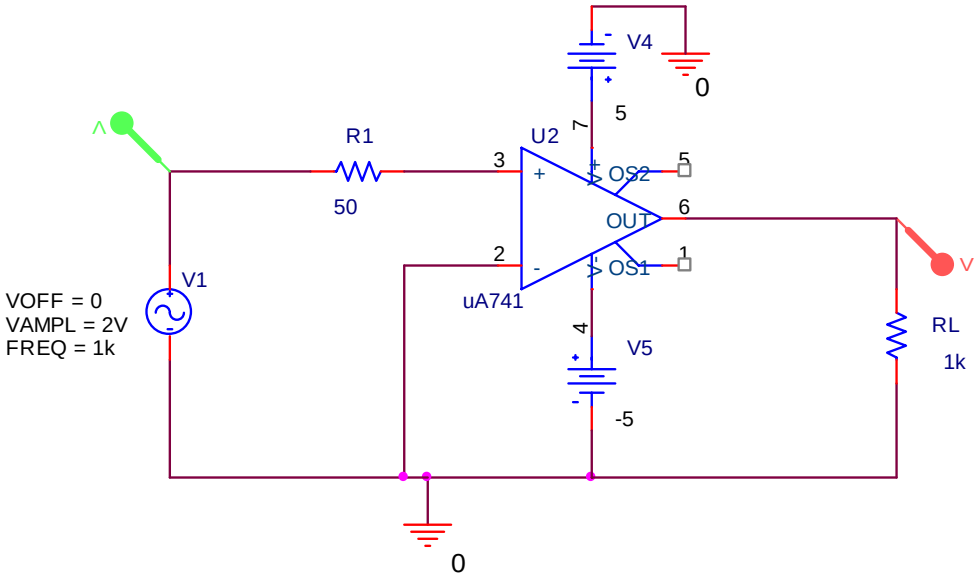

Figure B-1

- Run a transient simulation
  - Run the simulation from 0 to 3ms with a time step of 1us.
  - Print a plot of your output, showing the source voltage V1 and the load voltage (pin 6 of the op-amp). Include this plot in your report.

- Note that the point at which the input and output signals cross is not the point in time when the comparator starts to switch states. You can see by closely examining the plot, that the op-amp *starts to change state when the input signal crosses zero.*
- The saturation voltage is the voltage level that the *output* reaches when the op amp is saturated. What are the positive and negative saturation voltages of the op-amp?

- Add a 1V reference voltage to the comparator as shown in figure B-2 below

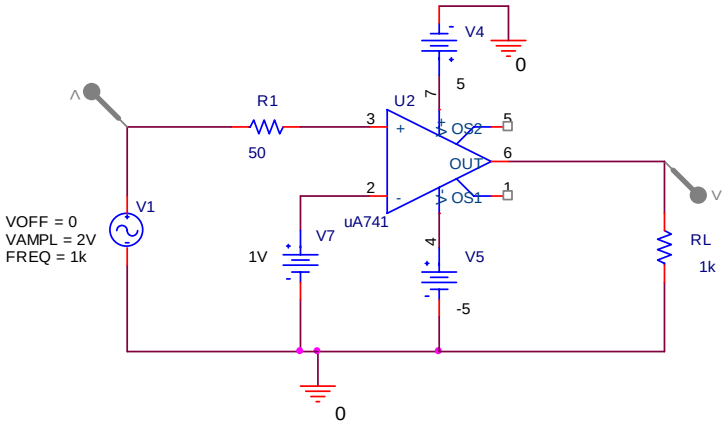

Figure B-2

- Run a transient simulation
  - Rerun the simulation from 0 to 3ms with a time step of 1us.
  - Print a plot of your output, showing the source voltage V1 and the load voltage (pin 6 of the op-amp). Include this plot in your report.
  - Note the value that the *input signal* is crossing when the comparator starts to change state. Is it at a different input voltage than circuit B1? How does it compare to the reference voltage of 1V?
  - Now look at the saturation voltages of the output. Are they the same as in circuit B1? Saturation voltages are a characteristic of the op amp itself, so these should not change.

Schmitt Trigger

Now we will examine a model of a Schmitt trigger.

- Build the circuit in figure B-3 in PSpice.

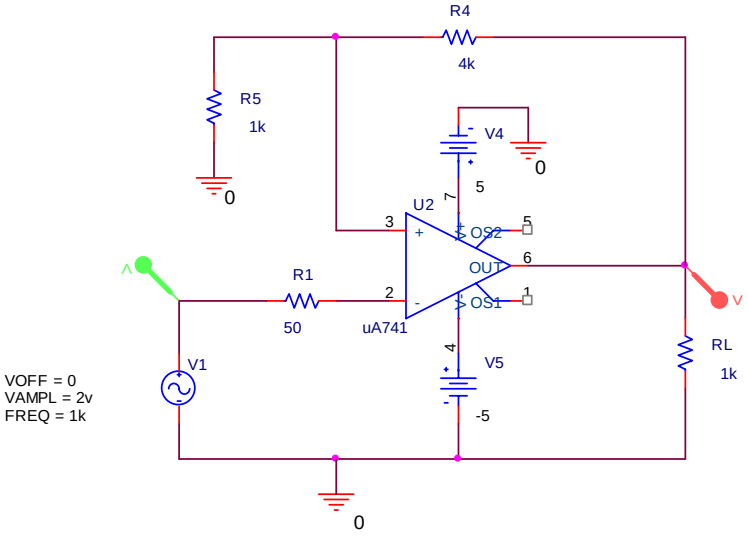

Figure B-3

- Now simulate this circuit.
  - Use the same transient analysis as above.
  - Print one plot, again showing the source voltage V1 and the output voltage (pin 6). Include this plot in your report.
  - The reference voltage for this circuit is zero. Does the output change when the input crosses the reference voltage? What is the value of the input voltage when the output starts to change state from high to low?...from low to high? These are the values of the threshold voltages for the circuit, T_{upper} and T_{lower}. What is the hysteresis?
  - You can calculate the thresholds, T_{upper} and T_{lower}, from the circuit diagram by using the voltage divider formed by R4 and R5. If the output is saturated positive, at +5V, what will be the voltage at the non-inverting input of the op-amp? The op-amp is comparing the input voltage, V1, to this value. This must be the positive threshold, T_{upper}. What happens when the output is saturated negative, at -5V? This is the negative threshold, T_{lower}.

- A Schmitt Trigger can be further generalized by adding a reference voltage to the voltage divider at the non-inverting input. Modify the Schmitt trigger model by adding a 1V source as shown below:

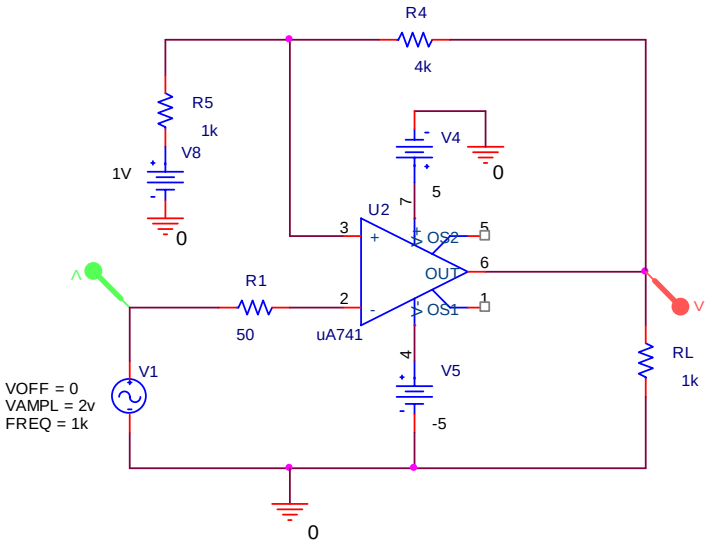

Figure B-4

- Simulate this circuit
  - Use the same transient analysis as above.
  - Print one plot, again showing the source voltage V1 and the output voltage (pin 6). Include this plot in your report.
  - What is the reference voltage for this circuit? Does the output switch states when the input crosses the reference voltage? What are the values of the upper and lower thresholds of this circuit? Are they the same as circuit B-3? Why not? What is the hysteresis?
  - You can use a voltage divider to calculate the upper and lower thresholds of this circuit as well. Use the method described in the class notes to do so.

Summary

An op-amp can be used to create binary devices. The comparator, a single op-amp with no feedback, is the simplest of these. The comparator can be used to compare a signal to zero or to any reference voltage. The comparator does not work well in the presence of noise. A more complicated op-amp circuit, that solves this problem, can be created by adding a voltage divider to the non-inverting input of the op-amp. This creates a threshold above and below the reference voltage around which the op-amp will not switch state. Such an op-amp configuration is called a Schmitt trigger.

Part C –Digital Switching

Digital chips: Digital chips are electronic devices that perform logic operations on binary signals. This type of chip forms the basis for all digital computers. There are digital chips that are designed using the same principals as both the Schmitt trigger and the comparator. A *Schmitt trigger inverter* is a digital version of the Schmitt trigger and an *inverter* is a digital version of the comparator. These chips are slightly more restrictive then the op-amp models because they are based on digital conventions. Therefore, by convention, the high power voltage, +Vcc, is 5V and the low power voltage, –Vcc, is 0V. The switching voltage lies at a point between low and high. We will examine where this point is in this part of the experiment. Just like op-amps, all digital chips must be supplied with two power voltages, +5V and 0V. By convention, these connections are always made at the lower left hand corner (0V) and the upper right hand corner (5V) of the chip. In fact, these conventions are so common in digital chips, that PSpice does not require that you make them. It just assumes they are made. On your protoboard, however, you must make the connections.

The SN7414: The SN7414 chip pictured in figure C-1 contains six Schmitt trigger inverters. The inputs are donated by nA and the corresponding output by nY, where n is an integer from 1 to 6. By convention, pin 7 is attached to ground and pin 14 is attached to Vcc, 5V.

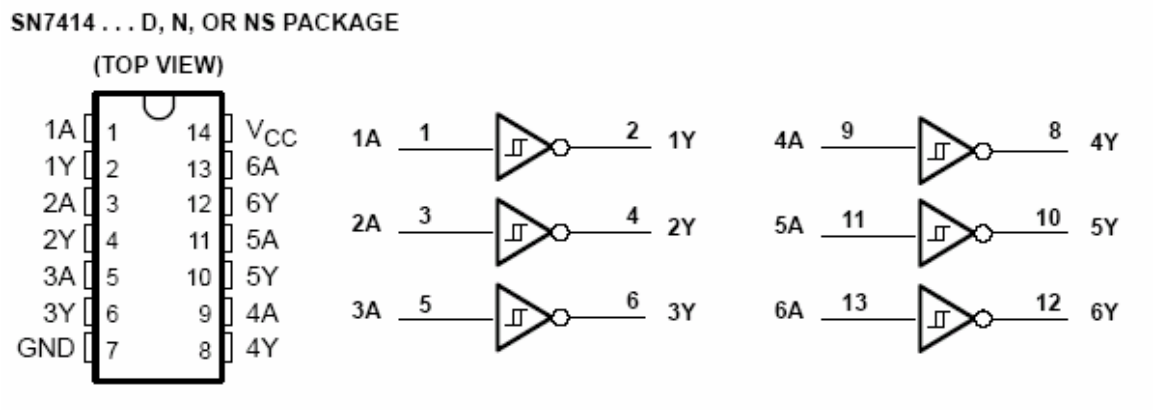

Figure C-1

The purpose of the Schmitt trigger inverter is to convert an analog voltage into a binary digital voltage. When the input voltage of the SN7414 exceeds a threshold, V_{T+}, the device output switches to LOGIC 0 (0V); the input voltage must drop below a second threshold, V_{T-}, for the output to switch back to LOGIC 1 (5V). The difference in thresholds (called hysteresis) is very important in preventing false triggering on noise. The device is also inverting, but the Schmitt trigger inverter does not behave in the same manner as the inverter. You can find more information about this chip on the spec sheet for the 7414 located on the links page for the course.

The SN7404: This chip contains six inverters. The purpose of the chip is to invert a binary signal. The pinout is exactly the same as the Schmitt trigger inverter, but this chip is not designed to handle analog signals. It assumes the input takes on one of two distinct values: LOW (somewhere near 0V) and HIGH (somewhere near 5V). There is a grey area between a cutoff for LOW, V_{IL}, and a second cutoff for HIGH, V_{IH}. The inverter is not designed to function correctly in this area. You can find more information about this chip on the spec sheet for the 7404 located on the links page for the course.

The VPULSE source: In this experiment, you will need to understand a new type of source in PSpice. It is used to create trapezoidal pulses, as pictured in figure C-2. It can also model specialized versions of the trapezoid, such as square waves and triangular waves. The VPULSE source has several parameters. V1 is the lowest point on the pulse (the voltage at the base of the trapezoid). V2 is the highest point on the pulse (the voltage at the top of the trapezoid). TD is an initial time you can set to delay the start of the wave. (This is usually 0). TR and TF stand for "rise time" and "fall time". These indicate how much time should be spent transitioning from V1 to V2 and from V2 to V1, respectively. These determine the slope of the

sides of the trapezoid. The PW parameter, pulse width, is the time spent at the constant high voltage, V2. This defines the width of the top of the trapezoid. The final parameter, PER, is the period of the whole signal. The amount of time between trapezoidal pulses is PER - (TR+PW+TF).

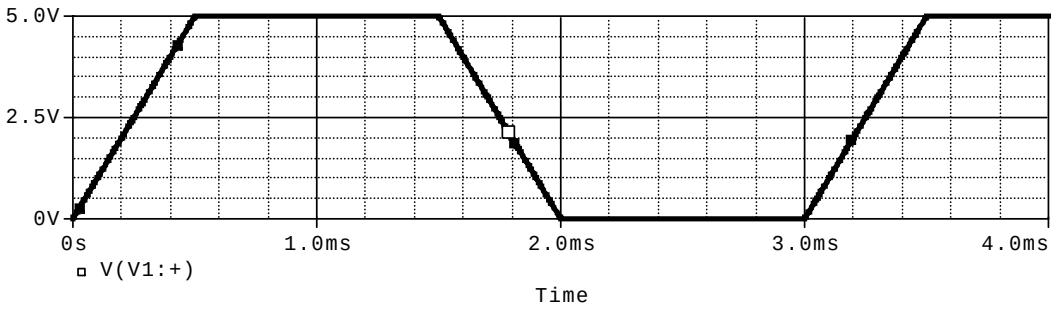

Figure C-2

For example, in the pulse above, the period is 3ms, the rise and fall times are 0.5 ms and the pulse width is 1ms. The VPULSE source is located in the SOURCE library in PSpice.

Experiment

Comparing the Schmitt Trigger and the Comparator in the presence of noise.
Now we will use PSpice to simulate a circuit that uses the SN7404 and the SN7414 to compare the behavior of the inverter to the Schmitt trigger inverter in the presence of noise. We will use two voltage sources to simulate a noisy signal.

- Create the circuit in figure C-3 in PSpice.

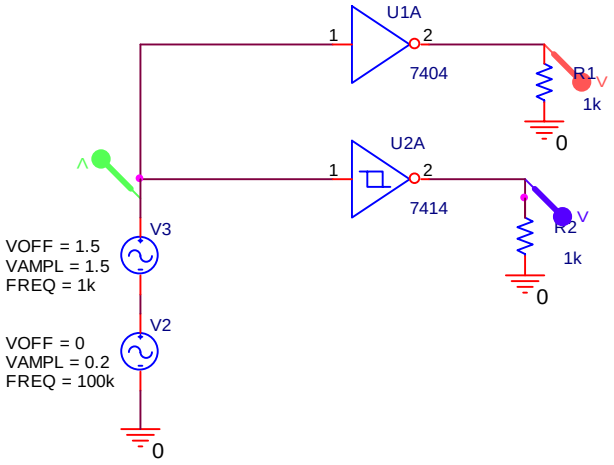

Figure C-3

- Simulate this circuit.
  - For V3, use an offset of 1.5V, an amplitude of 1.5V and a frequency of 1k.
  - For V2, use no offset, an amplitude of 0.2V and a frequency of 100k.
  - Run the simulation for 1.5ms using a step size of 1us.
  - Plot both outputs along with the input signal. Include this plot in your report.
  - Determine what the input voltage is when the output of the inverter changes state. This is V_{ref} for the digital comparator. You will need to choose a new time scale around each of the transition points or use the magnifier to find the exact voltage. What is the simulated noise doing to the output of the inverter? Is there any hysteresis around V_{ref} at all?

- Check to be sure that the inverter performs as it should by looking up the characteristics of the SN7404 on the links page. (See page 5: V_{IH} and V_{IL}) For what range of voltages should the device not invert correctly?
- Determine the value of the input voltage when the output of the Schmitt trigger changes state. (Find T_{upper} and T_{lower}.) You will need to choose a new time scale around each of the transition points or use the magnifier to find the exact voltages. What is the hysteresis of the Schmitt trigger?
- Check to be sure that the Schmitt trigger device performs as it should by looking up the characteristics of the SN7414 on course links page. (See page 4: V_{T+}, V_{T-}, and hysteresis). What are the typical switching thresholds and hysteresis for this device? Does the PSpice simulation work as expected?

Using the Schmitt trigger and the inverter to control a transistor switch.
In the following simulation, we will use the comparator and the Schmitt trigger to open and close a transistor switch.

- Wire the circuit in figure C-4 in PSpice. Note that there are two identical circuits in this diagram: one containing an inverter and the other a Schmitt trigger inverter.
  - The VPULSE pulse should range between 0 and 5V. The rise and fall times should be 0.5ms. The pulse width should be 1ms. The total period should be 3ms.

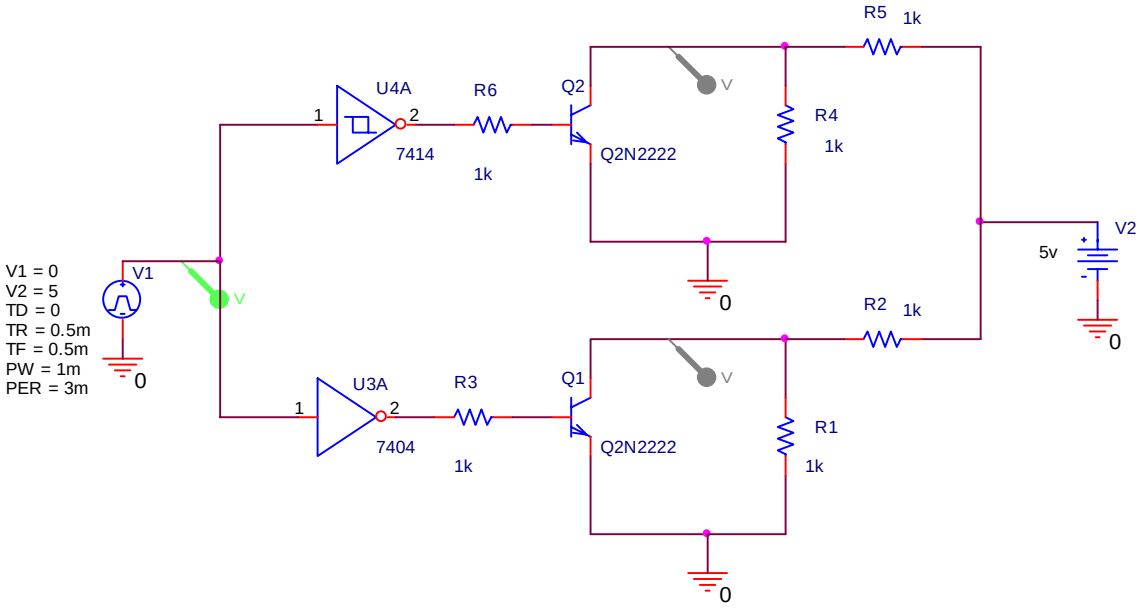

Figure C-4

- Run a simulation
  - Create a simulation for this circuit. Use a run time of 3ms and a step size of 3us. This should show a single input pulse.
  - Run the simulation.
  - Mark the locations on the plot where the Schmitt trigger causes transistor Q2 to switch.
  - Mark the locations on the plot where the inverter causes the transistor Q1 to switch.
  - Print this plot and include it in your report.
  - What is the voltage at the output voltage marker when transistor Q2 is open? Why is it at this voltage?

- Alter the values of the resistors to change the magnitude of the output voltage.
  - Change R2 and R5 to 100 ohms. Also change R1 and R4 to 10K ohms.
  - Rerun the simulation.

- What happened to the magnitude of the output voltage when transistor Q2 is open? Why did this happen?
- You will be building a circuit like this on your protoboard to switch an electro-mechanical device called a relay.

Summary

The Schmitt trigger and the comparator are both used in digital circuitry. The Schmitt trigger inverter is used to convert an analog signal to a digital signal. It also inverts the signal. The inverter is used to invert a digital signal. Whereas the Schmitt trigger works as expected in the presence of noise, the inverter does not work well in the area between the range of voltages corresponding to LOGIC 1 and the range of voltages corresponding to LOGIC 0.

Part D – Relay Circuit

Relays: A relay is a switch that is controlled by an inductor coil. A PSpice model is shown in figure D-1 When no current is flowing through the inductor between the pins connected to the coil, the switch remains in the closed (NC) position. However, when current flows through the inductor, it forces the switch to open (NO). The switch itself is attracted by the electromagnet created by the inductor. When the relay switches state, you can hear a little click.

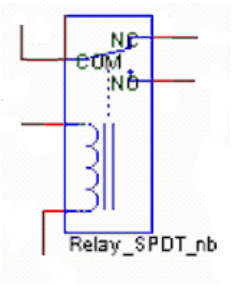

Figure D-1

The pinout for two relays are shown in figure D-2. Depending upon the brand of relay you have, the pinout may be different. If yours is not here, look up the spec sheet on the links page, or consult the staff.

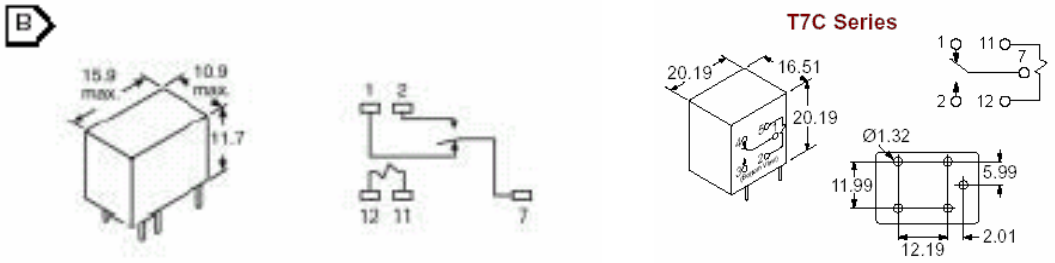

Figure D-2

Experiment

Building a switching circuit
To see how practical transistor switches can be, we will use the circuit you simulated in PSpice to control a relay. This way we will be able to hear where the two devices switch.

- Build the circuit in figure D-3 on your protoboard.
  - Note that this is ½ of the circuit you built using PSpice in part C with a relay added to the load. Instead of building the circuit twice, we can use the fact that both types of inverters have the same pinout and swap the chips in and out to observe their properties.

- This circuit requires three DC voltage sources: 5V to power the digital chip at pin 14, 9V(V2) to power the relay, and a variable DC voltage source (V3) for the input.

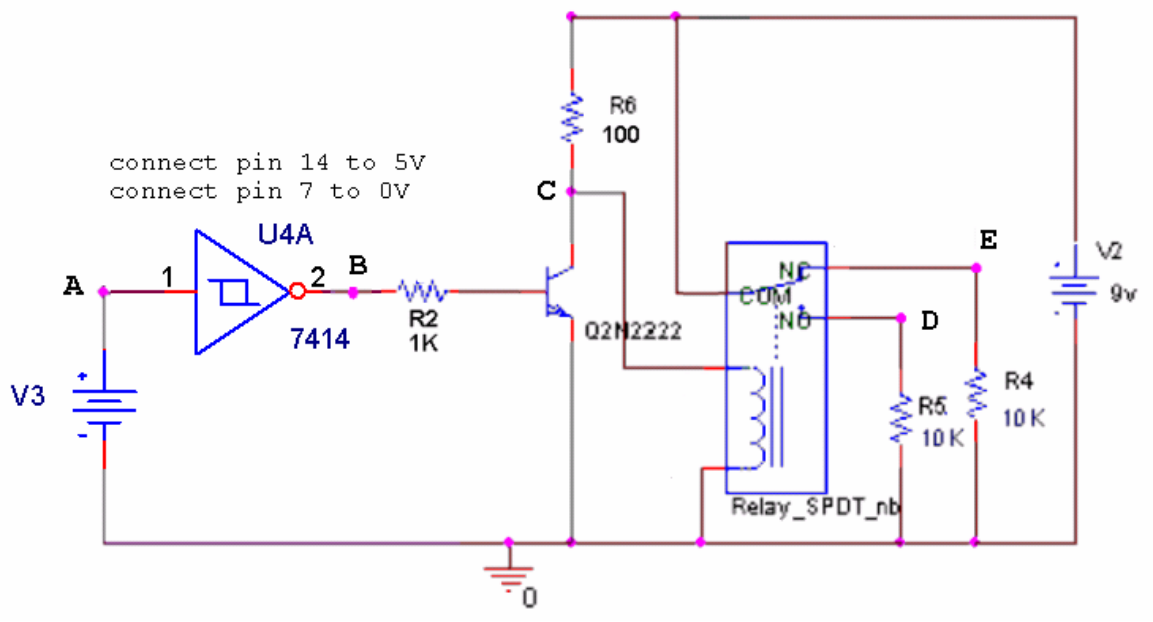

Figure D-3

- When the transistor switch is open, point C is not attached to ground directly and current flows through the inductor in the relay, and when the switch is closed, point C is connected directly to ground and no current flows through the inductor in the relay. What level of input voltage will turn the transistor on and off?
  - Warning: Do not keep the power on this circuit for prolonged periods. The 100 ohm resistor can get very hot.
  - Set V3 to a voltage of 0V.
  - Slowly turn up the input voltage until the relay clicks. Never let the voltage exceed 5V.
  - At what input voltage did you hear the relay switch? This gives us T_{upper}.
  - Now slowly turn the input voltage down again. The relay should switch back.
  - At what input voltage did you hear the relay switch? This gives us T_{lower}.
  - Are the switching voltages you found consistent with your knowledge of Schmitt triggers?
  - Put the voltage at 5V (above T_{upper}) and record the voltage levels at points A, B, C, D, and E in the table below.
  - Put the voltage at 0V (below T_{lower}) and record the voltage levels at points A, B, C, D, and E in the table below.

	A	B	C	D	E
above upper threshold					
below lower threshold					

- Now take out the Schmitt trigger inverter and replace it with a SN7404 inverter chip. What do you think will happen to the relay now?

- Set V3 to a voltage of 0V.
- Slowly turn up the input voltage until the relay clicks. Never let the voltage exceed 5V.
- At what input voltage did you hear the relay switch?
- Now slowly turn the input voltage down again. The relay should switch back.
- At what input voltage did you hear the relay switch?
- How is this different than the Schmitt trigger inverter?

Summary

In this part of the experiment we built a circuit using three devices that do electrical switching. The Schmitt trigger uses an op-amp to create a known voltage from a (possibly noisy) analog input signal. The transistor is made of a semi-conductor material that allows a small voltage at the base to switch the current through the device on and off. The relay uses an electromagnet to control a mechanical switch.

Report and Conclusions

The following should be included in your written report. Everything should be clearly labeled and easy to find. Partial credit will be deducted for poor labeling or unclear presentation.

Part A (17 points)

Include the following plots:
1) PSpice DC sweep of transistor circuit with cutoff and saturation indicated. (3 pt)
2) PSpice DC sweep of transistor circuit with voltage divided. (2 pt)
3) PSpice plot of normalized currents with active region marked. (2 pt)

Answer the following questions:
1) Draw a simplified circuit diagram for plot 1) that includes just V2, R2 and a simple switch to represent the transistor. (2 pt)
2) For your simplified circuit, when the switch is open (OFF), how much voltage will there be at Vc? When the switch is closed (ON), how much voltage will be at Vc? (2 pt)
3) What is a typical voltage across R3 in plot 2) when the switch is OFF? …when the switch is ON? (2 pt)
4) Why do you think that the values in question 3) make sense? (2 pt)
5) For what range of input voltages did the transistor act like a current amplifier? (Where was there a direct relationship between base current and the current from collector to emitter?) About what was the amplification? (2 pt)

Part B (19 points)

Include the following plots:
1) PSpice transient for the comparator with 0V reference voltage. (1 pt)
2) PSpice transient for the comparator with 1V reference voltage. (1 pt)
3) PSpice transient for Schmitt trigger with 0V reference voltage. (1 pt)
4) PSpice transient for Schmitt trigger with 1V reference voltage. (1 pt)

Answer the following questions:
1) At what input voltage level does the comparator in plot 1) switch states? (1 pt)
2) At what input voltage level does the comparator in plot 2) switch states? (1 pt)
3) What are the switching thresholds of the input for the Schmitt trigger in plot 3)? What is the hysteresis? (3 pt)
4) Use a voltage divider to prove that the values in question 3) make sense. (3 pt)

5) What are the switching thresholds of the input for the Schmitt trigger in plot 4)? What is the hysteresis? (3 pt)
6) Use a voltage divider to prove that the values in question 5) make sense. (4 pt)

Part C (20 points)

Include the following plots:
1) PSpice transient of Schmitt trigger and inverter in the presence of noise. (1 pt)
2) PSpice transient of Schmitt trigger and inverter switching transistors with transition points marked. (3 pt)

Answer the following questions:
1) From plot 1), between what input voltages does the inverter seem to be unable to find a stable output? (2 pt)
2) How do the values you found for the operating region of the inverter compare to the values of V_{IH} and V_{IL} you found on the spec sheet for the device? (2 pt)
3) From plot 1), at what input voltage level does the Schmitt trigger switch from low to high? …from high to low? What is the hysteresis? (3 pt)
4) How do the values you found for the thresholds and hysteresis of the Schmitt trigger compare to the values of V_{T+}, V_{T-}, and hysteresis you found on the spec sheet for the device? (2 pt)
5) At what input voltage does the transistor switch in plot 2) close and open when using the inverter? (2 pt)
6) At what input voltage does the transistor switch in plot 2) close and open when using the Schmitt trigger? (2 pt)
7) What effect did changing the values of the resistors R1, R2, R4 and R5 have on the output voltage? Why? (2 pt)
8) Why do you think the Schmitt trigger is preferable to an inverter in the presence of noise? (1 pt)

Part D (12 points)

Include the following plots:
1) Table of data points A, B, C, D, and E (5 pt)

Answer the following questions:
1) At what input voltage did the Schmitt trigger toggle the relay as you increased the voltage? (2 pt)
2) At what input voltage did the Schmitt trigger toggle the relay as you decreased the voltage? (2 pt)
3) Is the range found in questions 1) and 2) consistent with your PSpice results? (2 pt)
4) At what input voltage did the inverter toggle the relay? (1 pt)

Summary (12 points)

1. Summarize key points (8 pts)
2. Discuss mistakes and problems (2 pts)
3. List member responsibilities (2 pts)

Total: 80 points for write up + 20 for attendance = 100 points

Attendance: 3 classes (20 points) 2 classes (10 points) 1 class (0 points) out of 20 possible points
Minus 5 points for each late.
No attendance at all = No grade for experiment.