Digital-to-Analog Converters

If we have a system in which data is processed digitally, we usually need some kind of digital-to-analog converter (DAC) to transform the information we need into analog form. For example, music is stored digitally on a compact disk, but we need to listen to it in analog form. The circuit below is an example of a very simple DAC.
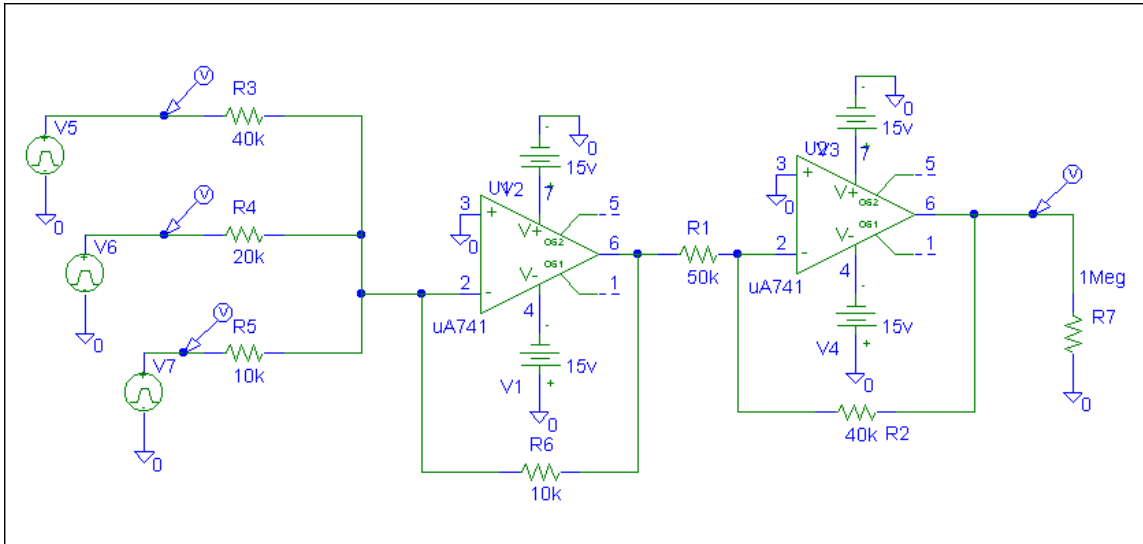
The input to this circuit is a 3-bit binary number which we can write as $A_2A_1A_0$. For this circuit, we are assuming that the digital devices are TTL so that each of the variables will take on values of 0 volts or 5 volts when the signals are low and high, respectively. For example, the number 4 written in binary form is 1 0 0 so that the respective voltages will be 5 0 0. In the circuit above, V7 is A_2, V6 is A_1, and V5 is A_0. Assume for the moment that V7 and V6 are at 0 volt while V5 is at 5 volts. This is supposed to represent the decimal number 1. The output voltage (across resistor R3) is given by the product of the gains of the two stages of amplification seen by V5.

$$V_{out} = V5*(-R2/R1)*(-R6/R3) = 5*(-40k/50k)*(-10k/40k) = 1 \text{ volt}$$

Thus, it works as it is supposed to. In general,

$$V_{out} = (V5/R3 + V6/R4 + V7/R5)*(R2/R1)*R6 = V5/5 + V6/2.5 + V7/1.25$$
$$= (4A_2 + 2A_1 + A_0)/5$$

for TTL voltages. To test out this circuit, the three voltage sources are specified to cycle on and off with different periods, resulting in the plots below. The pulses have been specified to cycle through the numbers 7 3 5 1 6 2 4 0. Notice that this circuit works the way it should since these are indeed the voltages seen during the flat tops of the pulses on the bottom trace. The ramps up and down of the voltage are due to the slew rate of the op-amps. There is a limit to how fast the output voltages in op-amps can change. This limit is called the slew rate.
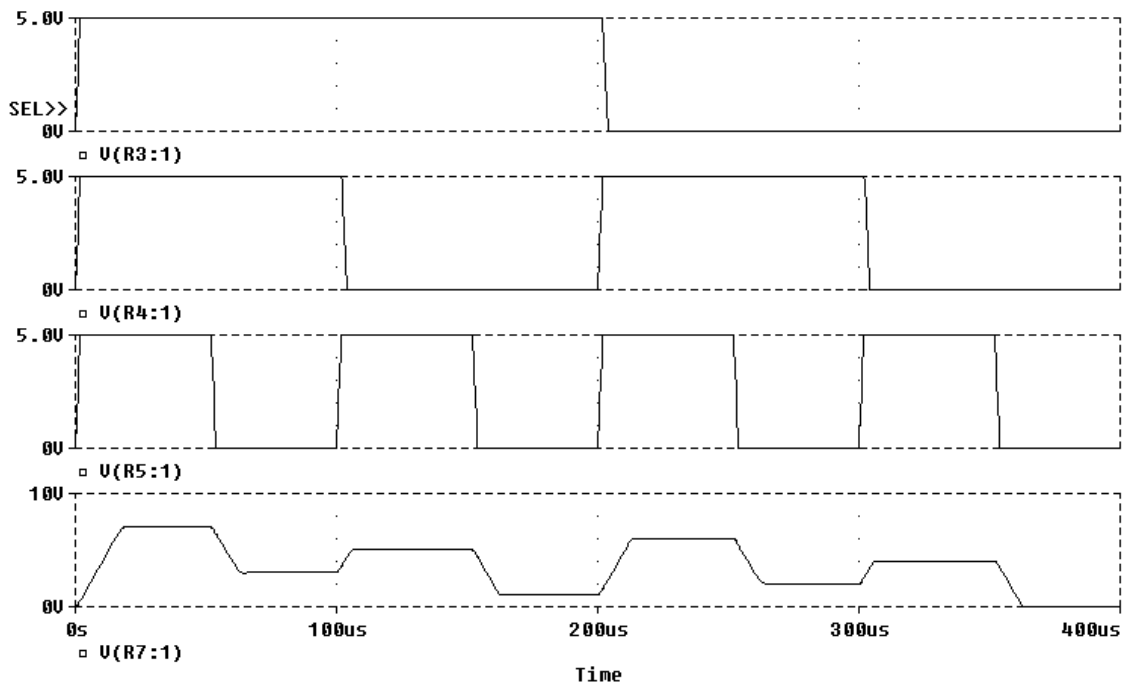
In practical application, it is very difficult to use this circuit, since it requires that the resistors all be matched very carefully. We know that resistors vary in value by typically 5-10%. We can take the time to search through a very large pile of resistors to find the ones that work exactly as we would like. However, even that is nearly impossible most of the time, since it is unlikely that we can find any resistor that is exactly its specified value. There is, fortunately, a very simple way around this problem using another resistor configuration called an R-2R ladder. A DAC with an R-2R ladder is shown below, where we have chosen R = 20k. Note that the resistors connected to the sources and ground (R3, R4, R5, R6, R9) are equal to 2R while the two resistors that bridge the source legs (R7 and R8) are equal to R. To analyze this configuration, we need to go back to the basics of resistive circuits and op-amps. Since the input current to an op-amp is zero, we can analyze this circuit as if the op-amp were absent. Starting from the same number as before $(A_2A_1A_0)$ and setting $A_0 = A_1 = 0$, we have, in effect, connected the source ends of V5 and V6 to ground. Then, all the resistors, except the 2R resistor connected to A_2, can be reduced by parallel and series combinations to a resistor equal to R. Then, by voltage division, the voltage at the + input of the op-amp is equal to $A_2*R/(R+2R) = A_2/3$. Taking similar approaches to the other two sources, we find the total voltage at the + input to be $V_+ = A_2/3 + A_1/6 + A_0/12 = (4A_2 + 2A_1 + A_0)/12$. The output of the op-amp (non-inverting configuration) is $V_{out} = (1 + R_2/R_1)V_+$. Thus, if we choose $R_2 = 1.4R_1$, we will have

$$V_{out} = (4A_2 + 2A_1 + A_0)/5 = (4V7 + 2V6 + V5)/5$$

so that if all three voltages are 5 volts, we obtain $V_{out} = 7$, as we had hoped. The voltage plots for this circuit (on the next page), show that it indeed works.
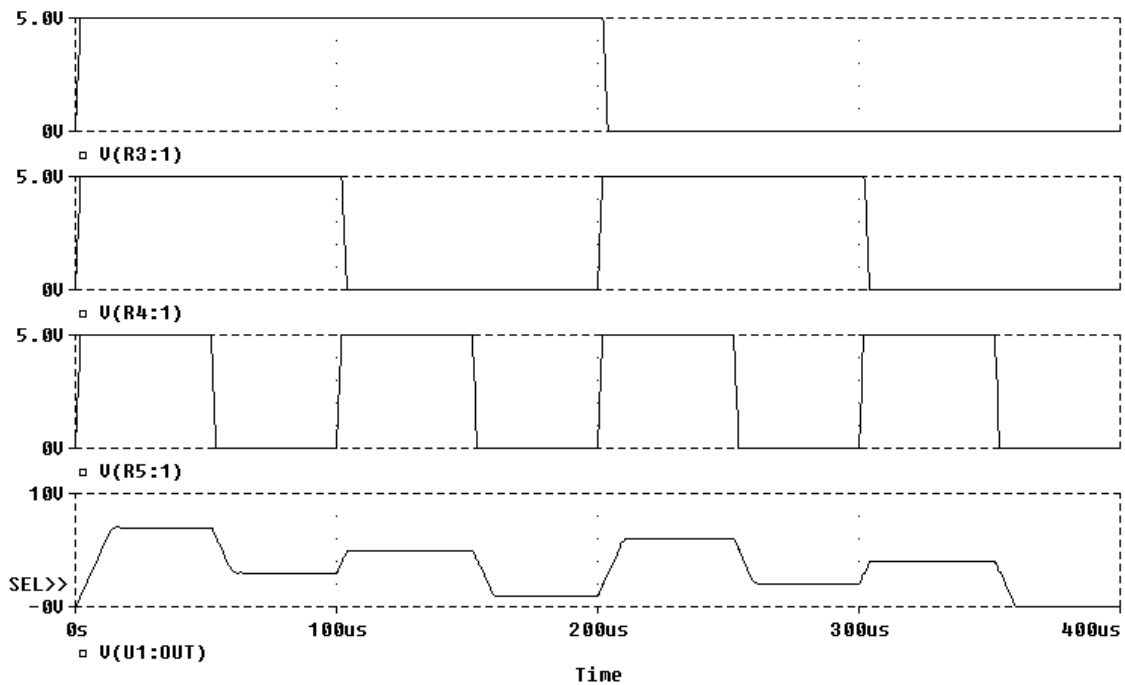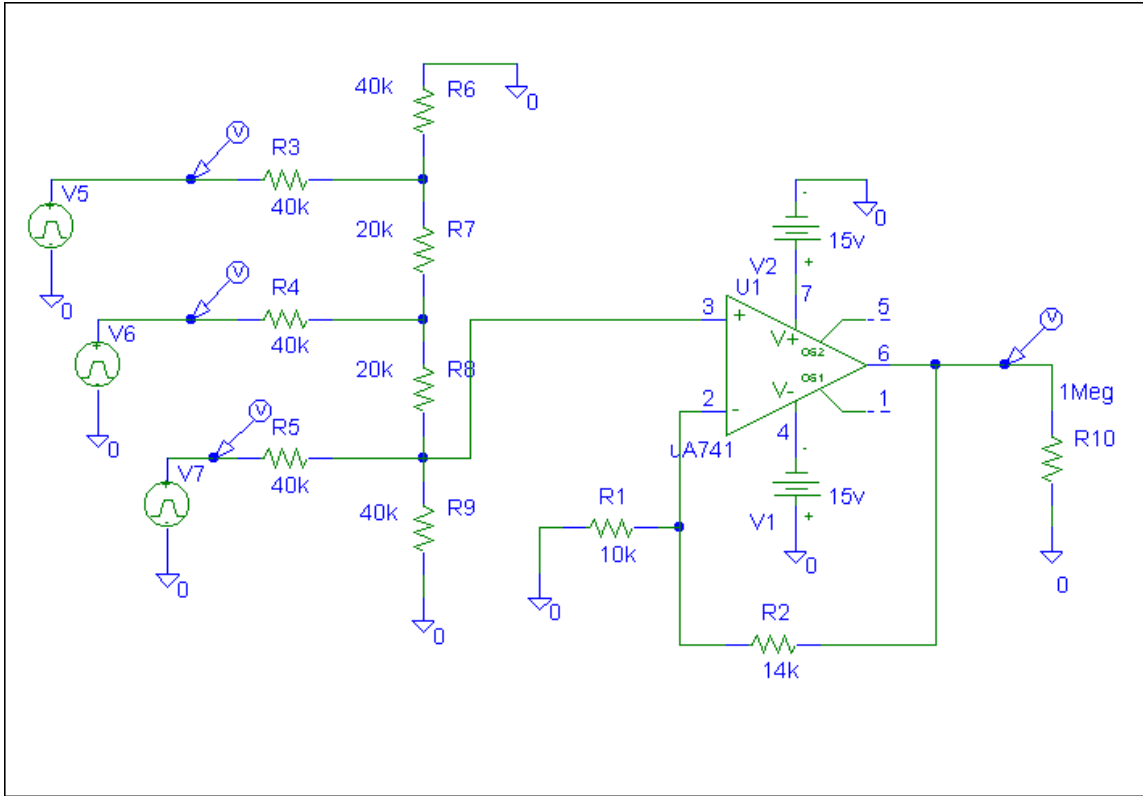
For all of the discussion above, we have assumed TTL voltage levels of 0 and 5 volts. We can generalize our results to any voltages by assuming normalized levels of 0 and 1 volt. For both DACs, this requires that we increase the overall gain by 5. For the first DAC, we can do this by changing R1 to 10k, while for the second DAC, we should change R2 to 110k.