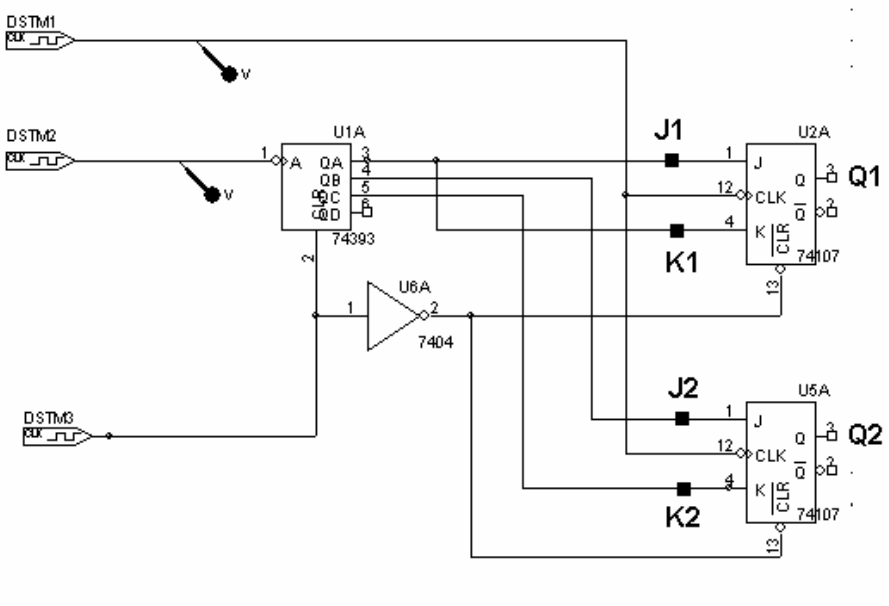
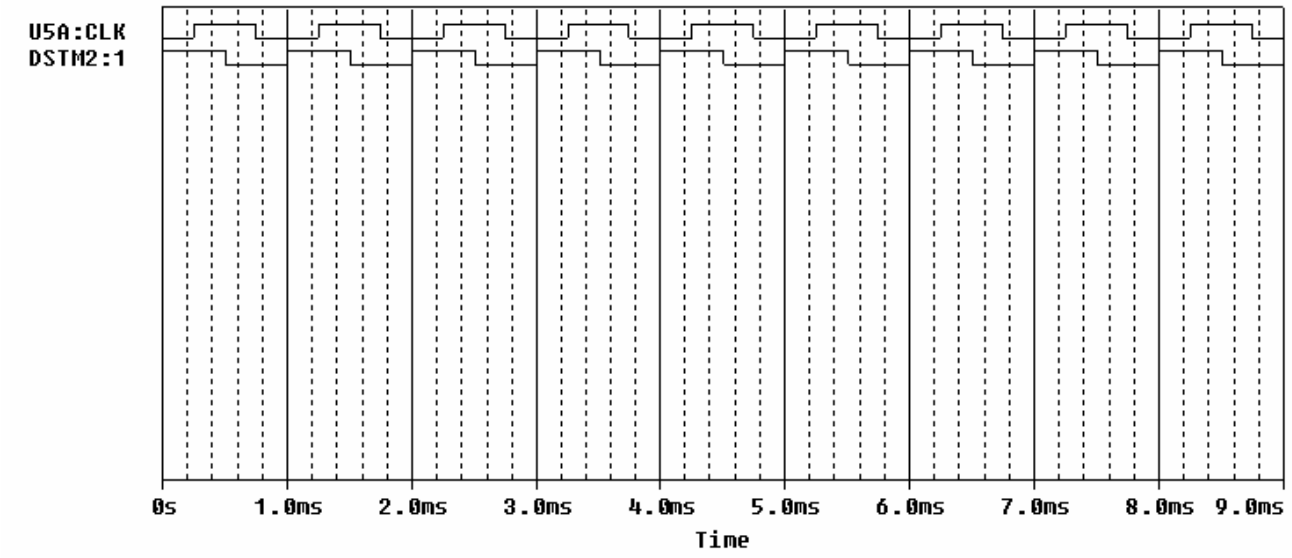
Spring 2004

Question 1 -- Flip Flops and Counters (20 points)



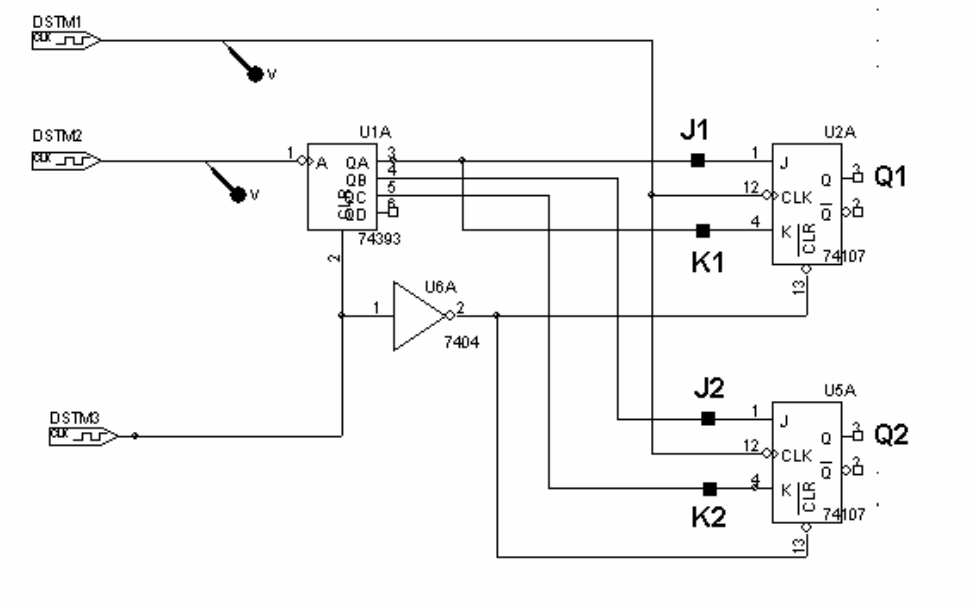
a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (flip flop clock), the second trace shown is DSTM2 (counter clock), and DSTM3 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0 and that all three devices change on the falling edge of the clock.. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2)
(3 points each = 18 points)



b) To what value does the counter count in the time frame indicated? *(2 points)*

Spring 2004 solution

Question 1 -- Flip Flops and Counters (20 points)



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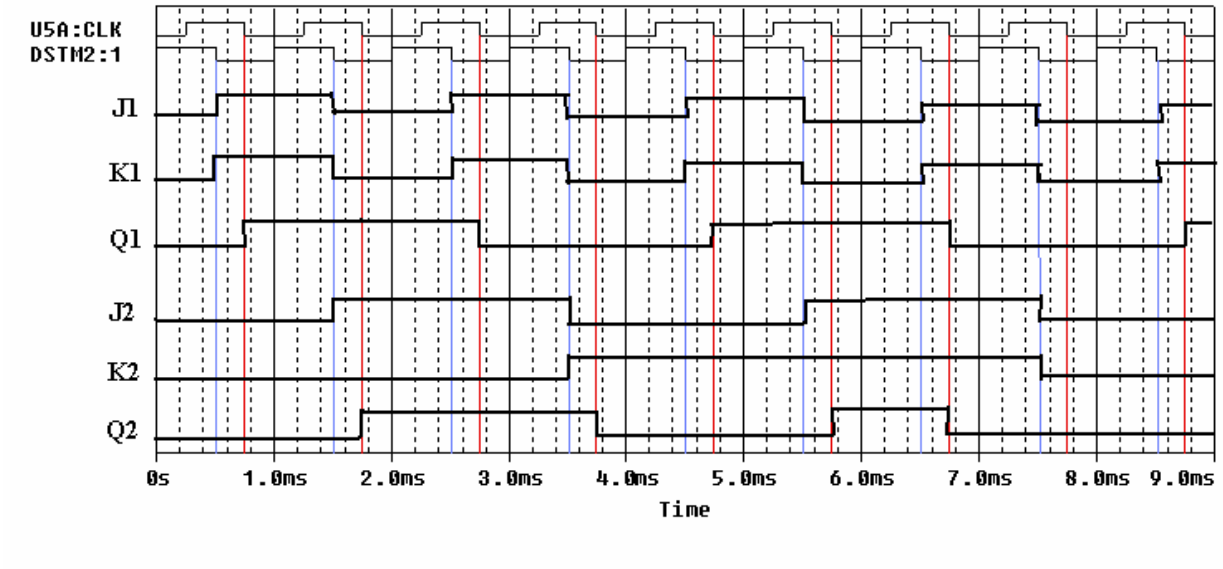
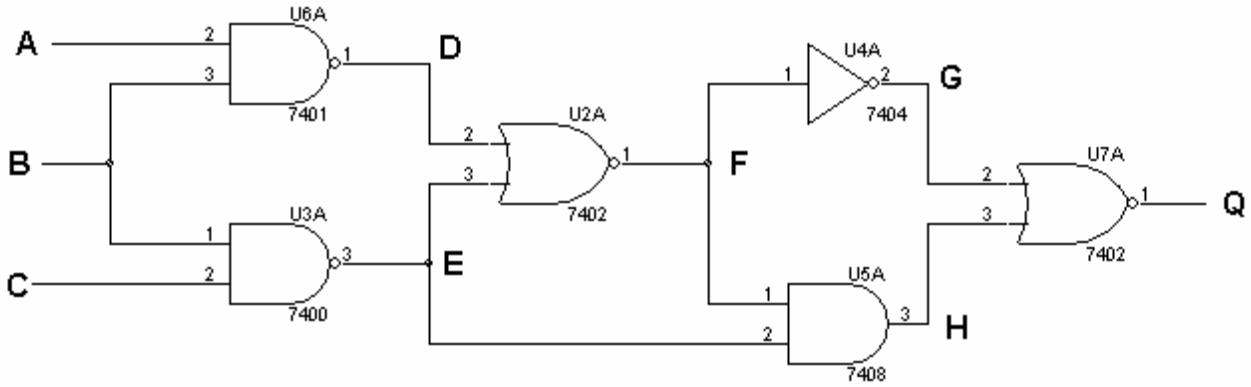


c) To what value does the counter count in the time frame indicated? *(2 points)*

1001 = ***9***

Spring 2004

Question 2 – Logic Gates (20 points)



a) Fill in the truth table for the circuit above: *(12 points)*

A	B	C	D	E	F	G	H	Q
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

b) Write the Boolean expression for the circuit in a). Do not simplify. *(6 points)*

c) What type of gate could the above circuit be replaced with to give the same results for Q based on A, B and C? *(2 points)*

1) Three input AND gate

2) Three input OR gate

3) Three input NOR gate

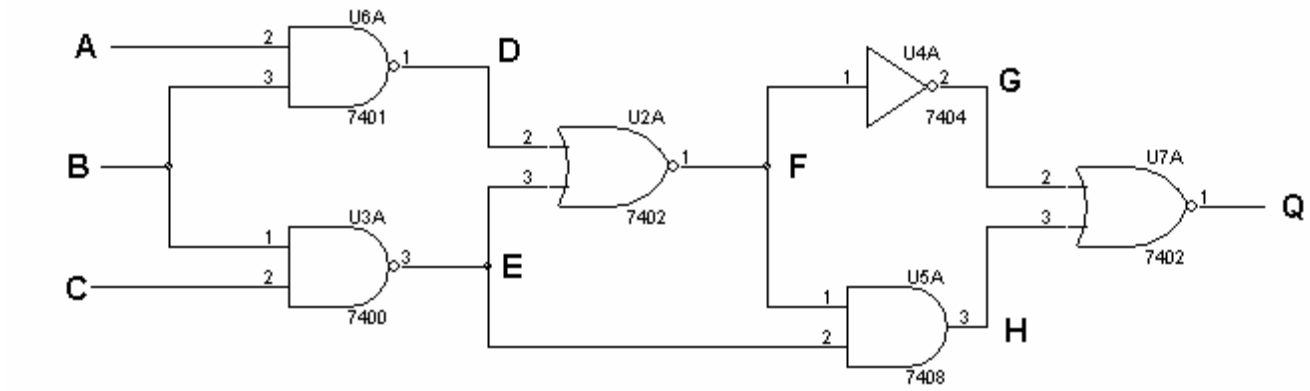
4) Three input NAND gate

5) none of the above

Extra credit *(1 point):* Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.

Spring 2004 solution

Question 2 – Logic Gates (20 points)



b) Fill in the truth table for the circuit above: *(12 points)*

A	B	C	D	E	F	G	H	Q
0	0	0	***1***	***1***	***0***	***1***	***0***	***0***
0	0	1	***1***	***1***	***0***	***1***	***0***	***0***
0	1	0	***1***	***1***	***0***	***1***	***0***	***0***
0	1	1	***1***	***0***	***0***	***1***	***0***	***0***
1	0	0	***1***	***1***	***0***	***1***	***0***	***0***
1	0	1	***1***	***1***	***0***	***1***	***0***	***0***
1	1	0	***0***	***1***	***0***	***1***	***0***	***0***
1	1	1	***0***	***0***	***1***	***0***	***0***	***1***

b) Write the Boolean expression for the circuit in a). Do not simplify. *(6 points)*
Q = ~{G + H} = ~{~F + (F&E)} = ~{~~(D+E) + (~(D+E)&E)}
G = ~F H=F&E
F=~(D+E)
E= ~(B&C) D=~(A&B)
Q = ~{ [~~(~(A&B) + ~(B&C))] + [~(~(A&B)+~(B&C)) & ~(B&C)] }

c) What type of gate could the above circuit be replaced with to give the same results for Q based on A, B and C? *(2 points)*

1) ***Three input AND gate***
2) Three input OR gate
3) Three input NOR gate
4) Three input NAND gate
5) none of the above

Extra credit *(1 point):* Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.

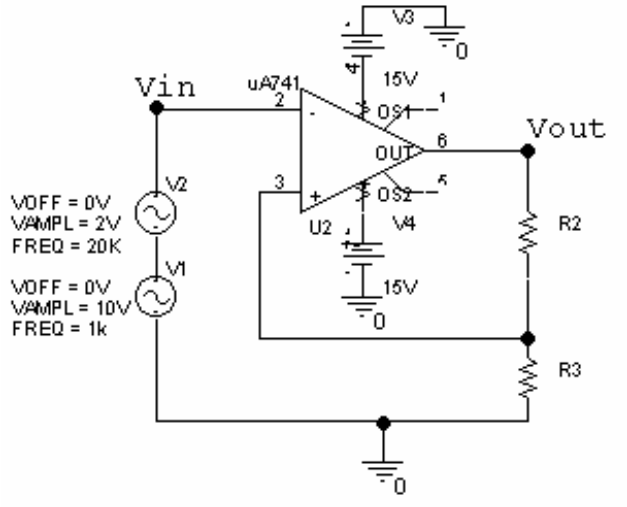
expression	rule
Q=~{[~~(~(A&B) + ~(B&C))] + [~(~(A&B)+~(B&C)) & ~(B&C)]}	*given*
Q=~{[(~A&B) + ~(B&C)] + [~(~(A&B)+~(B&C)) & ~(B&C)]}	*~~X = X*
Q=~{~[(A&B) & (B&C)] + [~~(A&B & B&C)) & ~(B&C)]}	*~X&~Y=~(X&Y)*
Q=~{~[A&B&B&C] + [(A&B&B&C) & ~(B&C)]}	*~~X = X*
Q=~{~[A&B&C] + [(A & (B&C) & ~(B&C)]}	*X&X=X*
Q=~{~[A&B&C] +[A&0]}	*X&~X=0*
Q=~{~{A&B&C] + 0 }	*X&0=0*
Q=~~{A&B&C}	*X+0=X*
Q= A&B&C	*~~X=X*

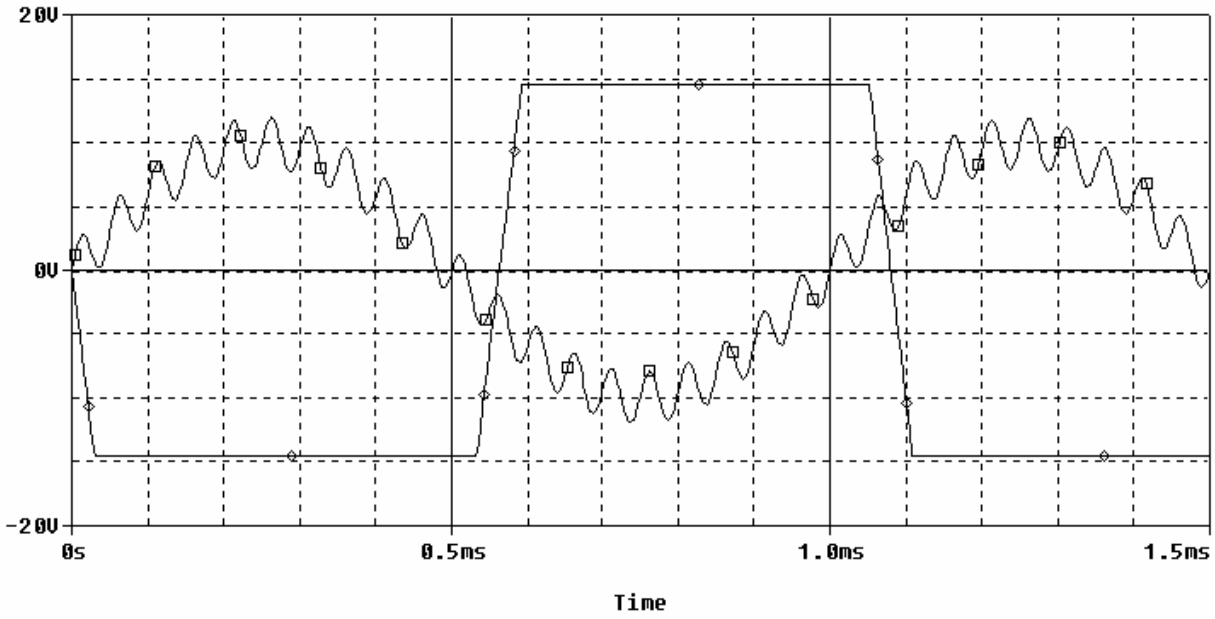
QED

Fall 2002

Question 3) Schmitt Trigger Model (25 Points)

Below is a model of a Schmitt trigger, which uses an op amp and two voltage sources. The first source, V1, represents the source voltage and the second source, V2, represents noise on the signal. The plot below the circuit is the PSpice output from this circuit.





a) Indicate Vin and Vout for the model of a Schmitt trigger above on the output plot below (4 pts).

b) Estimate the value of the hysteresis for the Schmitt trigger model AND indicate the hysteresis range on the output plot. (8 pts).

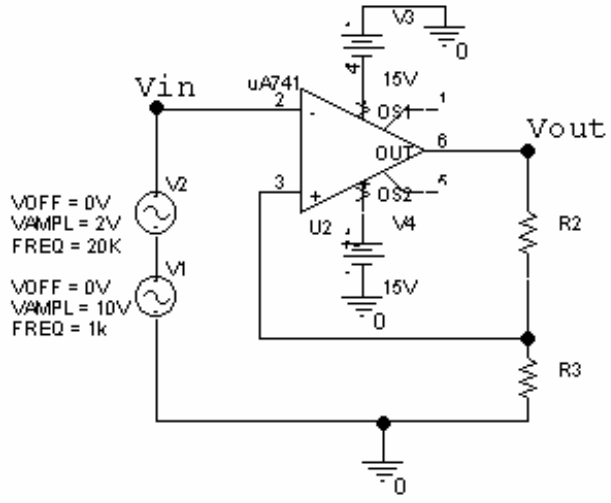
c) What is the saturation voltage range of the op-amp in the model? (4 pts)

e) If R2 is 120K ohms, then what does R3 have to be to give results similar to the output plot pictured.? (9 pts)

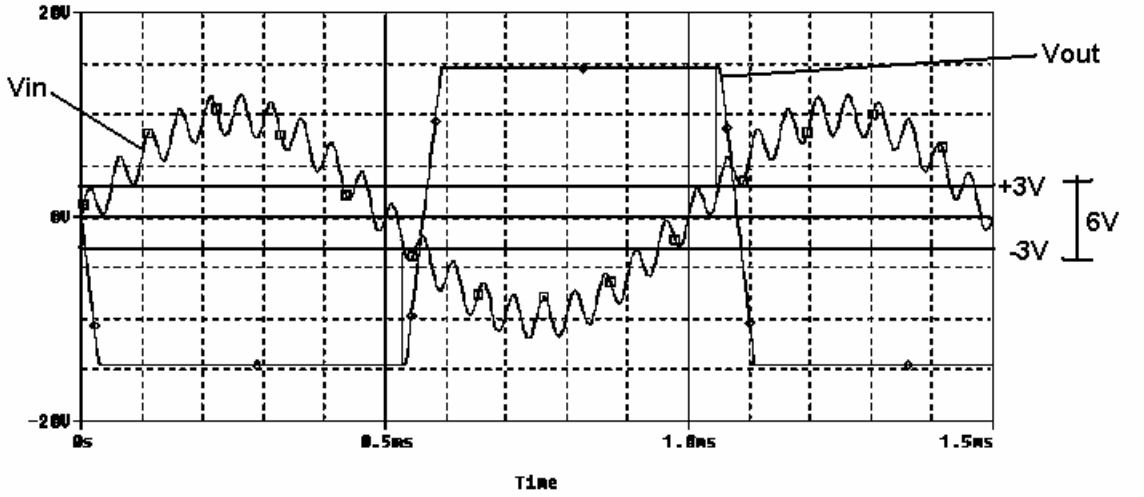
Fall 2002 Solution

Question 3) Schmitt Trigger Model (25 Points)

Below is a model of a Schmitt trigger, which uses an op amp and two voltage sources. The first source, V1, represents the source voltage and the second source, V2, represents noise on the signal. The plot below the circuit is the PSpice output from this circuit.



a) Indicate Vin and Vout for the model of a Schmitt trigger above on the output plot below (4 pts).



b) Estimate the value of the hysteresis for the Schmitt trigger model AND indicate the hysteresis range on the output plot. (8 pts).

The point of transition seems to be at +3 volts and –3 volts. This makes the hysteresis 6 volts. (Answers may vary from about +/-2 to +/-4 depending on your interpretation.)

c) What is the saturation voltage range of the op-amp in the model? (4 pts)

The amp saturates at +14.6 is the positive and –14.6 in the negative. (Answers may vary, they should be consistent with the plot.) If there is no plot given, a saturation range from +/-14 (book) to +/-15(class) is acceptable.

a) If R2 is 120K ohms, then what does R3 have to be to give results similar to the output plot pictured.? (9 pts)

[R3/(R2+R3)] Vout = Vref Vref=+/- 3V Vout = +/- 14.6V

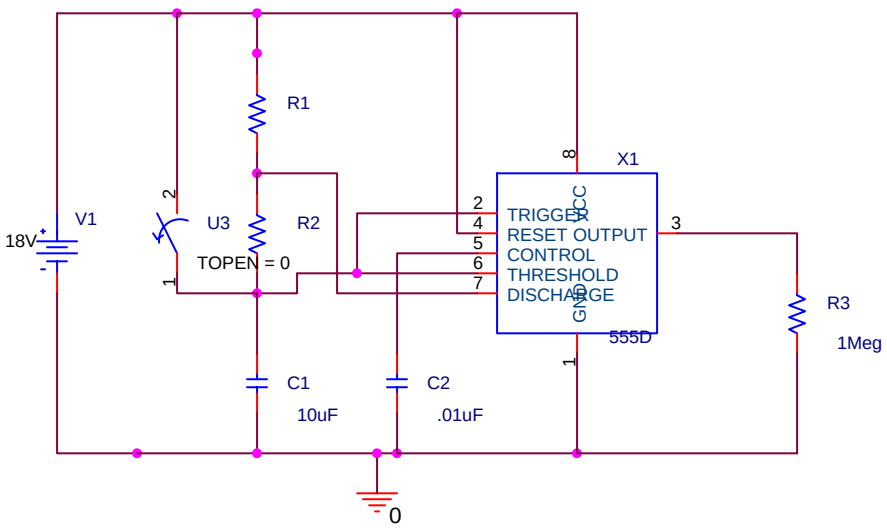
[R3/(120+R3)](14.6)=3 14.6R3=3(120K+R3) 11.6R3=360K R3=31K ohms

R3 = 31K ohms

(This answer depends on part b and part c, so answers will vary.)

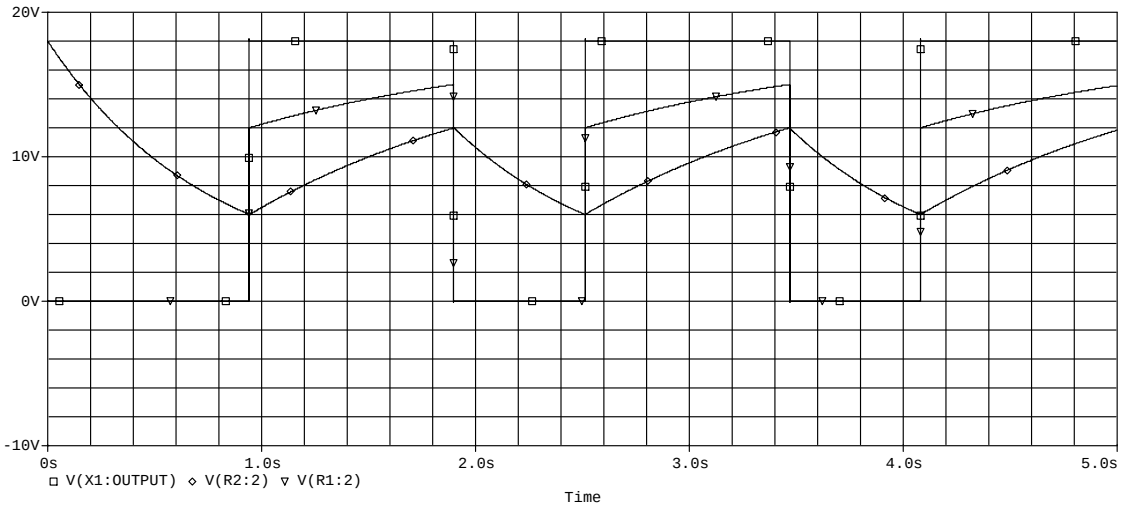
Fall 2003

Question 1 -- Astable Multivibrator



The circuit above has been simulated using PSpice. Using PROBE, the voltages at pins 2, 6, 7, and 3 have been displayed.

a. Label which trace goes with which pin (2,3,6,7) in each time period. Be sure that you label the traces in both the on and off parts of the pulse cycle. *(8 points)*

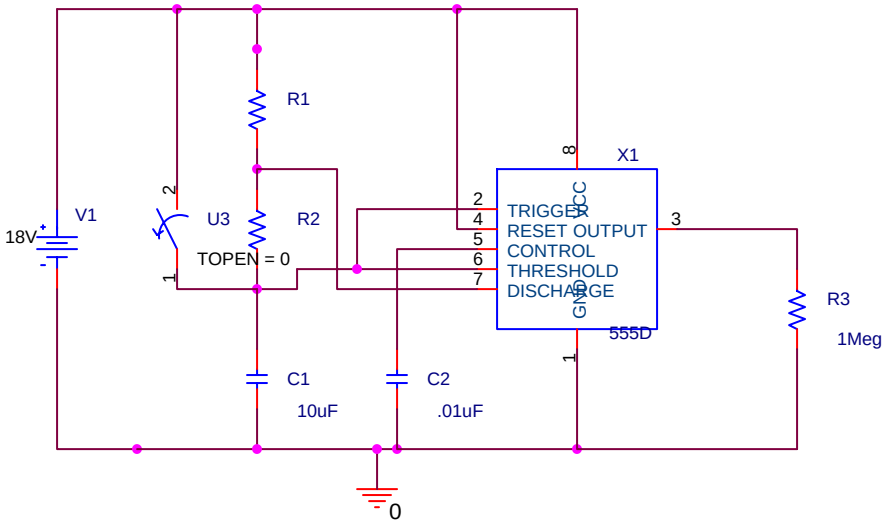


b. What is the duty cycle of the pulses in the plot? *(4 points)*

b. Determine the values of R1 and R2 from the information in this plot. *(4 points)*

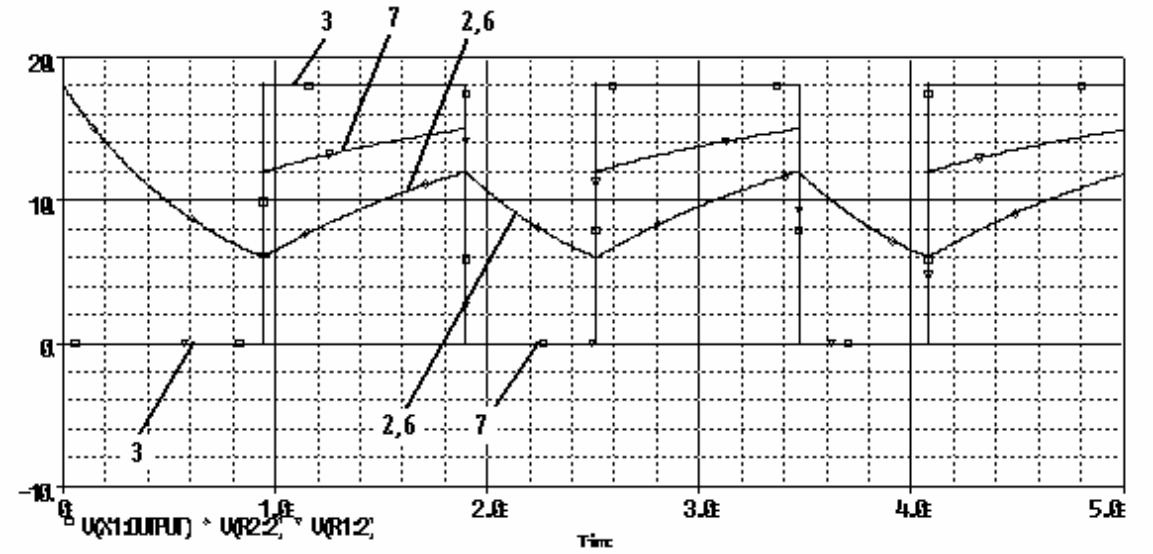
c. What could you do to increase the duty cycle of the pulses? *(4 points)*

Fall 2003 Solution
Question 1 -- Astable Multivibrator



The circuit above has been simulated using PSpice. Using PROBE, the voltages at pins 2, 6, 7, and 3 have been displayed.

a. Label which trace goes with which pin (2,3,6,7) in each time period. Be sure that you label the traces in both the on and off parts of the pulse cycle. *(8 points)*



b. What is the duty cycle of the pulses in the plot? *(4 points)*

T1 = 0.96s T2=0.60s T=1.56s

duty cycle = T1/T = .615 ***duty cycle = 61.5% (answers may vary)***

b. Determine the values of R1 and R2 from the information in this plot. *(4 points)*

T2 = 0.693(R2)(C1) 0.6=0.693(R2)(10EE-6) R2=0.0866EE6 ***R2=86.6K ohms***

T1=0.693(R1+R2)(C1) 0.96=0.693(R1+86.6K)(10EE-6) R1+86.6K=138.5K

R1=51.9K ohms

c. What could you do to increase the duty cycle of the pulses? *(4 points)*

duty cycle = T1/T = [0.693(R1+R2)C1]=[0.693(R1+2R2)C1]=[R1+R2]/[R1+2R2]

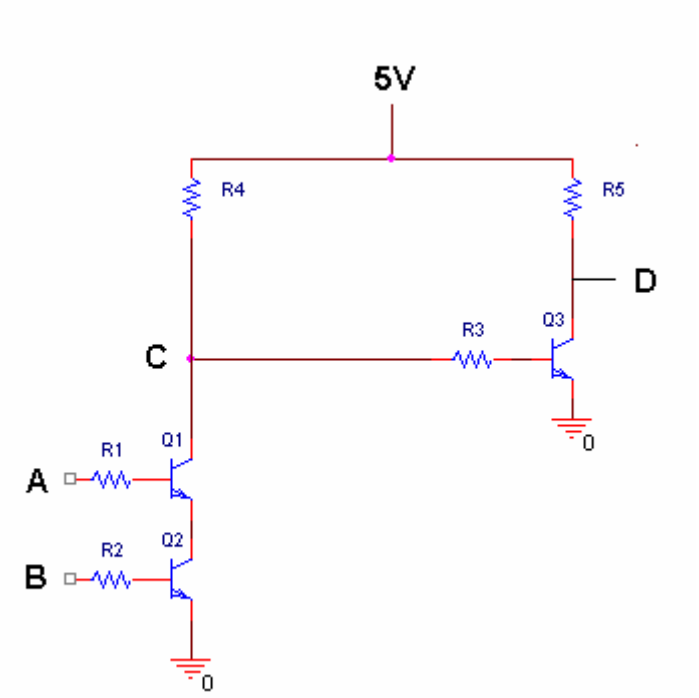
$$duty\ cycle = \frac{\frac{R1}{R2}+1}{\frac{R1}{R2}+2}$$

If R1>>R2 then the duty cycle approaches 100% -- It increases. If R1<<R2 then the duty cycle approaches 50% -- It decreases. Changing the value of the capacitor will influence the frequency, but not the duty cycle.

increase R1 or decrease R2

Spring 2004

Question 5) Transistors (20 points)



a) Redraw the figure above with the transistors modeled as a switch and a diode. (*7 points)*

c) Fill in the following table of C and D as a function of A and B based on the model you gave in part a). *(8 points)*

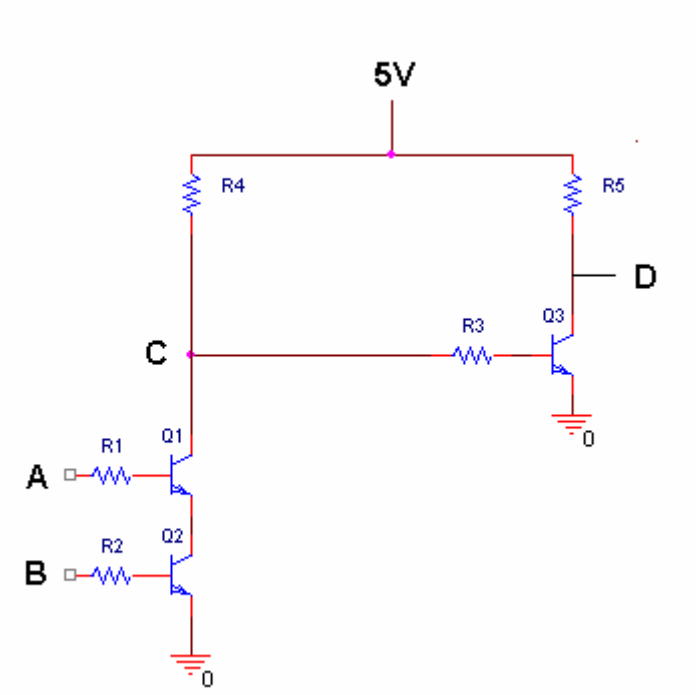
A	B	C	D
0V	0V		
0V	5V		
5V	0V		
5V	5V		

b) If we assume the output of this gate is measured at D, what kind of gate is it? *(5 points)*

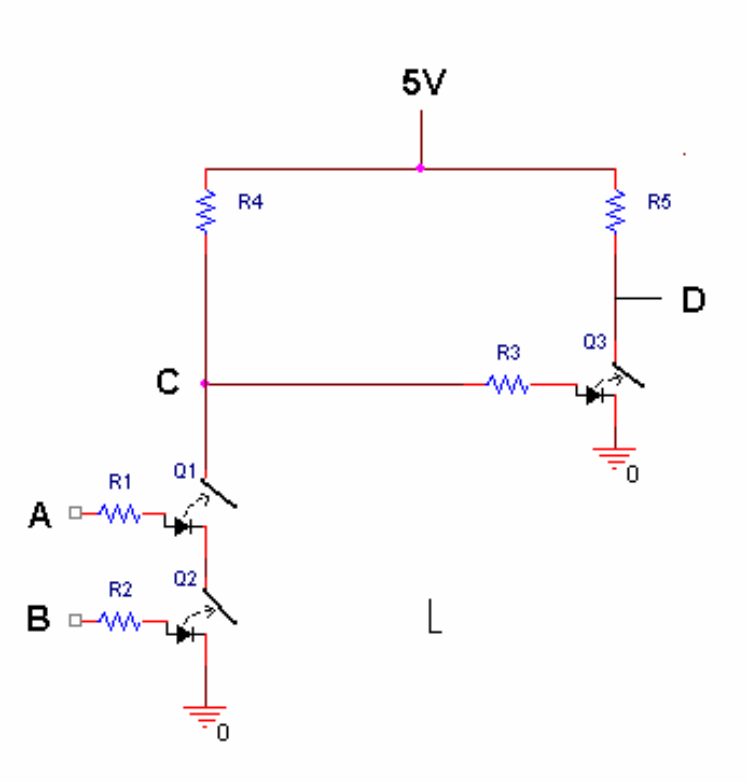
a. AND
b. NAND
c. OR
d. NOR
e. XOR
f. None of the above

Spring 2004 solution

Question 5) Transistors (20 points)



c) Redraw the figure above with the transistors modeled as a switch and a diode. (*7 points)*



c) Fill in the following table of C and D as a function of A and B based on the model you gave in part a). *(8 points)*

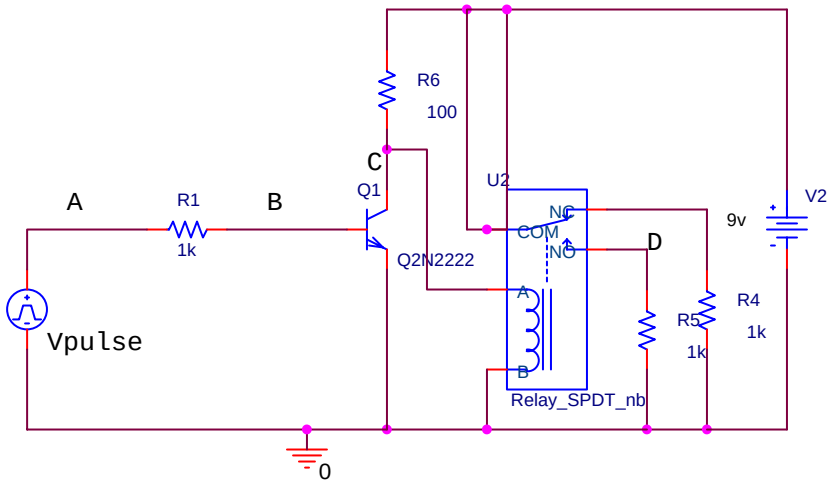
A	B	C	D
0V	0V	***5V***	***0V***
0V	5V	***5V***	***0V***
5V	0V	***5V***	***0V***
5V	5V	***0V***	***5V***

d) If we assume the output of this gate is measured at D, what kind of gate is it? *(5 points)*

a. ***AND***
b. NAND
c. OR
d. NOR
e. XOR
f. None of the above

Fall 2000

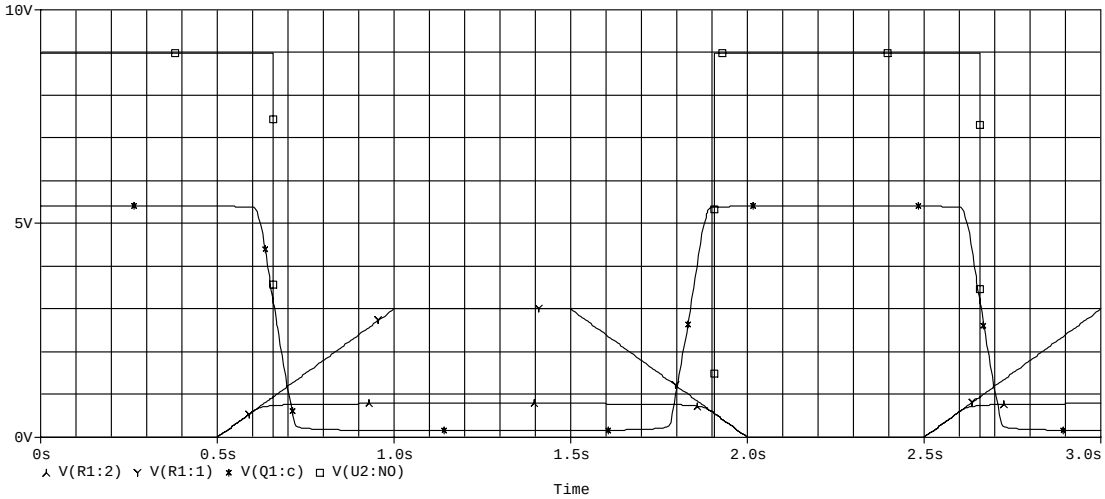
5. **Transistor Switch – Relay Circuit**

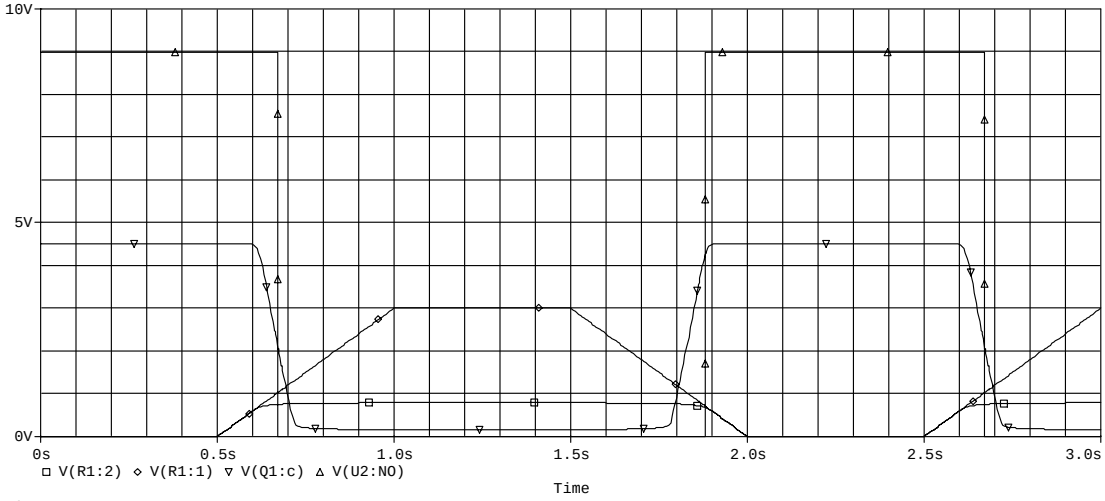


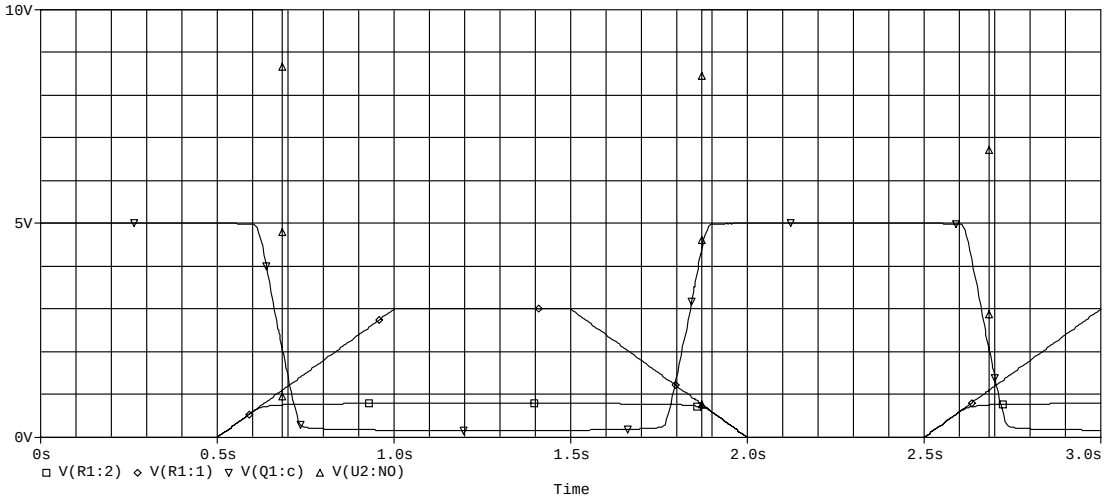
In the circuit above, the voltage source Vpulse puts out a sequence of pulses and the voltages at the source and three other points are monitored (marked A, B, C and D). You will note that this circuit is like the one we used in Exp 10 and in the Clapper project. The relay model used by PSpice (which gives switch times, circuit parameters, etc.) is listed below:

X_U2 N00064 0 N00350 N00343 N00087 Relay_Spdt_Bhv PARAMS:
+ T_make=20m
+ T_break=10m
+ I_pull=35ma
+ I_drop=25ma
+ R_coil=100
+ L_coil=5mH
+ R_open=100MEG
+ R_close=.05

Using this information and the overall circuit diagram, identify which of the following plots goes with this circuit?

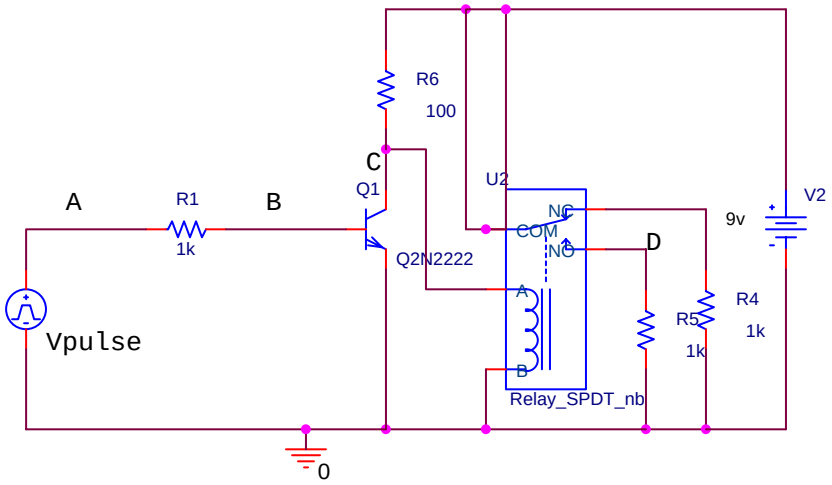

10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time


10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time


10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time

Fall 2000 Solution

Transistor Switch – Relay Circuit

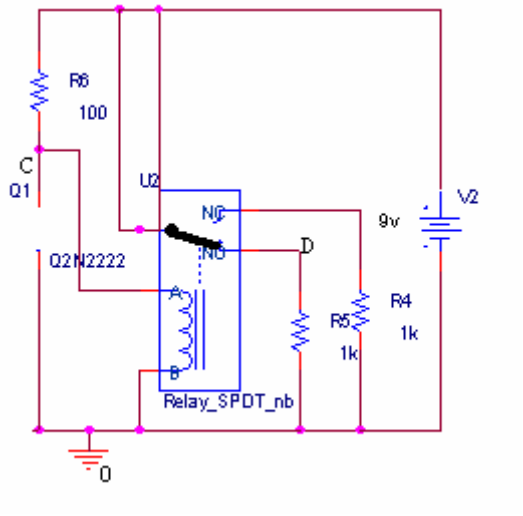


In the circuit above, the voltage source Vpulse puts out a sequence of pulses and the voltages at the source and three other points are monitored (marked A, B, C and D). You will note that this circuit is like the one we used in Exp 10 and in the Clapper project. The relay model used by PSpice (which gives switch times, circuit parameters, etc.) is listed below:

X_U2 N00064 0 N00350 N00343 N00087 Relay_Spdt_Bhv PARAMS:
+ T_make=20m
+ T_break=10m
+ I_pull=35ma
+ I_drop=25ma
+ R_coil=100 *(This is important)*
+ L_coil=5mH
+ R_open=100MEG
+ R_close=.05

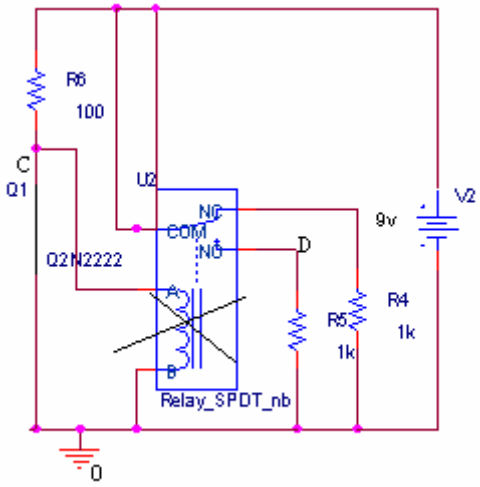
Using this information and the overall circuit diagram, identify which of the following plots goes with this circuit?

Answer:Vpulse is off(0 volts) → VA = 0V (pulse low) and VB = 0V (pulse low) → diode is off → current flows through relay → relay switch at NO

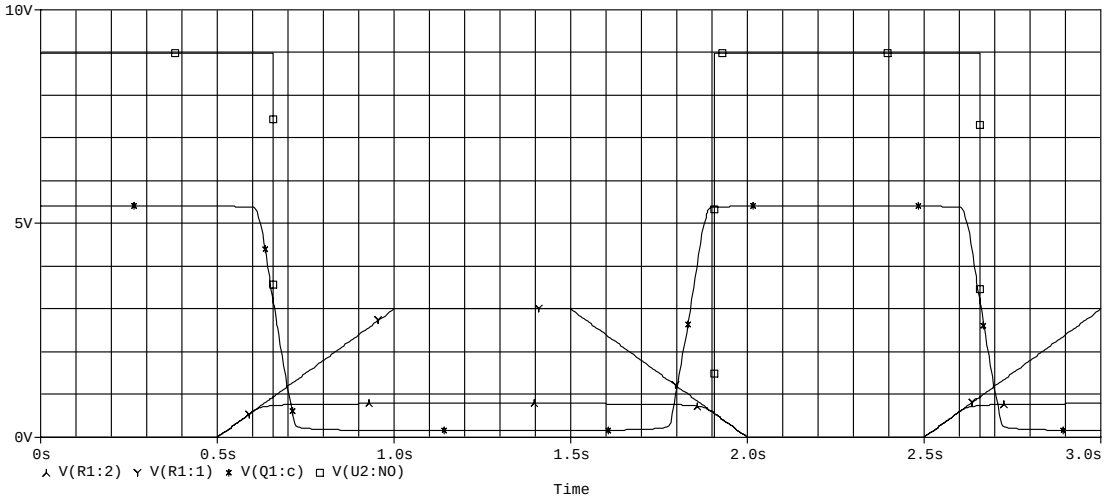


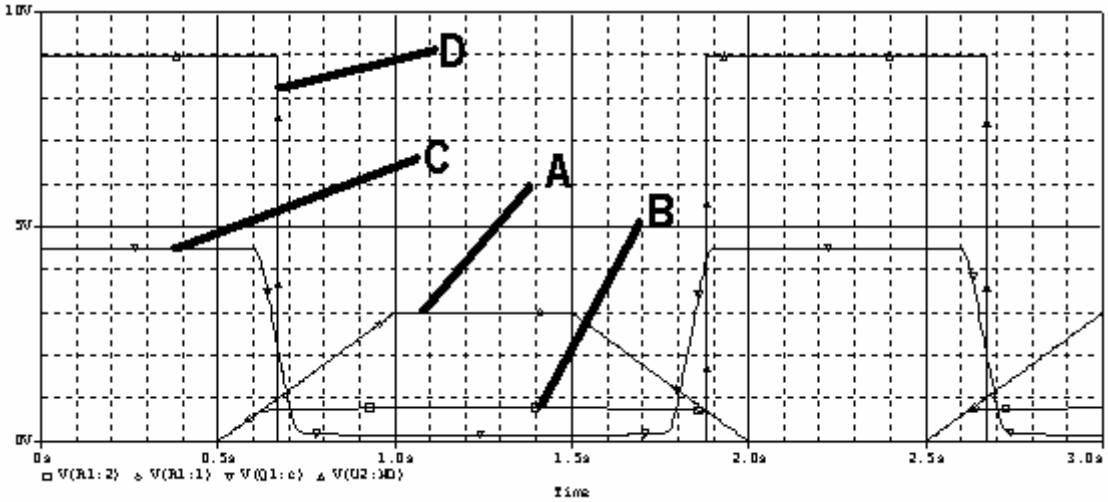
VD = 9V
*VC = V2*R_{relay}/(R_{relay} + R6) =9(100)/(100+100) = 4.5V*

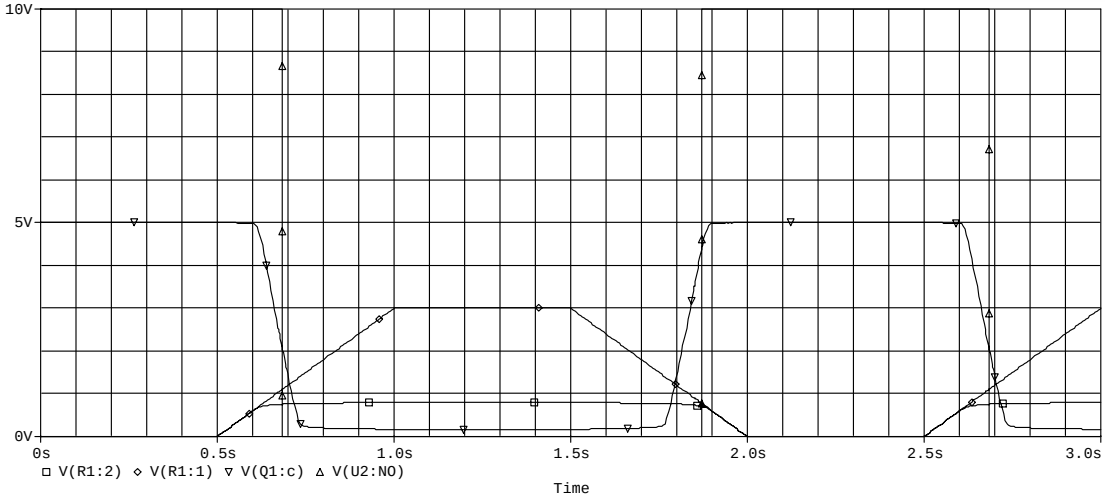
Vpulse is on(3 volts) → VA = 3V (pulse high) and VB = 0.6 volts (drop across diode when on) → diode is on → no current flows through relay → relay switch at NC



VC = 0 V (There is actually a 0.2 voltage drop across the transistor when it is shorted which you can see, if you look.)
VD = 0 V (NO is not attached to anything)


10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time


D
C
A
B
10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time


10V
5V
0V
0s
0.5s
1.0s
1.5s
2.0s
2.5s
3.0s
V(R1:2) V(R1:1) V(Q1:c) V(U2:NO)
Time