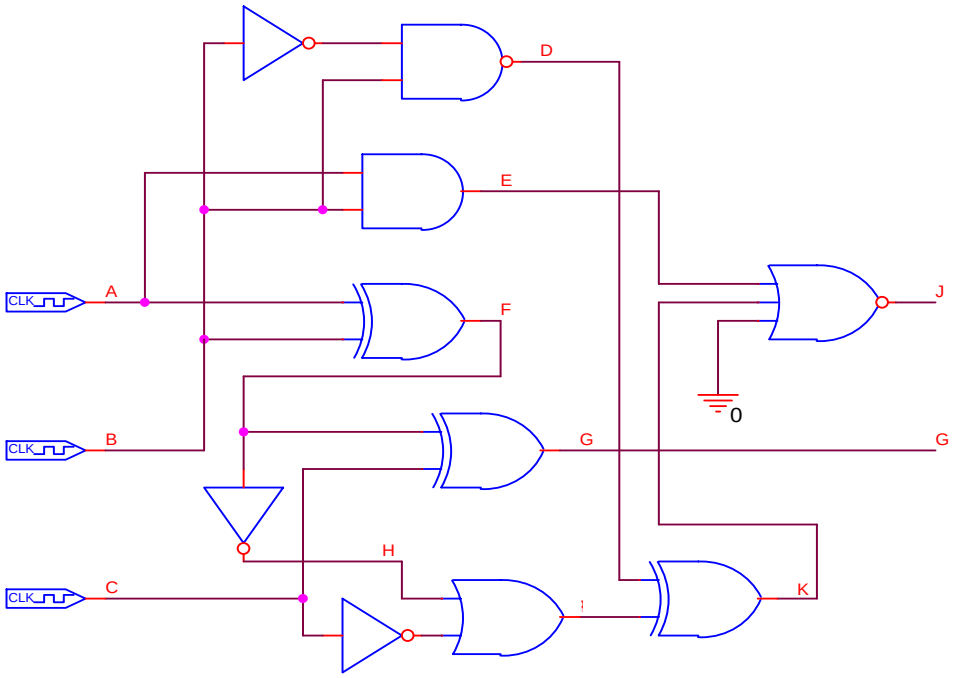
# ENGR4300 Test 3B
# Spring 2005

**Name**_____

**Section** _____

**1) Combinational Logic (25 points)**



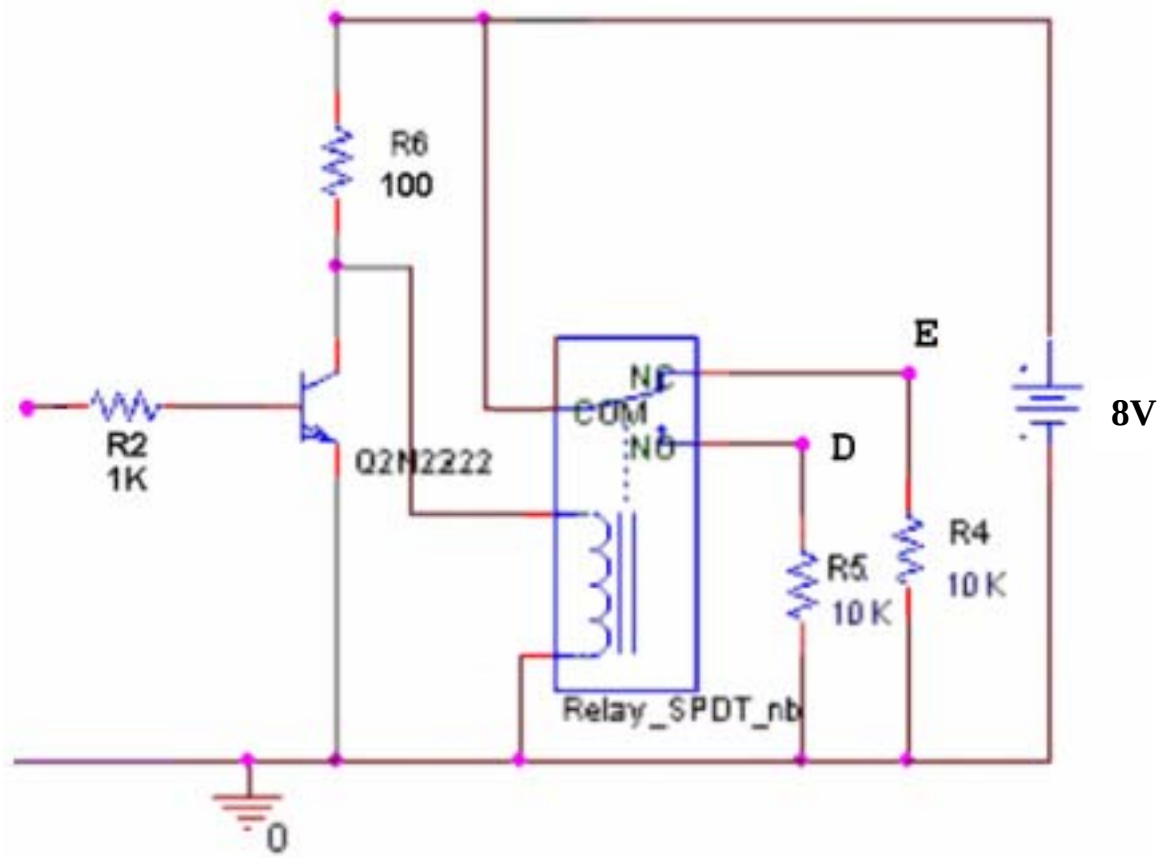

A. From the truth table for all marked points in the above circuit. (2 points each column D-K = 16 points)

| A | B | C | D | E | F | G | H | I | J | K |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | ***1*** | ***0*** | ***0*** | ***0*** | ***1*** | ***1*** | ***1*** | ***0*** |
| 0 | 0 | 1 | ***1*** | ***0*** | ***0*** | ***1*** | ***1*** | ***1*** | ***1*** | ***0*** |
| 0 | 1 | 0 | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** |
| 0 | 1 | 1 | ***1*** | ***0*** | ***1*** | ***0*** | ***0*** | ***0*** | ***0*** | ***1*** |
| 1 | 0 | 0 | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** |
| 1 | 0 | 1 | ***1*** | ***0*** | ***1*** | ***0*** | ***0*** | ***0*** | ***0*** | ***1*** |
| 1 | 1 | 0 | ***1*** | ***1*** | ***0*** | ***0*** | ***1*** | ***1*** | ***0*** | ***0*** |
| 1 | 1 | 1 | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***1*** | ***0*** | ***1*** |

B. Based on the truth table you formed, write a Boolean expression for G in terms of A, B, and C using only AND, OR, and NOT operations (i.e. you may not symbolically use the XOR operation in your expression). DO NOT SIMPLIFY. (3 points)

$$G = F \oplus C = (A \oplus B) \oplus C = (\overline{A} \bullet B + A \bullet \overline{B}) \oplus C = \overline{(\overline{A} \bullet B + A \bullet \overline{B})} \bullet C + (\overline{A} \bullet B + A \bullet \overline{B}) \bullet \overline{C}$$

C. If the open end of R2 in the following circuit is connected to output J in the circuit above and a common ground is established between both circuits, what are the *currents* flowing in R4 and R5 of this circuit when an input value of "5" (in binary) is presented to our original circuit. (Assume the input is made up of binary digits ABC, where A is the most significant bit). (6 points)



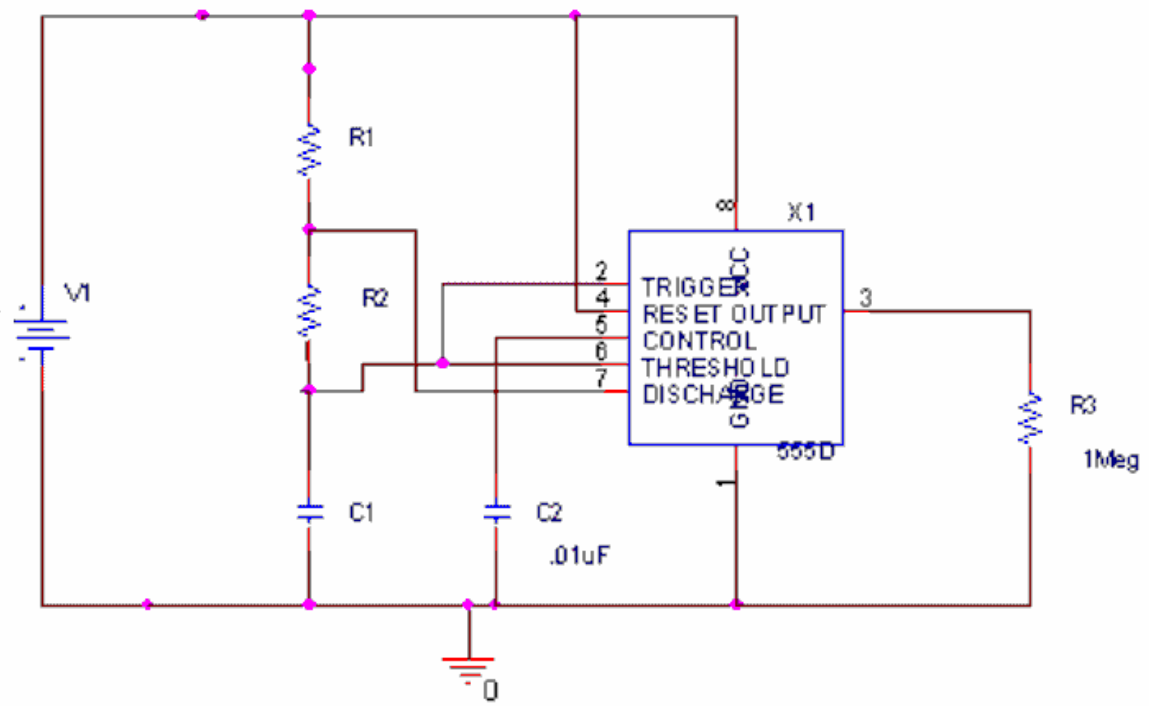

*5V = 101 Output at J is low. Transistor is open. Inductor is on. VD is 8V VE is 0V*

R4: *VE = 0V I4 = 0/10k* ***I4 = 0 mA***

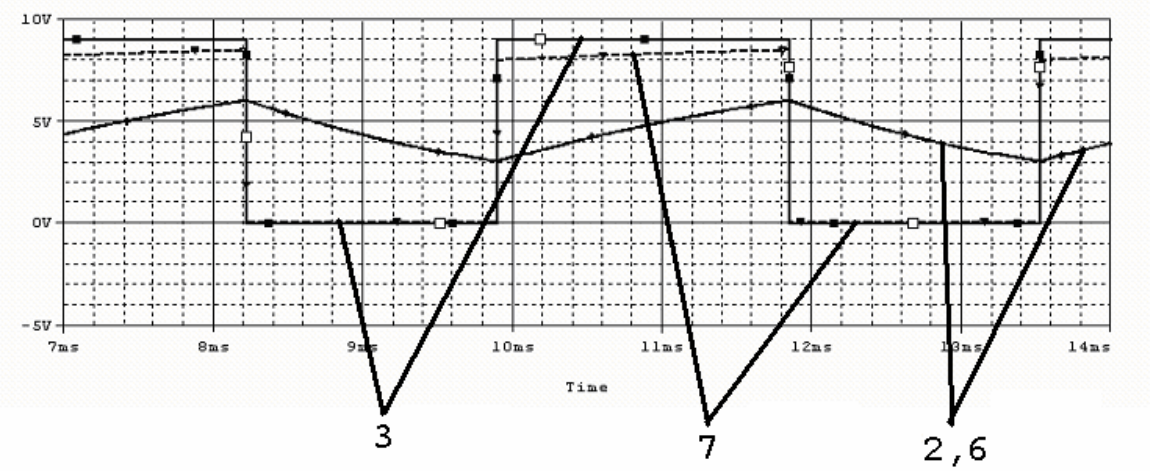
R5: *VD = 8V I5 = 8/10k* ***I5 = 0.8 mA***

Extra Credit On the back of this page, simplify the circuit from part A to use the fewest gates possible. (1 point)

**2) 555-Timer (25 points)**




The following plot was created in PSpice using the 555-Timer circuit pictured above.




a) Identify the signals that are attached to pin 2, pin 6, pin 7, and pin 3. Identify both parts of each cycle. (4 pt)

b) Using the output trace, determine the on-time, off-time and period of the output signal. (Try to be as accurate as possible.) (3 pt)

*Ton = t2-t1  Toff=t3-t2  T=Ton+Toff*
*t1=9.89ms t2=11.86ms t3=13.53ms*
***Ton=1.97ms  Toff=1.67ms  T=3.34ms  (answers may vary)***

c) Find the values for R2 and C1 given that R1 is 1K ohms. (9 pt)

*Toff = 0.693(R2)(C1)  C1=[1.67m]/[(0.693)(R2))*
*Ton = 0.693(R1+R2)C1  1.97m = [(0.693)(1k+R2)(1.67m)]/[(0.693)(R2)]*
*[1k+R2]/[R2] = 1.18  1k=(1.18-1)(R2)  R2=5.6K ohms*

*C1=[1.67m]/[(0.693)(5.6k)] = 0.43μF*

***R2 = 5.6K ohms  C1 = 0.43μF  (answers may vary)***

d) What is the time constant, τ , for the capacitor in the charge cycle of this circuit? (2 pt)

*tau (charge) = (R1+R2)(C1) = (1k+5.6k)(0.43μ) =* ***2.8ms***

e) What is the time constant, τ , for the capacitor in the discharge cycle of this circuit? (2 pt)

*tau (discharge) = (R2)(C1) = (5.6k)(0.43μ) =* ***2.4ms***

f) Using the plot, determine the input voltage, V1,  of the circuit. (2 pt)

***V1 = 9V***

g) Which of the following circuit elements are not contained in our model of the *inside* of the 555-timer chip?  You should NOT assume it is wired in astable mode or has any outside components attached to it. (Circle all that apply.) (3 points)

| | | | |
|---|---|---|---|
| comparator | transistor | ***Schmitt trigger*** | voltage divider |
| ***bridge*** | ***capacitor*** | flip flop | ***counter*** |

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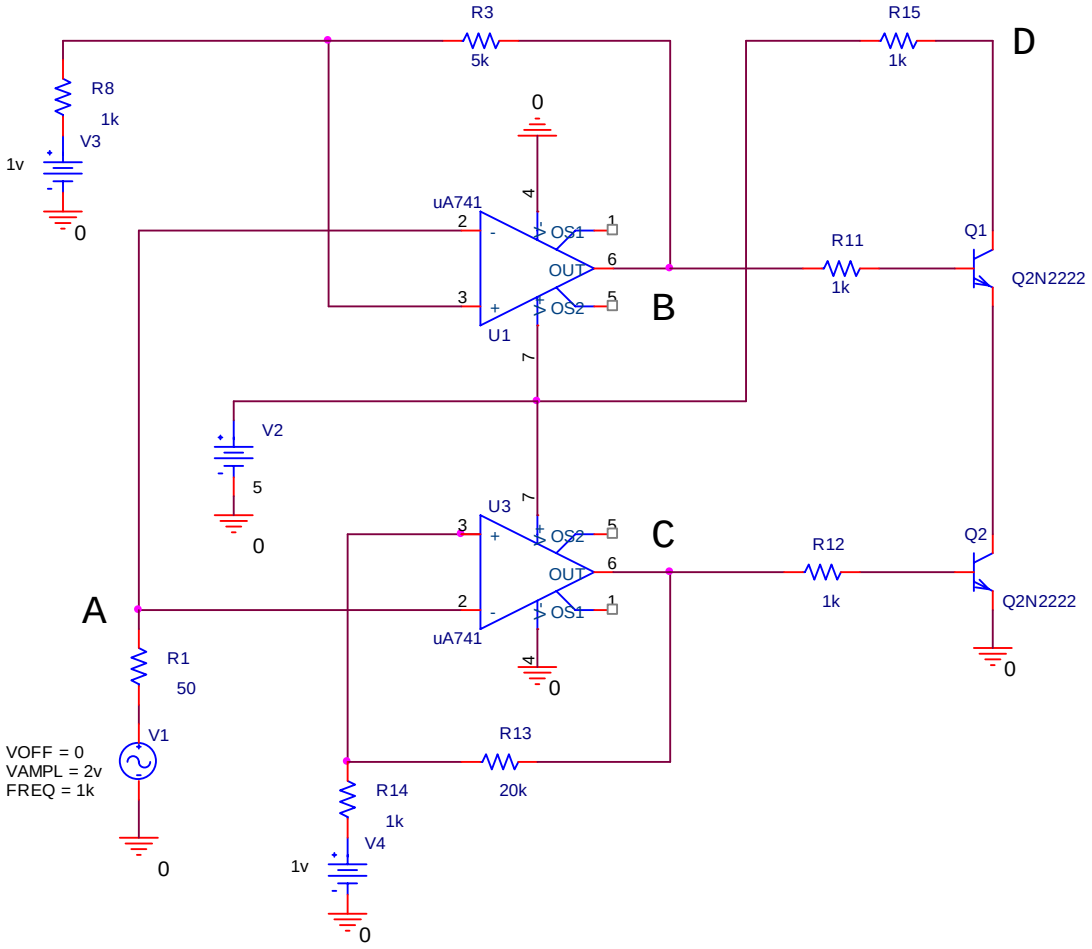
**3) Switching Circuits (30 points)**




The circuit above consists of two Schmitt triggers with the same sinusoidal input signal (point A). The output of each Schmitt trigger becomes the base signal to a transistor (points B and C). The final output of the circuit is read at point D.

a) Saturation Voltages

i) If the op-amp is ideal, what is the maximum voltage that can ever occur at points B and C? (1 pt)

***5V***

ii) If the op-amp is ideal, what is the minimum voltage that can ever occur at points B and C? (1 pt)

***0V***

b) Schmitt trigger B (using 741 op-amp U1)

i) When op-amp U1 is outputting its maximum value, what will be the voltage at the non-inverting input to Schmitt trigger B? (3 pts)

*R1=5k R2=1k Vref=1V*
*v+ = [(1k)/(5k+1k)](5V-1V) + 1V*

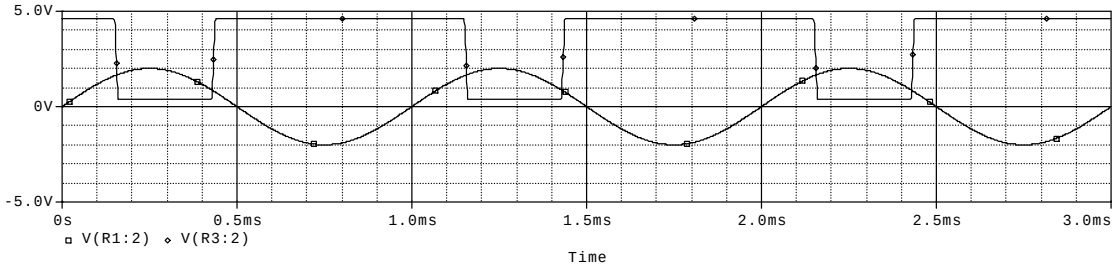
***v+ = 1.67 V***

ii) When the op-amp U1 is outputting its minimum value, what will be the voltage at the non-inverting input to Schmitt trigger B? (3 pts)

*R1=5k R2=1k Vref=1V*
*v+ = [(1k)/(5k+1k)](0V-1V) + 1V*

***v+ = 0.83V***

iii) The input at V1 is shown below. Sketch the voltage at point B. (3 pts)



c) Schmitt trigger C (using 741 op-amp U3)

i) When op-amp U3 is outputting its maximum value, what will be the voltage at the non-inverting input to Schmitt trigger C? (3 pts)

*R1=20K R2=1K Vref = 1V*
*v+ = [(1k)/(20k+1k)](5V-1V) + 1V*

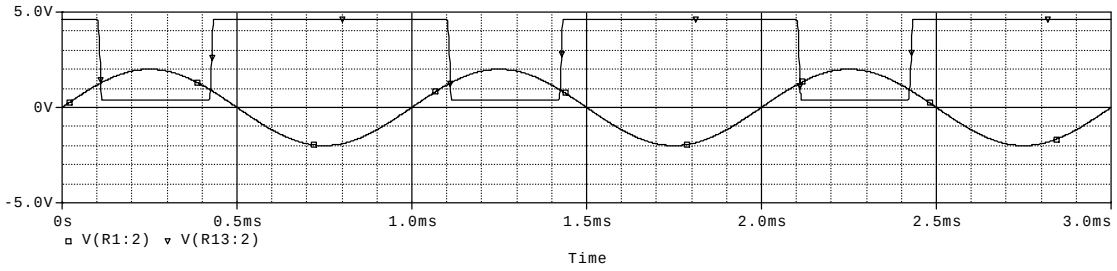
***v+ = 1.19 V***

ii) When the op-amp U3 is outputting its minimum value, what will be the voltage at the non-inverting input to Schmitt trigger C? (3 pts)

*R1=20K R2=1K Vref = 1V*
*v+ = [(1k)/(20k+1k)](0V-1V) + 1V*

***v+ = 0.95 V***

iii) The input at V1 is shown below. Sketch the voltage at point C. (3 pts)



d) Transistor Circuit

i) Fill in the following table for the voltage at D as a function of all possible combinations of outputs at B and C. (6 pts)

| B | C | D |
|---|---|---|
| 0 | 0 | 5 |
| 0 | 5 | 5 |
| 5 | 0 | 5 |
| 5 | 5 | 0 |

ii) What kind of gate does the transistor pair represent? (circle 1) (1 pt)

a. AND

b. ***NAND***

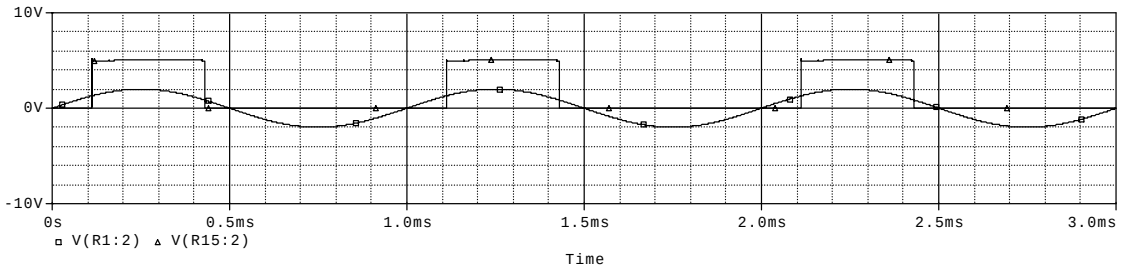
c. OR

d. NOR

e. XOR

f. None of the above

iii) Given the input signal at V1 shown below, sketch the output voltage at D. (3 pts)



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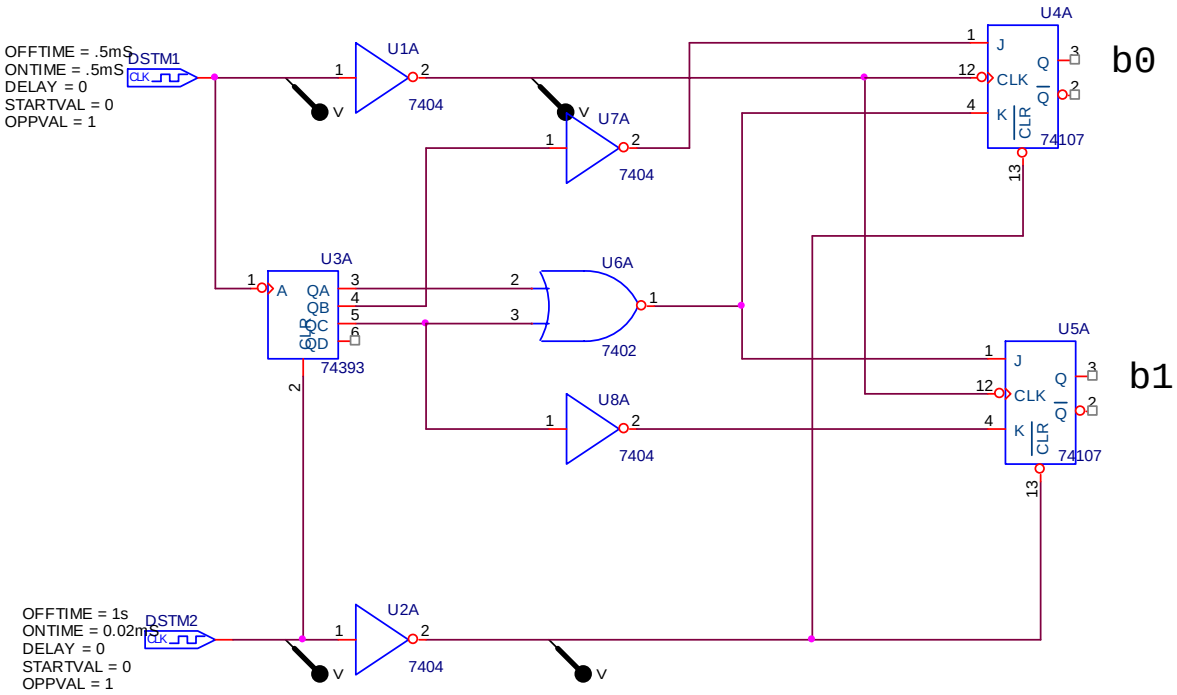
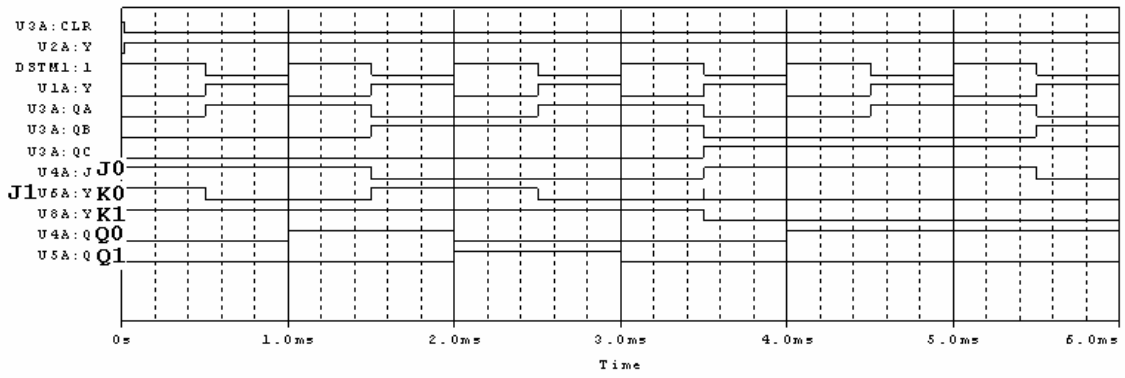
## 4) Sequential Logic (20 points)




In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for the propagation of the signals through the gates. (DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.)

a) The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the timer (U3A:QA, U3A:QB, and U3A:QC); the output from the combinational logic (U7A:Y, U6A:Y, and U8A:Y); and the output from the flip flops (U4A:Q and U5A:Q). (2 points per trace = 16 points)




b) If the output of the output of the two flip flops (U5A:Q U4A:Q) represents a two-digit binary number (b1 b0), what decimal number does it represents at time t=6ms? (4 pts)

*01 This is decimal number **1***