

**ENGR4300**  
**Spring 2006**  
**Test 3A**

Name \_\_\_\_\_ **Soln.** \_\_\_\_\_

Section \_\_\_\_\_ **Soln.** \_\_\_\_\_

Question 1 (20 points) \_\_\_\_\_

Question 2 (20 points) \_\_\_\_\_

Question 3 (20 points) \_\_\_\_\_

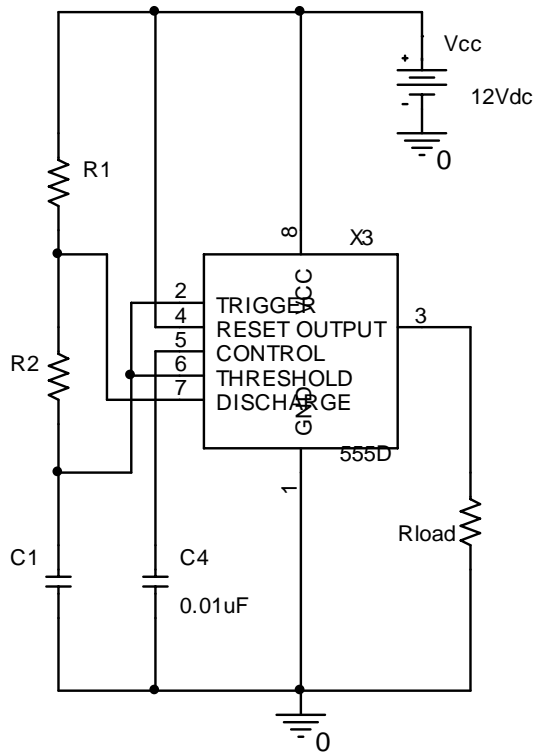
Question 4 (20 points) \_\_\_\_\_

Question 5 (20 points) \_\_\_\_\_

Total (100 points): \_\_\_\_\_

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question 1 – Astable Multivibrator (20 points)



The circuit shown above is used for parts a), b) and c). The 555 timer circuit shown is found to have an output frequency of 5kHz and a duty cycle of 60%.

a) What is the period of the output pulse? Include units. (1pt)

$$T = \frac{1}{f} = 0.2\text{msec}$$

b) What is the discharge time (or off time) of the timer? Include units (2pts)

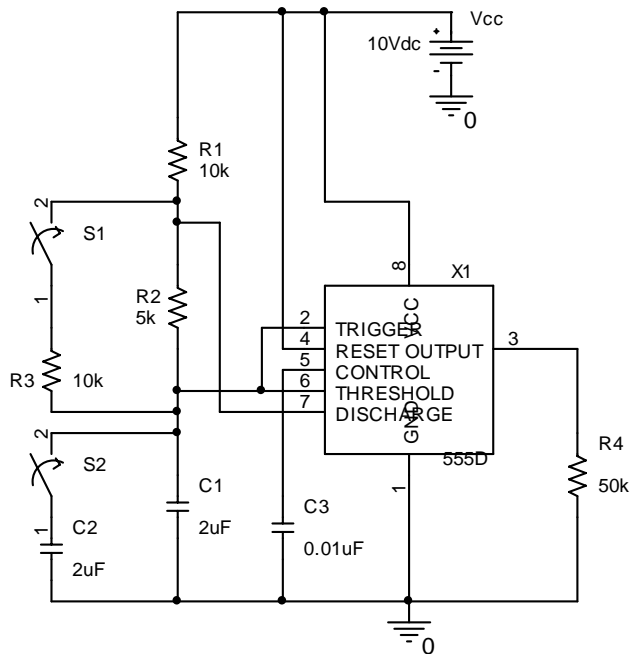
$$\frac{T_{on}}{T} = 0.6 \quad \frac{T_{off}}{T} = 0.4 \quad T_{off} = 0.4 \times 0.2 = 0.08\text{msec}$$

c) If  $C1=0.03\mu\text{F}$ , determine both R1 and R2. Include units. (6pts)

$$R1 = \underline{\hspace{2cm}} \quad T_{off} = 0.693 \times R2 \times C1 \quad R2 = \frac{0.08 \times 10^{-3}}{0.693 \times 3 \times 10^{-8}} = 3.8\text{k}\Omega$$

$$R2 = \underline{\hspace{2cm}} \quad T_{on} = 0.693 \times (R1 + R2) \times C1 \quad R1 = \frac{T_{on} - 0.693 \times R2 \times C1}{0.693 \times C1} = 1.9\text{k}\Omega$$

Question 1 – Astable Multivibrator (continued)



d) Using the circuit above, determine the output period and the off time with both switches open. Include units.(3pts)

Period = \_\_\_\_\_  $T = 0.693 \times (R1 + 2 \times R2) \times C1 = 28msec$

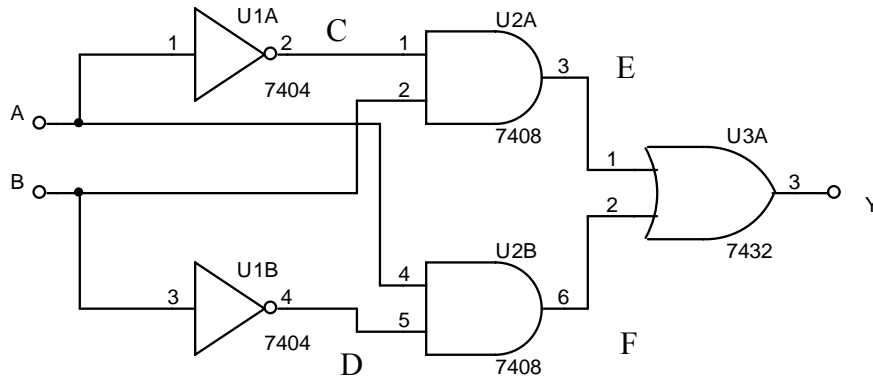
$T_{off} = 0.693 \times R2 \times C1 = 6.9ms$

Off Time (or discharge time) = \_\_\_\_\_

e) Answer the following using the circuit above. Circle the symbol that most correctly describes the statement that follows: T – true, F- false, I – insufficient information to determine. (2pts each)

- T  F  I The on time (or charge time) will decrease if S1, and only S1 is closed.
- T  F  I The frequency will be higher if S1 and only S1 is closed.
- T  F  I The off time (or discharge time) will increase if S1 and only S1 is closed.
- T  F  I The off time (or discharge time) will increase if S2 and only S2 is closed.

Question 2 – Combinational Logic Circuits (20 points)



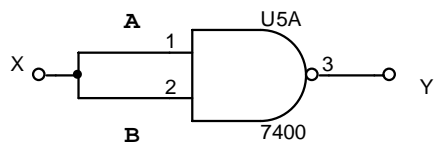
a) Complete the tabel for below for the circuit above. (12pts)

A	B	C	D	E	F	Y
0	0	1	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	1	1
1	1	0	0	0	0	0

b) What type of gate is this, if any ? (circle one) (1 pt)

AND    NAND    OR    NOR    **XOR**    NOT    None of the others.

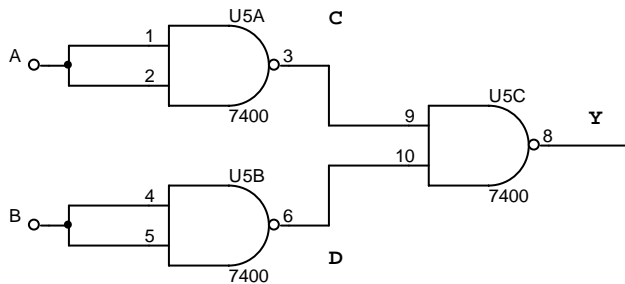
Question 2 – Combinational Logic Circuits (continued)



X	A	B	Y
0	0	0	1
1	1	1	0

c) Complete the truth table above to prove that a 2 input NAND gate can be used as an inverter by connecting both inputs together. (1pts)

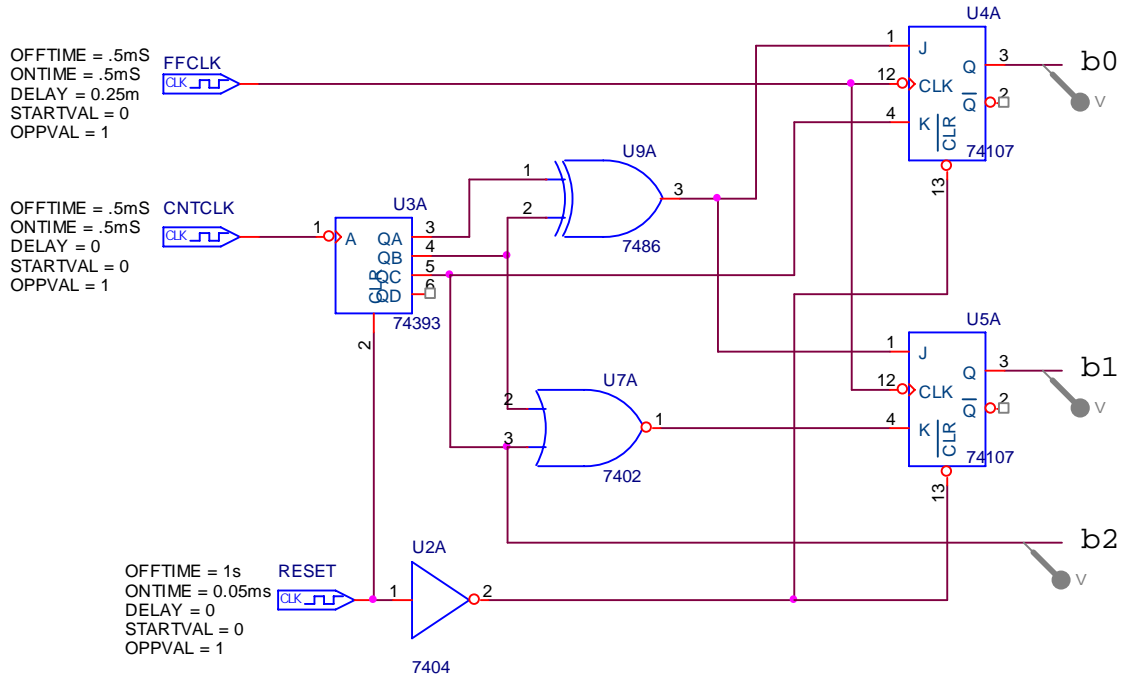
d) You need a 2 input OR gate, but all you have is left over NAND gates. Draw a circuit that uses only NAND gates but does the function of a 2 input OR gate. Create and complete a truth table that confirms your result. (Note : There is more than one solution, but it can be done using 3 gates.) (6 pts)



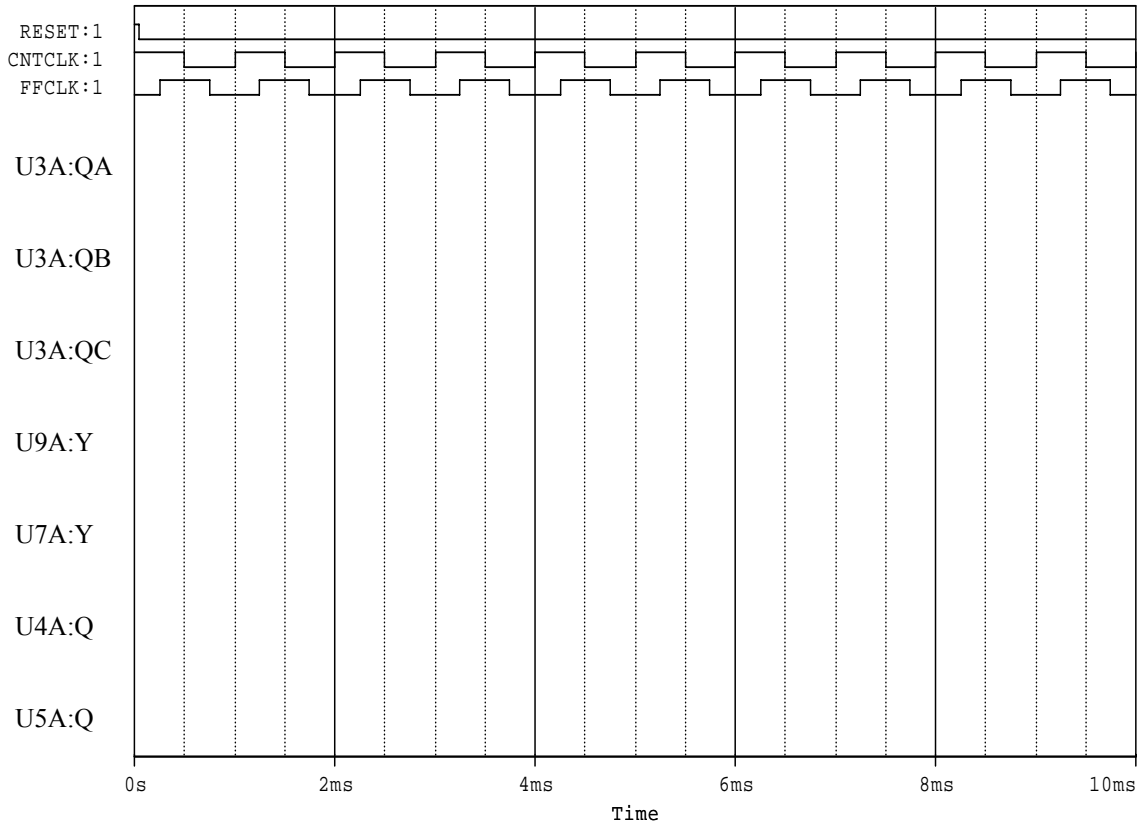
A	B	C	D	Y	A+B
0	0	1	1	0	0
0	1	1	0	1	1
1	0	0	1	1	1
1	1	0	0	1	1

Question 3 – Sequential Logic Circuits (20 points)

In the circuit below, the RESET clock provides an initial reset pulse to the counter and the two flip flops. The counter and flip flops all trigger on the falling edge of the clock.



a) Fill in the timing diagram with the signals indicated. (2 points each)



b) If b0, b1 and b2 represent bits in a binary number where b0 is the lowest order bit and b2 is the highest order bit, what is the value of the number at 6ms?

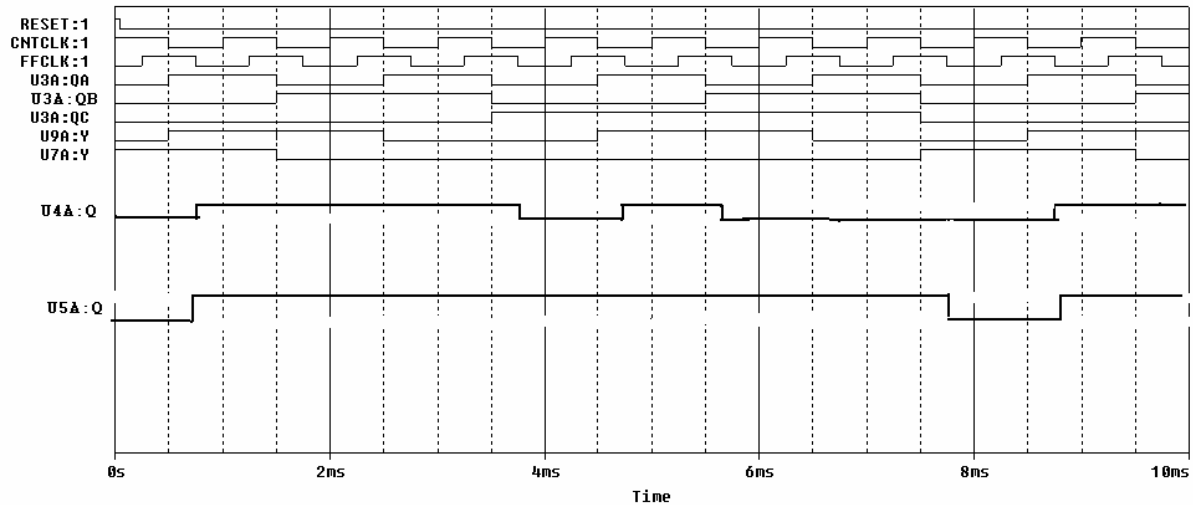
Binary Value (2 pts) :

Decimal Value (2 pts) :

c) What is the most important feature that differentiates sequential logic devices from combinational logic gates? (2 pts)

Answers to Quiz A, problem 3

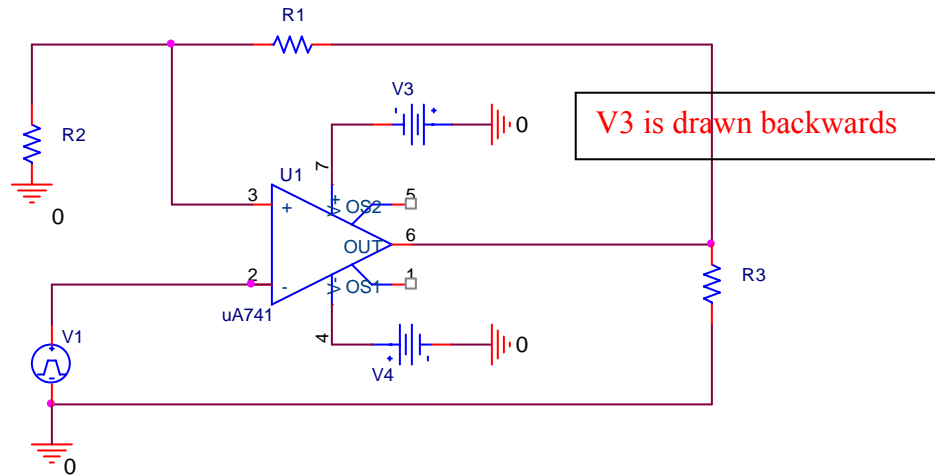
a) see below



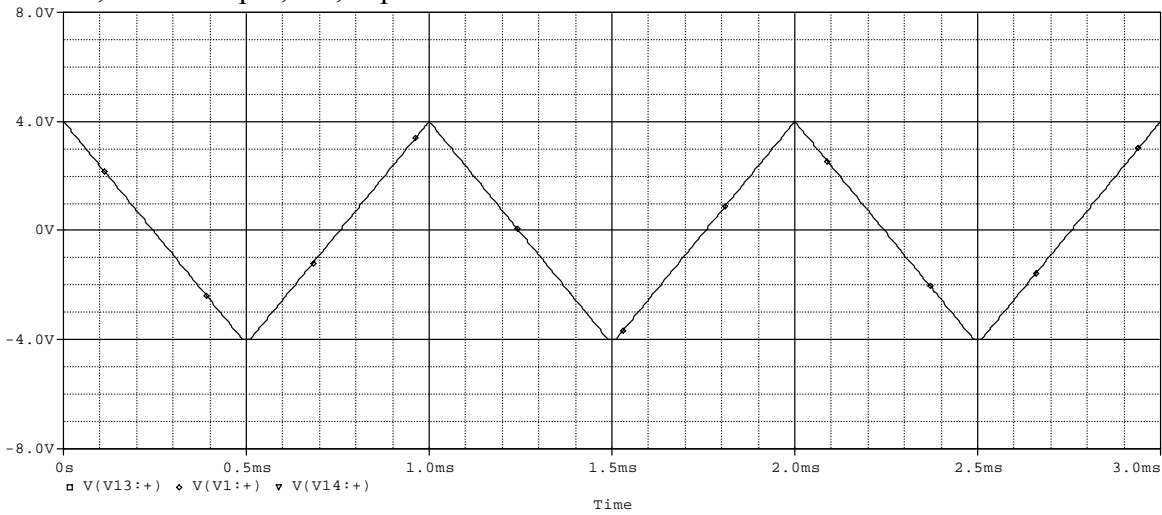
b) b0=U4A :Y=0 b1=U4a :Y=1 b2=U3A:QC=1 Binary = 110 Decimal = 6

c) Sequential logic devices have a clock that controls the timing, whereas combinational logic gates do not.

Question 4 – Comparators and Schmitt Triggers (20 points)

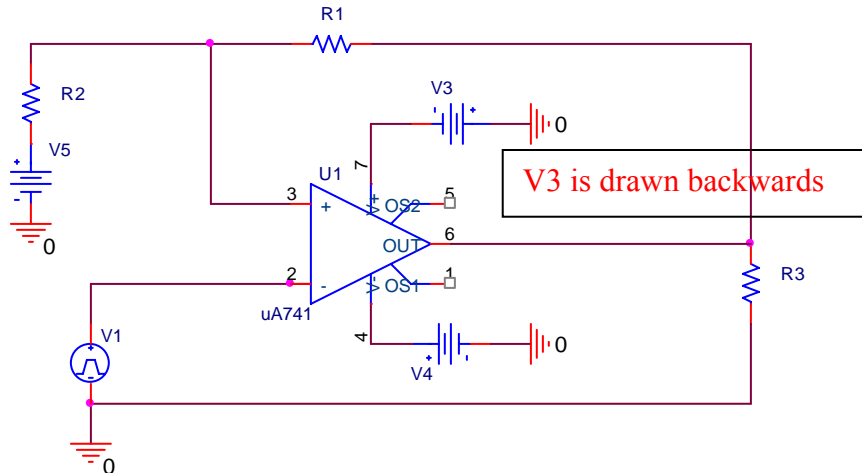


Part A: In the Schmitt trigger pictured above,  $R1 = 8k\Omega$ ,  $R2 = 1k\Omega$ ,  $R3 = 1k\Omega$ ,  $V3 = +6V$ ,  $V4 = -7V$ , and the input,  $V1$ , is pictured below.

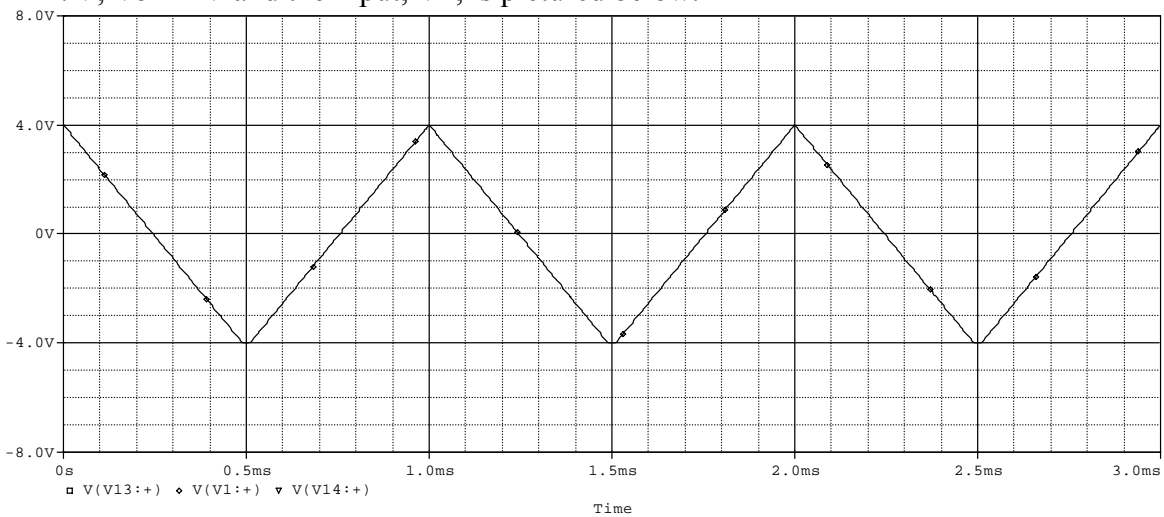


- a) What is the upper threshold for this Schmitt trigger? (3 pts)
  
- b) What is the lower threshold for this Schmitt trigger? (3 pts)
  
- c) What is the hysteresis for this Schmitt trigger? (1 pt)
  
- d) Given the input shown on the plot above, sketch the output of the Schmitt trigger at pin 6 of the op-amp. (3 pts)





Part B: In the Schmitt trigger pictured above,  $R1 = 8k\Omega$ ,  $R2 = 1k\Omega$ ,  $R3 = 1k\Omega$ ,  $V3 = +6V$ ,  $V4 = -7V$ ,  $V5 = 2V$  and the input,  $V1$ , is pictured below.

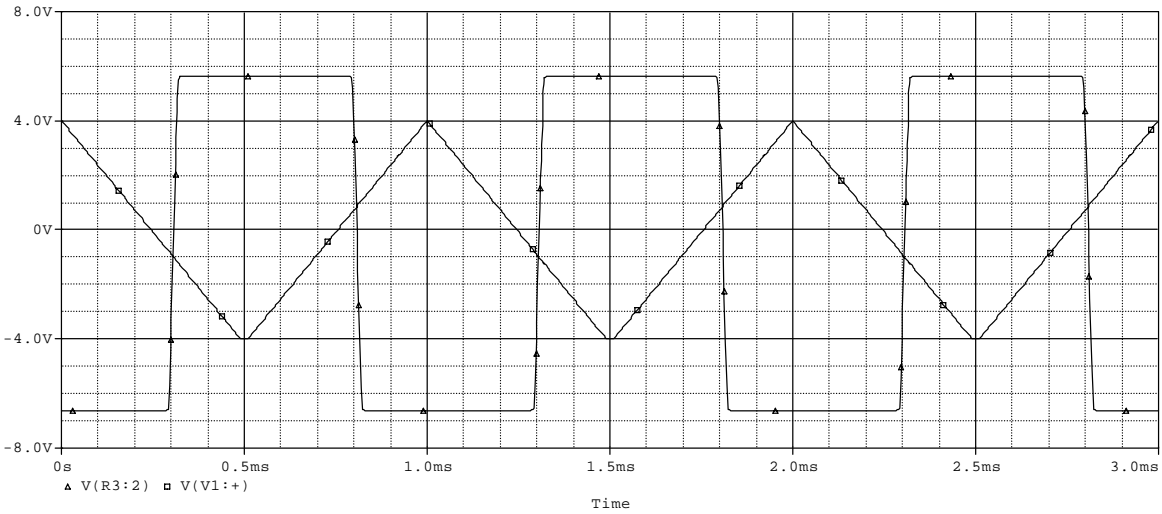


- What is the upper threshold for this Schmitt trigger? (3 pts)
- What is the lower threshold for this Schmitt trigger? (3 pts)
- What is the hysteresis for this Schmitt trigger? (1 pt)
- Given the input shown on the plot above, sketch the output of the Schmitt trigger at pin 6 of the op-amp. (3 pts)

**Answers to quiz A: Problem 4**

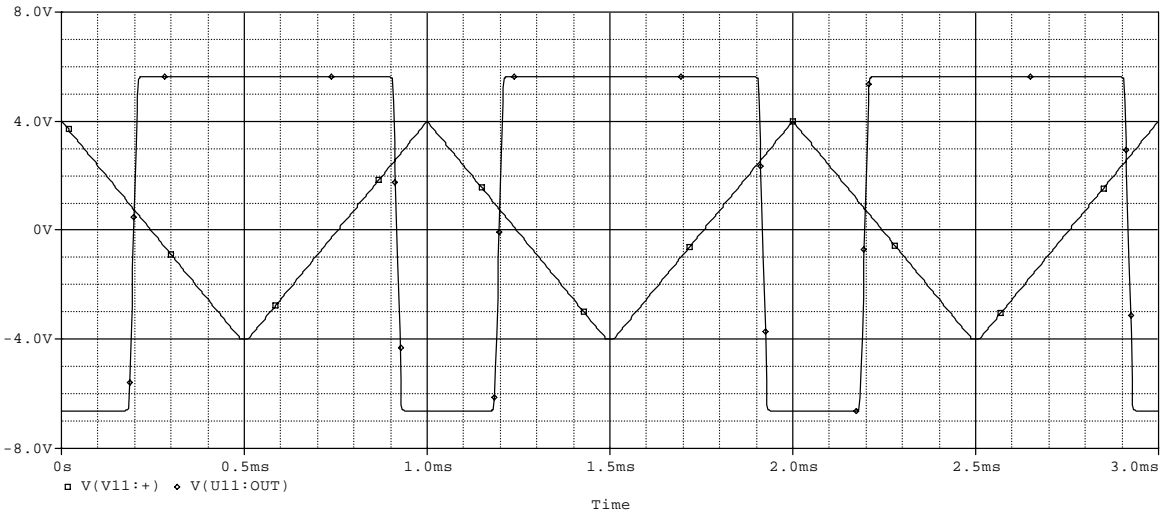
Part A:  $R1 = 8k\Omega$ ,  $R2 = 1k\Omega$ ,  $R3 = 1k\Omega$ ,  $V3 = +6V$ ,  $V4 = -7V$

- a)  $T_{upper} = (6)(1k)/(1k+8k) = 0.67V$
- b)  $T_{lower} = (-7)(1k)/(1k+8k) = -0.78V$
- c)  $Hysteresis = 0.667 - (-.778) = 1.45V$
- d) See below – Students can use vertical lines for transitions and saturate completely to +6 and -7V.

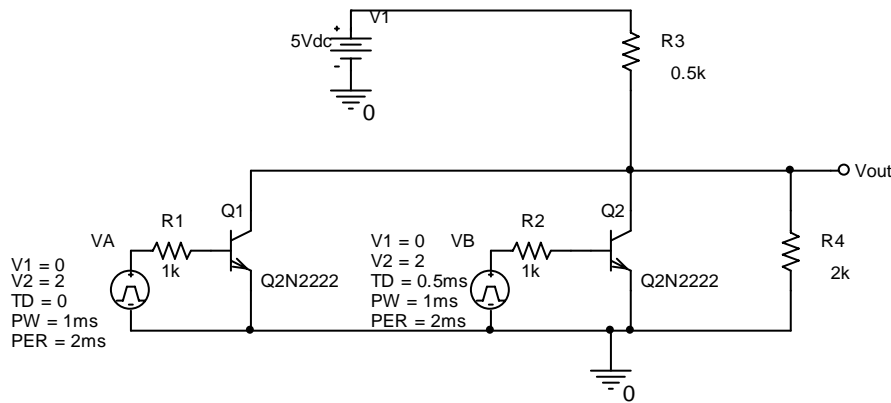


Part B:  $V5 = 2V$

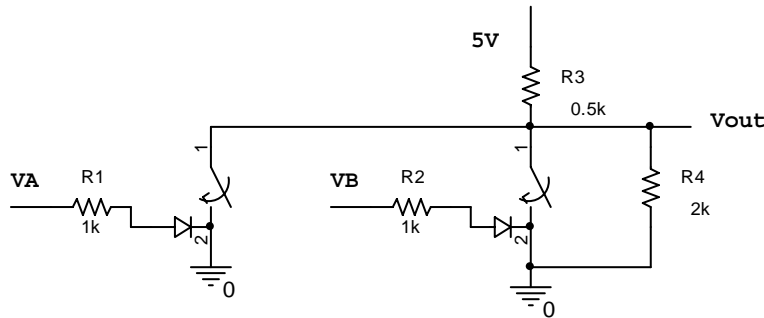
- a)  $T_{upper} = [(6-2)(1k)/(1k+8k)] + 2 = 2.44V$
- b)  $T_{lower} = [(-7-2)(1k)/(1k+8k)] + 2V = 1V$
- c)  $Hysteresis = 2.44 - 1 = 1.44V$
- d) See below – Students can use vertical lines for transitions and saturate completely to +6 and -7V



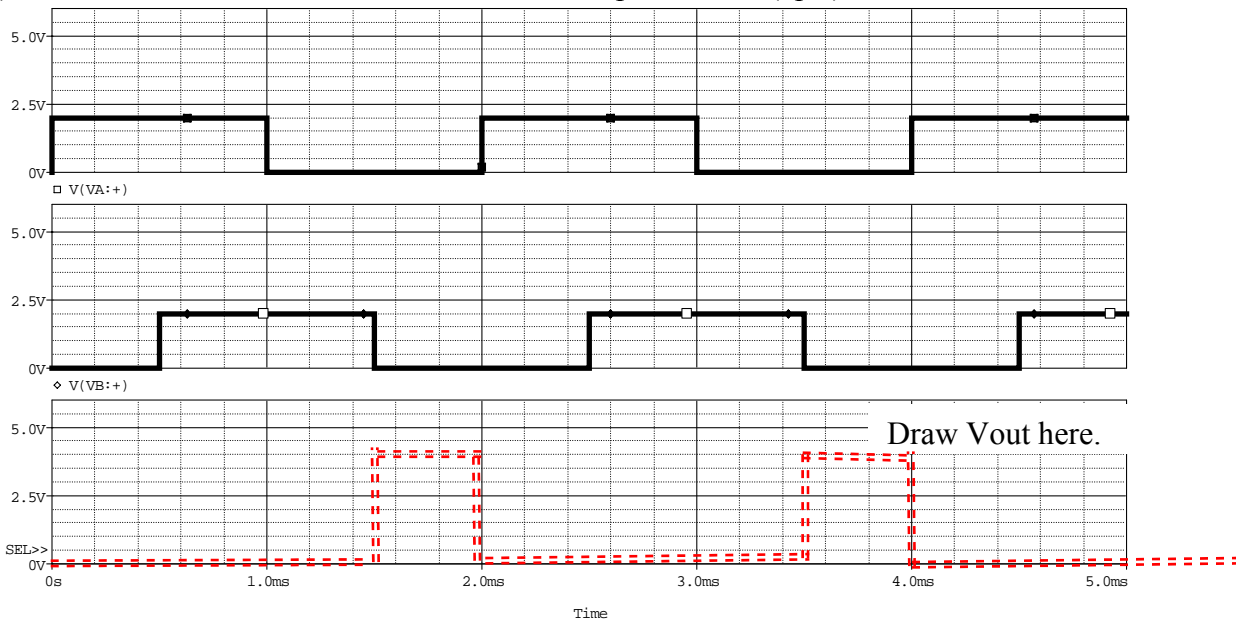
Question 5 – Switching Circuits (20 points)



a) Redraw this circuit using the diode switch model for both Q1 and Q2. (3pts)



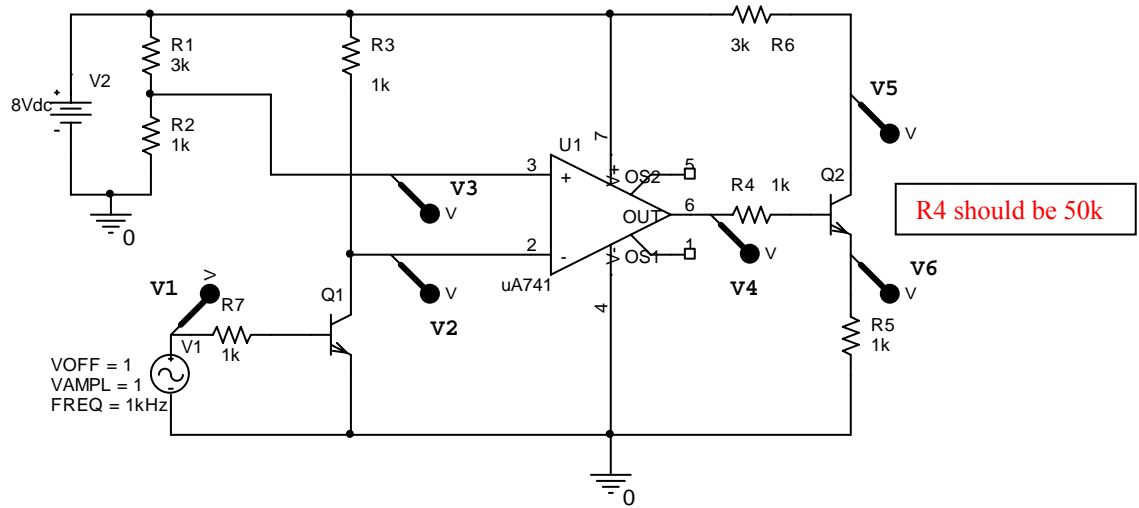
b) Draw the trace of Vout vs. time on the bottom plot below. (5pts)



c) If VA and VB are considered to be logic inputs, and Vout is a logic gate output, then what type of gate is this? (circle one) (2pts)

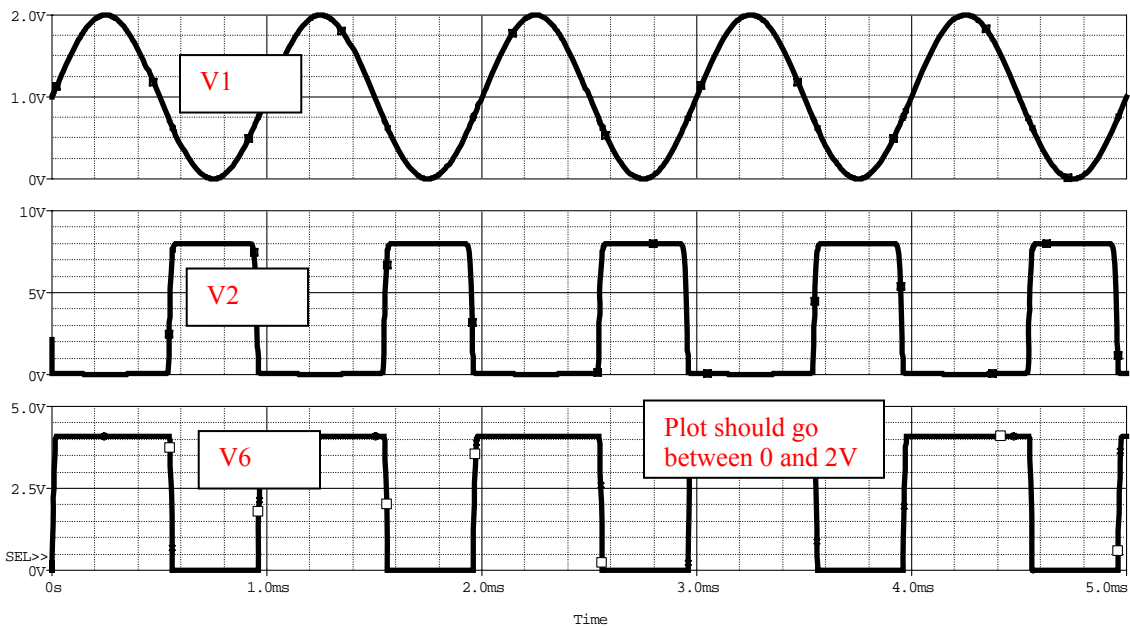
- AND    NAND    NOT    OR    **NOR**    XOR    none of these

Question 5 – Switching Circuits (continued)

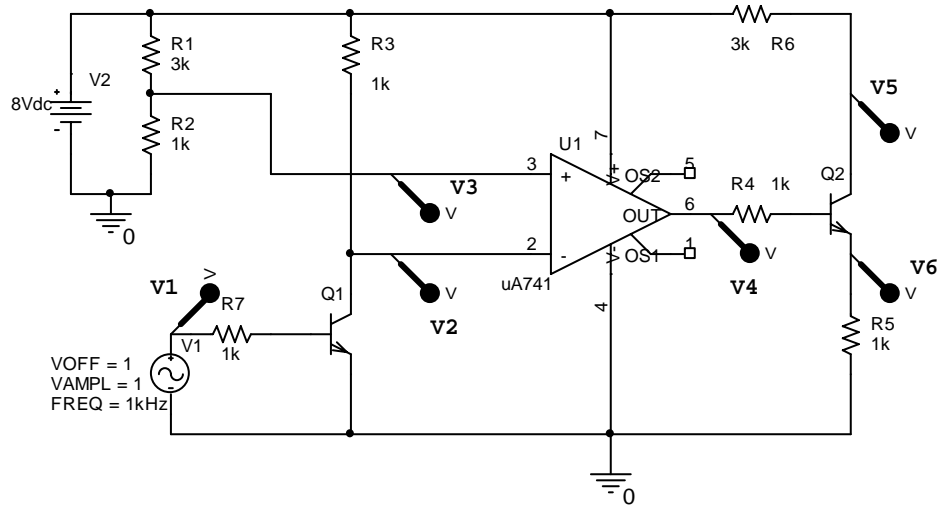


R4 should be 50k

d) For the circuit above, identify which markers correspond to the waveforms shown. (5pts)



**ERRORS on exam – R4 should be 50k, not 1k. Waveform on bottom plot should transition between 0 and 2V, not 0 and 4V.**



e) Complete the following table for the circuit shown above. Assume the devices are ideal. (5pts)

V1	V2	V3	V4	V5	V6
0V	8V	2V	0V	8V	0V
2V	0V	2V	8V	2V	2V