ENGR4300
Spring 2006
Test 3B

Name_____solution_____

Section_____

Question 1 (20 points)_____

Question 2 (20 points) _____

Question 3 (20 points)_____

Question 4 (20 points)_____

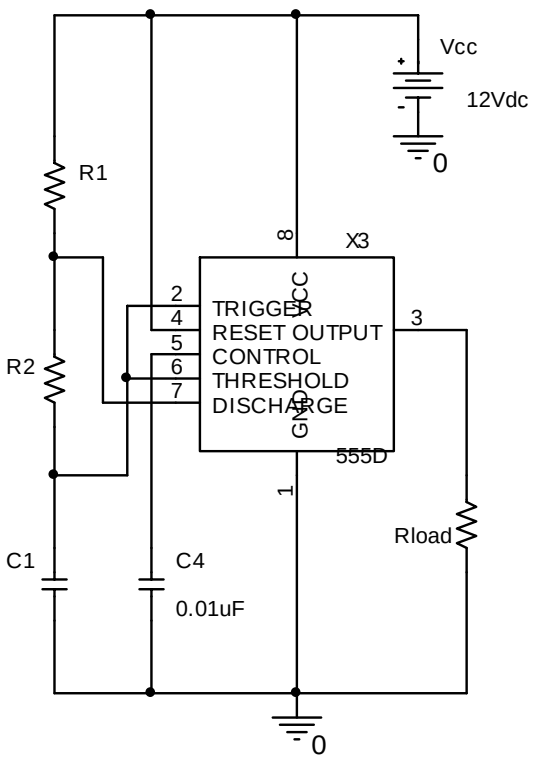
Question 5 (20 points)_____

Total (100 points): _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question 1 – Astable Multivibrator (20 points)

The circuit shown to the left is used for parts a), b) and c). The 555 timer circuit shown is found to have an output frequency of 25kHz and a duty cycle of 75%.



a) What is the period of the output pulse? Include units. (1pt)

T = 1/f = 1/(25k) = .04ms

T = 0.04ms

b) What is the discharge time (or off time) of the timer? Include units (2pts)

D = Ton/T .75 = Ton/0.04m Ton = .03ms
Toff = T-Ton = .04 -.03 = .01ms

Toff = 0.01ms

c) If R2=2kΩ, determine both R1 and C1. Include units. (6pts)

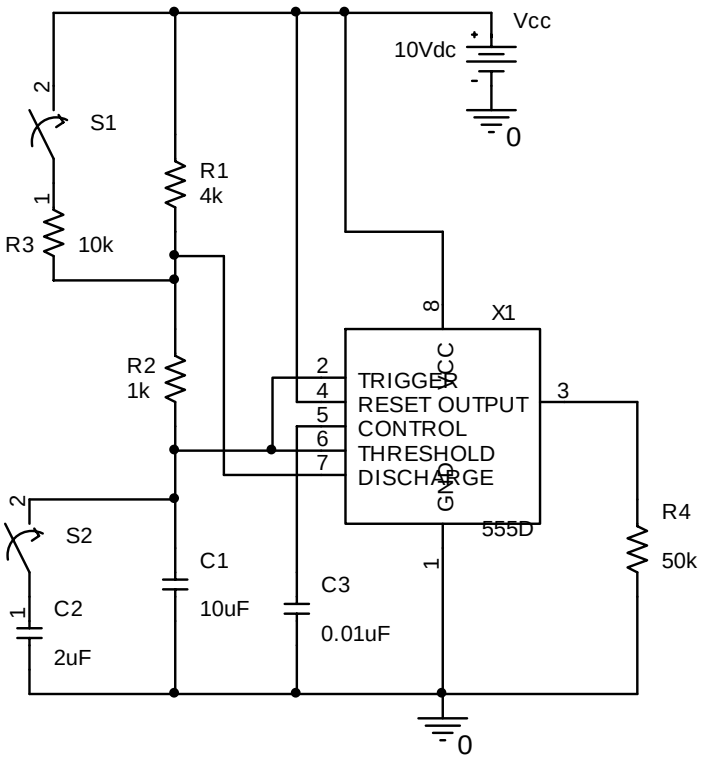
Toff = .693(R2)(C1) 0.01m = .693(2k)(C1) C1 = .0072μF

Ton = .693(R1+R2)(C1) 0.03m = .693(2k+R2)(.0072μ) R2 = 4k Ω

R1 = 4k Ω

C1= 0.0072μF

Question 1 – Astable Multivibrator (continued)



The circuit shown to the left is used for parts d) and e).

d) Determine the output frequency with both switches open. Include units.(2pt)

T = .693(R1+2R2)C1
T = .693(4k+2(1k))(10μ)
T = 41.6 ms

f=1/T =1/41.6m=0.024k Hz

f = 24Hz

d) Determine the on-time with both switches open. Include units.(1pt)

Ton = .693(R1+R2)(C1) = .693(4k+1k)(10μ) = 34.65ms

On Time = 34.65 ms

e) Answer the following using the circuit above. Circle the symbol that most correctly describes the statement that follows: T – true, F- false, I – insufficient information to determine. (2pts each)

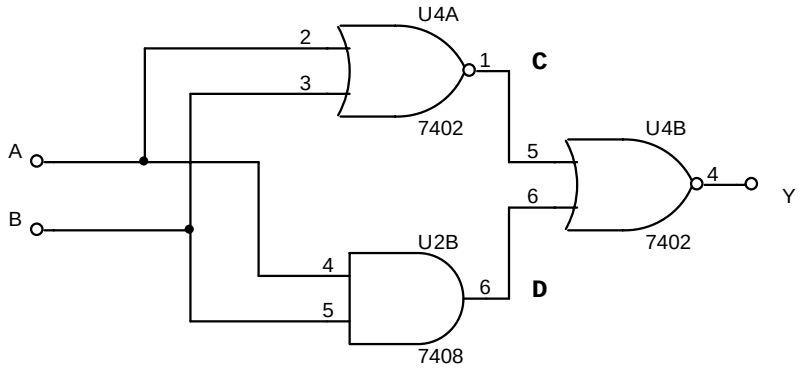
T ***F*** I The on time (or charge time) will increase if S1, and only S1 is closed.

T F I The frequency will be higher if S1 and only S1 is closed.

T ***F*** I The off time (or discharge time) will increase if S1 and only S1 is closed.

T F I The off time (or discharge time) will increase if S2 and only S2 is closed.

Question 2 – Combinational Logic Circuits (20 points)



a) Complete the table below for the circuit above. (6 pts)

A	B	C	D	Y
0	**0**	***1***	***0***	***0***
0	**1**	***0***	***0***	***1***
1	**0**	***0***	***0***	***1***
1	**1**	***0***	***1***	***0***

b) What type of gate is this, if any ? (circle one) (1 pt)

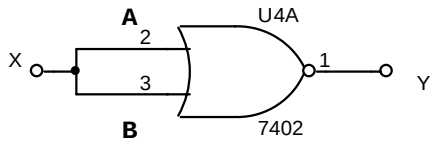
AND NAND OR NOR ***XOR*** NOT None of the others.

c) Use a truth table proof to prove the following relationship : (6 pts)

$$A \oplus B = \overline{A} \bullet B + A \bullet \overline{B}$$

A	B	$\overline{A}$	$\overline{B}$	$\overline{A} \bullet B$	$A \bullet \overline{B}$	$\overline{A} \bullet B + A \bullet \overline{B}$	$A \oplus B$
0	0	***1***	***1***	***0***	***0***	***0***	***0***
0	1	***1***	***0***	***1***	***0***	***1***	***1***
1	0	***0***	***1***	***0***	***1***	***1***	***1***
1	1	***0***	***0***	***0***	***0***	***0***	***0***

Question 2 – Combinational Logic Circuits (continued)



X	A	B	Y
0	*0*	*0*	*1*
1	*1*	*1*	*0*

d) Complete the truth table above to prove that a 2 input NOR gate can be used as an inverter by connecting both inputs together. (2 pts)

Grading note : Please note that question in not worth the same number of points in this test as it is in test A.

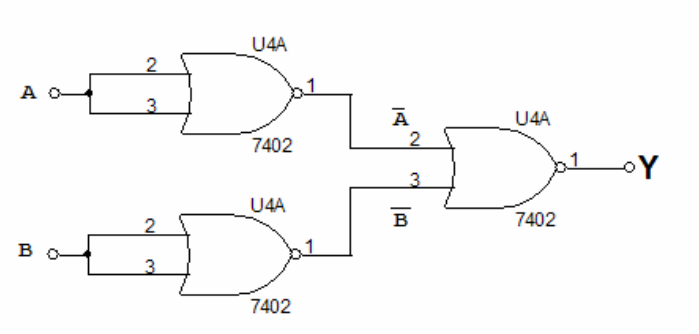
e) You need a 2 input AND gate, but all you have is left over NOR gates. Draw a circuit that uses only NOR gates but does the function of a 2 input AND gate. (Note : There is more than one solution, but it can be done using 3 gates.) [Hint : The relationship you proved in part d and DeMorgan's Laws may be helpful.] (5 pts)

Grading notes : GIVE PARTIAL CREDIT
This question is not worth the same number of points as in Test A.
This version does not require a truth table, only a circuit.

Starting with one of DeMorgan's Laws, we can negate both sides and derive a useful relationship for $A \bullet B$.

$$\overline{A \bullet B} = \overline{A} + \overline{B}$$
$$\overline{\overline{A \bullet B}} = \overline{\overline{A} + \overline{B}}$$
$$A \bullet B = \overline{\overline{A} + \overline{B}}$$

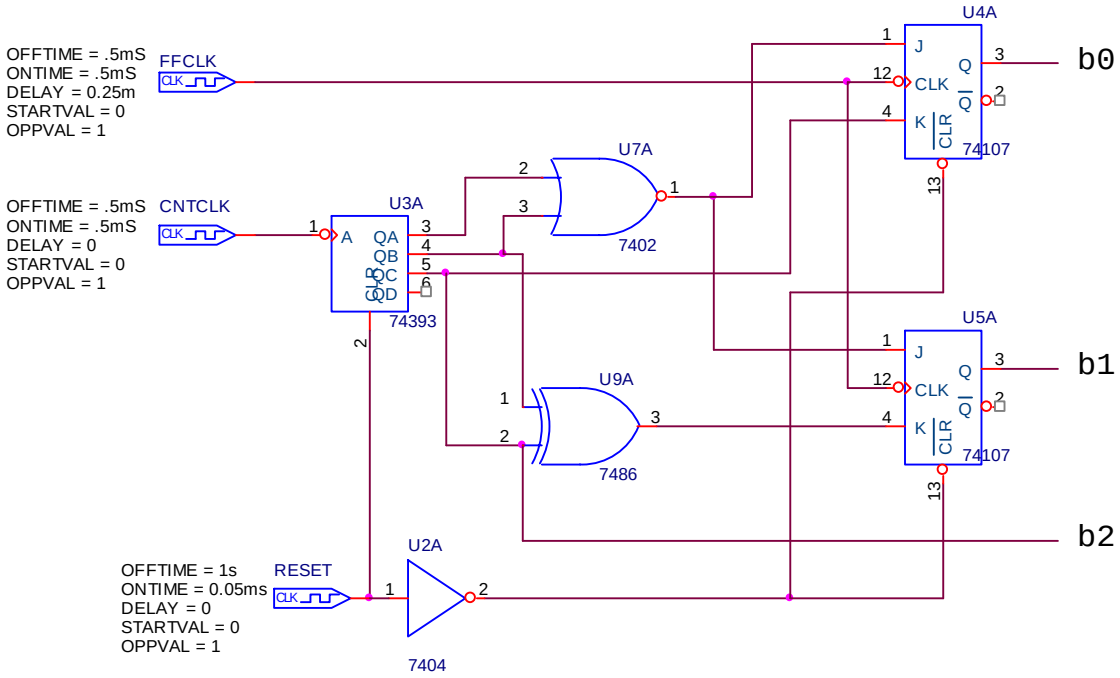
We can use the relationship from d to get ~A and ~B. Then we only need to send these into a NOR gate.



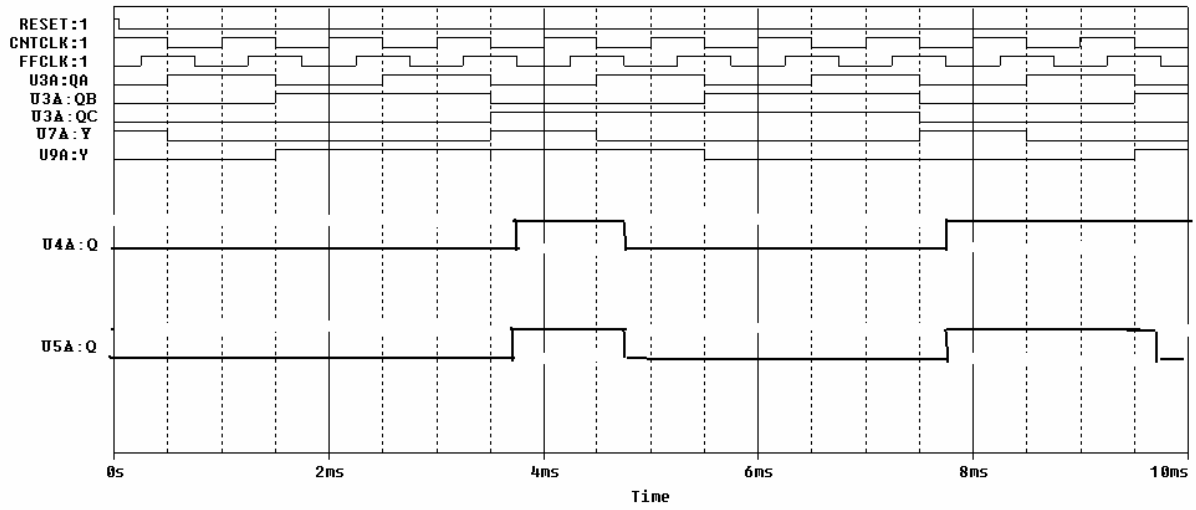
$$Y = \overline{\overline{A} + \overline{B}} = A \bullet B$$

Question 3 – Sequential Logic Circuits (20 points)

In the circuit below, the RESET clock provides an initial reset pulse to the counter and the two flip flops. The counter and flip flops all trigger on the falling edge of the clock.



a) Fill in the timing diagram with the signals indicated. (2 points each)



b) If b0, b1 and b2 represent bits in a binary number where b0 is the lowest order bit and b2 is the highest order bit, what is the value of the number at 8ms?

b0=U4A :Y= b1=U5A :Y=1 b2=U3A:QC=0 Binary = 011 Decimal = 3

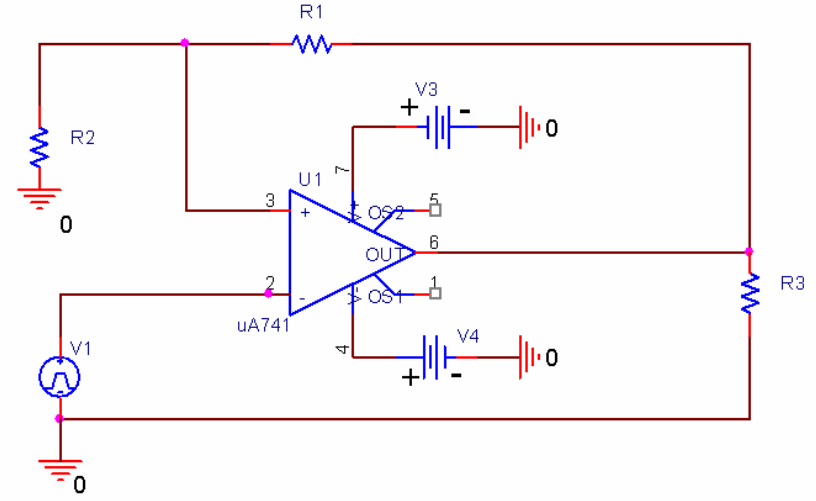
Binary Value (2 pts) : ***011***

Decimal Value (2 pts) : ***3***

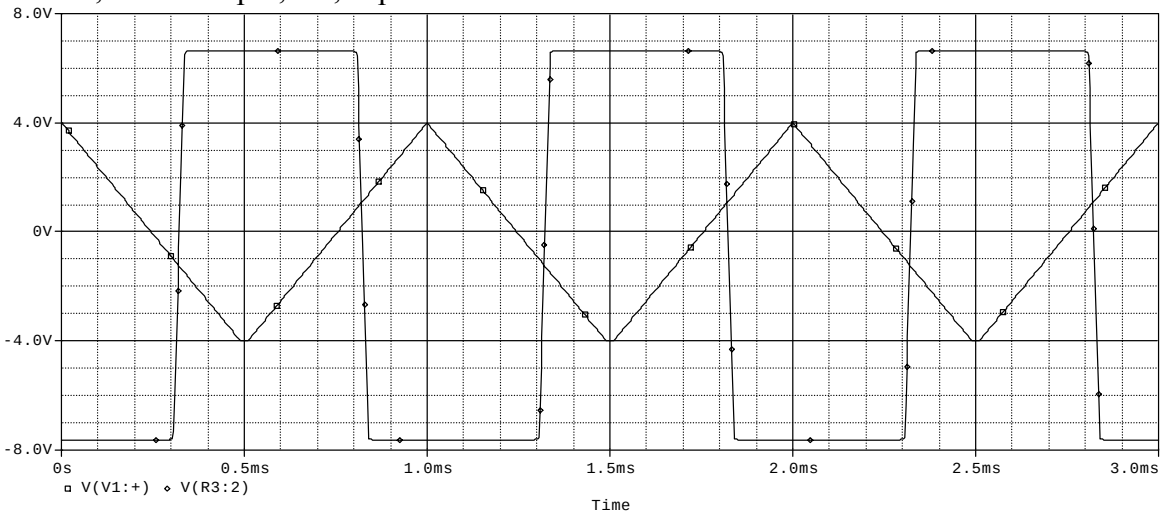
c) What is the most important feature that differentiates sequential logic devices from combinational logic gates? (2 pts)

Sequential logic devices have a clock that controls the timing, whereas combinational logic gates do not. The output of a combinational gate changes instantly when the input changes. The output of a sequential loic device changes on a rising or falling edge of the clock.

Question 4 – Comparators and Schmitt Triggers (20 points)



Part A: In the Schmitt trigger pictured above, R1 = 7kΩ, R2 = 1kΩ, R3 = 1kΩ, V3 = +7V, V4 = -8V, and the input, V1, is pictured below.



Students can use vertical lines for transitions and saturate completely to +7 and -8V

a) What is the upper threshold for this Schmitt trigger? (3 pts)

Tupper = (7)(1k)/(1k+7k) = 0.875V

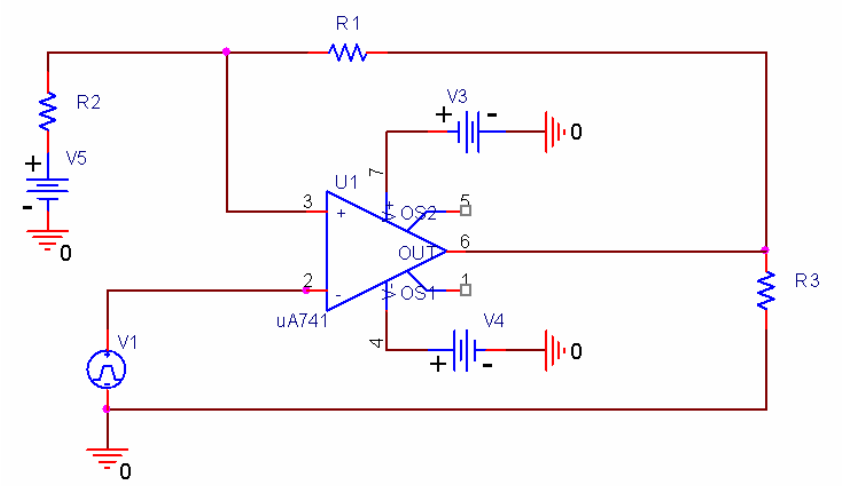
b) What is the lower threshold for this Schmitt trigger? (3 pts)

Tlower = (-8)(1k)/(1k+7k) = -1V

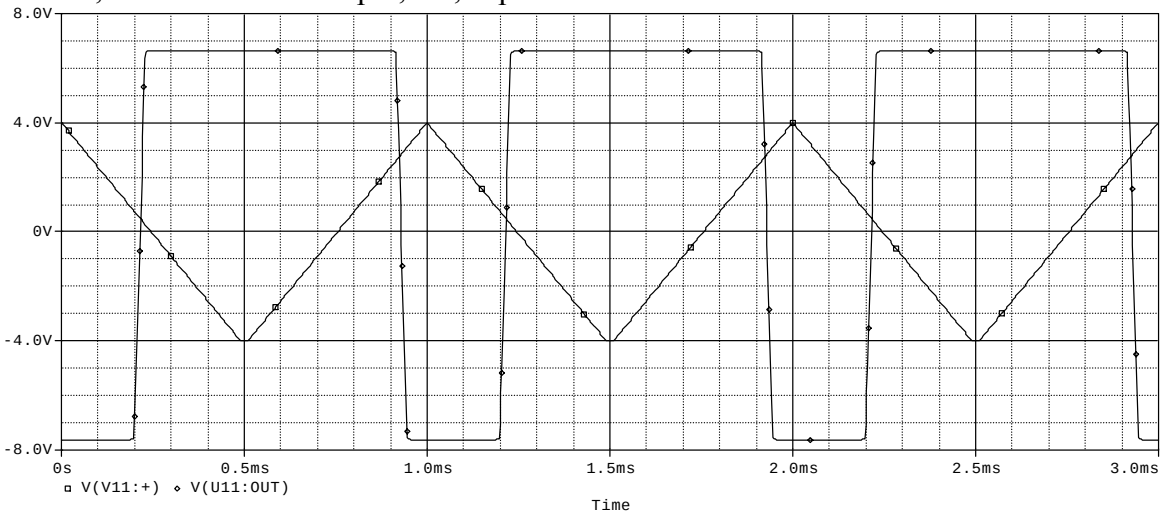
c) What is the hysteresis for this Schmitt trigger? (1 pt)

Hysteresis = 0.875-(-1) = 1.875V

d) Given the input shown on the plot above, sketch the output of the Schmitt trigger at pin 6 of the op-amp. (3 pts)



Part B: In the Schmitt trigger pictured above, R1 = 7kΩ, R2 = 1kΩ, R3 = 1kΩ, V3 = +7V, V4 = -8V, V5 = 2V and the input, V1, is pictured below.



Students can use vertical lines for transitions and saturate completely to +7 and -8V.

a) What is the upper threshold for this Schmitt trigger? (3 pts)

Tupper = [(7-2)(1k)/(1k+7k)] + 2 = 2.625V

b) What is the lower threshold for this Schmitt trigger? (3 pts)

Tlower = [(-8-2)(1k)/(1k+7k)] + 2V = 0.75V

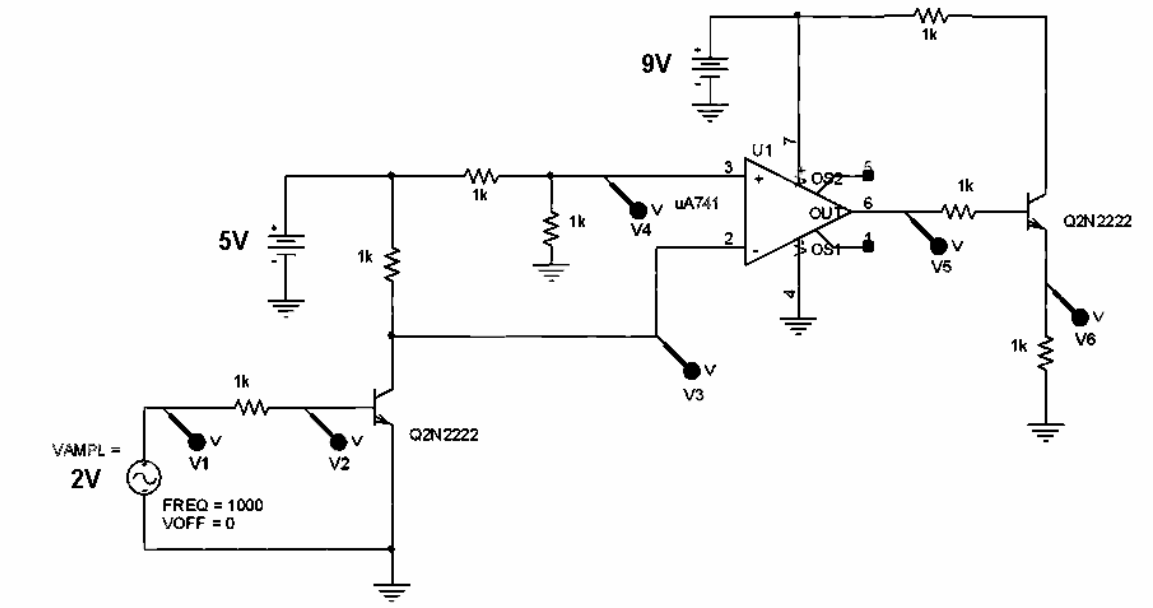
c) What is the hysteresis for this Schmitt trigger? (1 pt)

Hysteresis = 2.625-0.75 = 1.875V

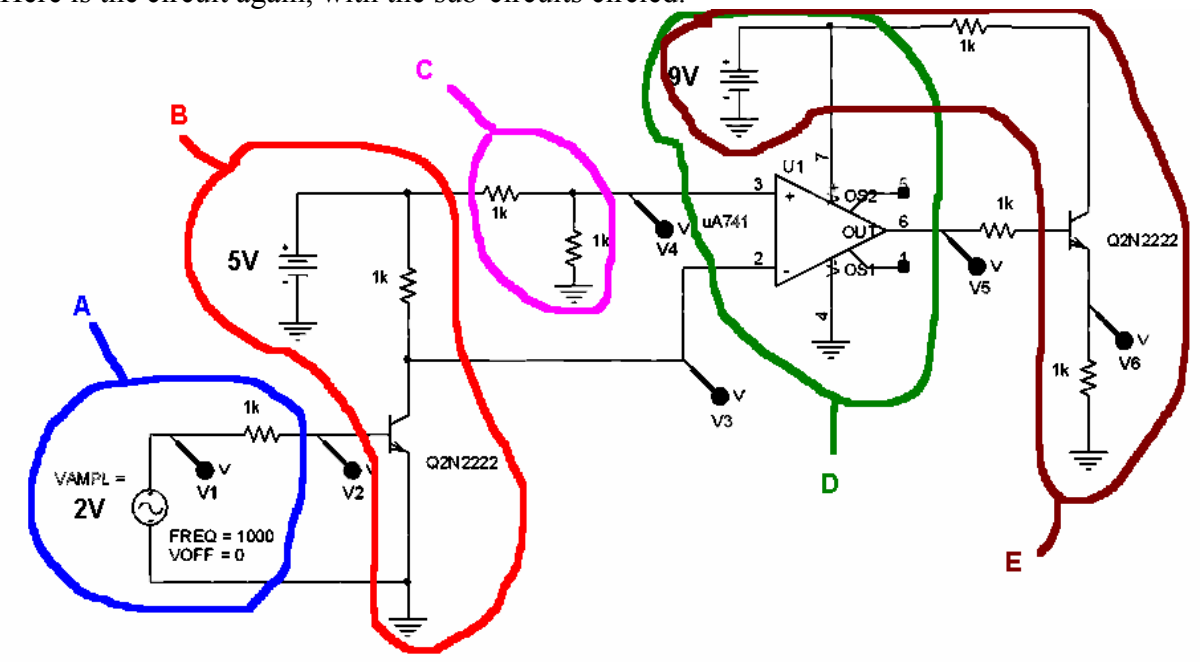
d) Given the input shown on the plot above, sketch the output of the Schmitt trigger at pin 6 of the op-amp. (3 pts)

Question 5 – Switching Circuits (20 points)

You are given the following switching circuit:



Here is the circuit again, with the sub-circuits circled.



a.) What type of circuit is circuit C and what is the voltage at V4? (2 pt)

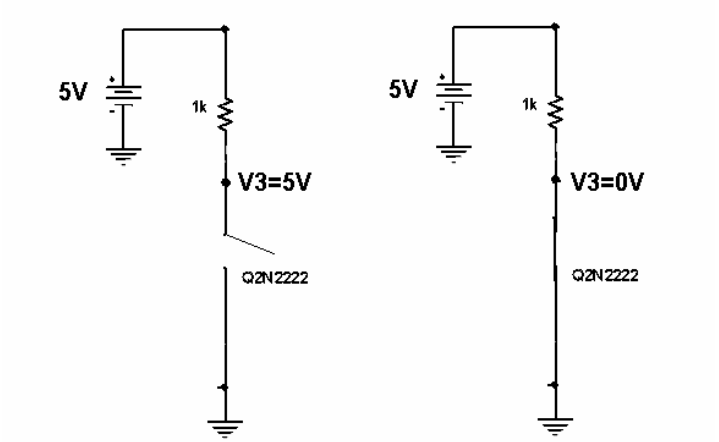
Voltage divider V4 = (5V)(1k)(1k+1k) = 2.5V

b.) What type of circuit is circuit D and what are the (theoretical) maximum and minimum voltages at V5? (3 pts)

Comparator (technically it is an inverting comparator) $V5_{max} = 9V$ $V5_{min} = 0V$

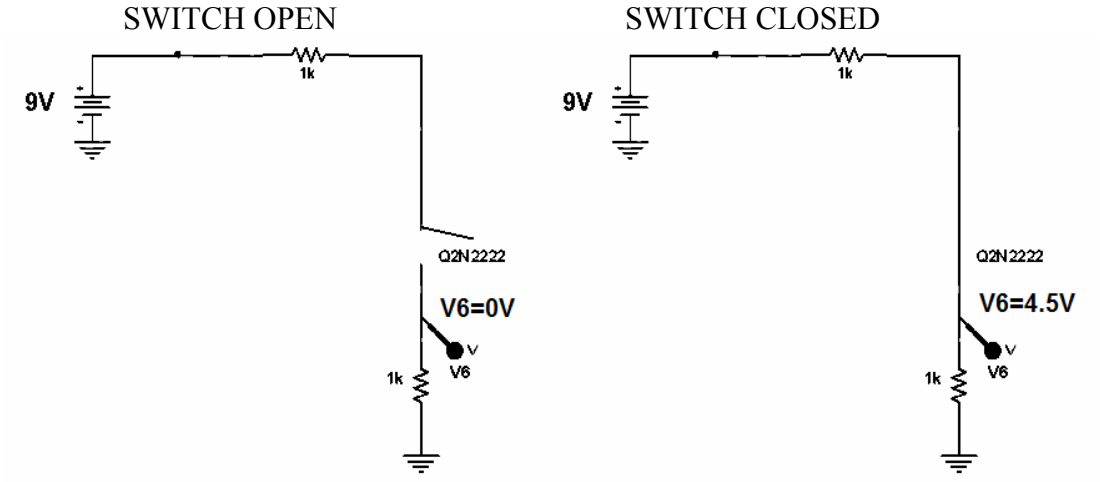
c.) Redraw sub-circuit B using the switch model of a transistor. That is, draw it twice -- once with the switch open and once with the switch closed. Indicate the voltage at V3 on both drawings. (3 pts)

SWITCH OPEN SWITCH CLOSED



d.) Redraw sub-circuit E using the switch model of a transistor. That is, draw it twice -- once with the switch open and once with the switch closed. Indicate the voltage at V6 on both drawings. (3 pts)

SWITCH OPEN SWITCH CLOSED



e.) What is the maximum voltage that can ever occur at the base of the transistor, V2? (1 pt)

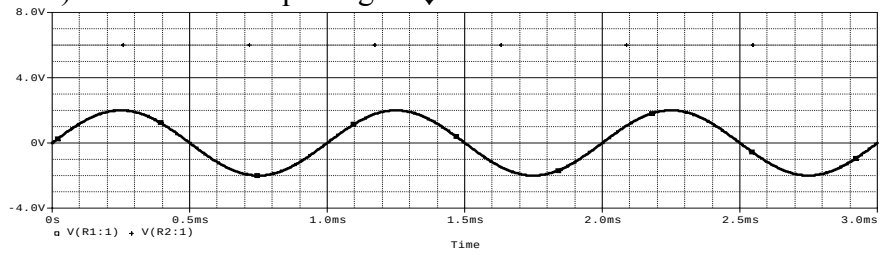
$V2_{max} = 0.7V$

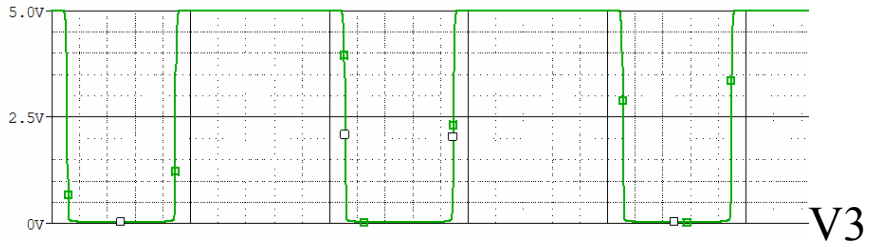
f) Use the information in parts a-e to fill in the following chart. (5 pts)

V1	V2	V3	V4	V5	V6
0v	***0V***	***5V***	***2.5V***	***0V***	***0V***
2v	***0.7V***	***0V***	***2.5V***	***9V***	***4.5V***

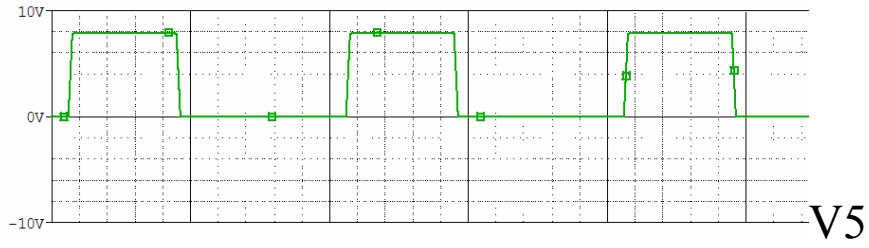
Grading note: If the values of the numbers are consistent with what they said in the previous parts, don't take off. We want to see if they know how the switching works in this part of the question.

g) Assuming that the signal pictured below represents the input at V1, identify which of the signals, V2, V3, V4, V5 and V6 the other plots below correspond to. (Not all signals are shown.) (1 pt each) Input Signal ↓

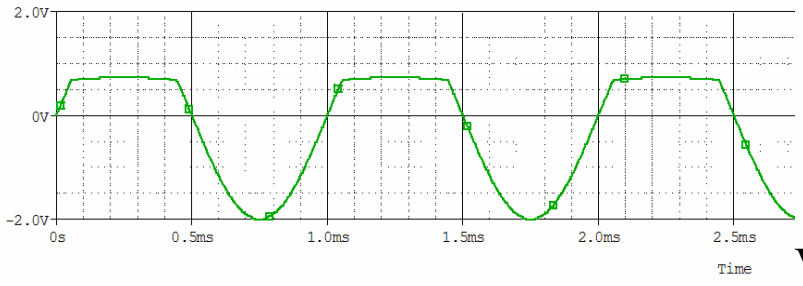




V3



V5



V2