ENGR-4300
Fall 2008
Test 3

Name _____

Section 1(MR 8:00) 2(TF 2:00)
(circle one)

Question I (20 points) _____

Question II (15 points) _____

Question III (20 points) _____

Question IV (20 points) _____

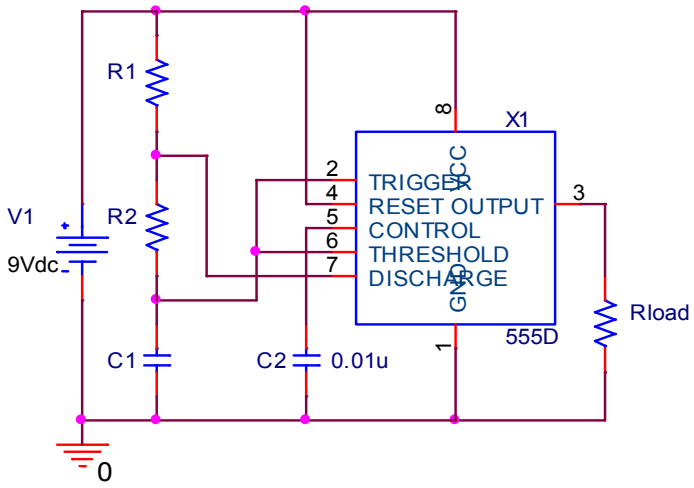
Question V (25 points) _____

Total (100 points): _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question I – Astable Multivibrator (20 points)

1. (4pt) The 555 timer circuit shown is to have a duty cycle of 66.67% (2/3). For a given C1, what ratio of resistors R1/R2 will produce this duty cycle



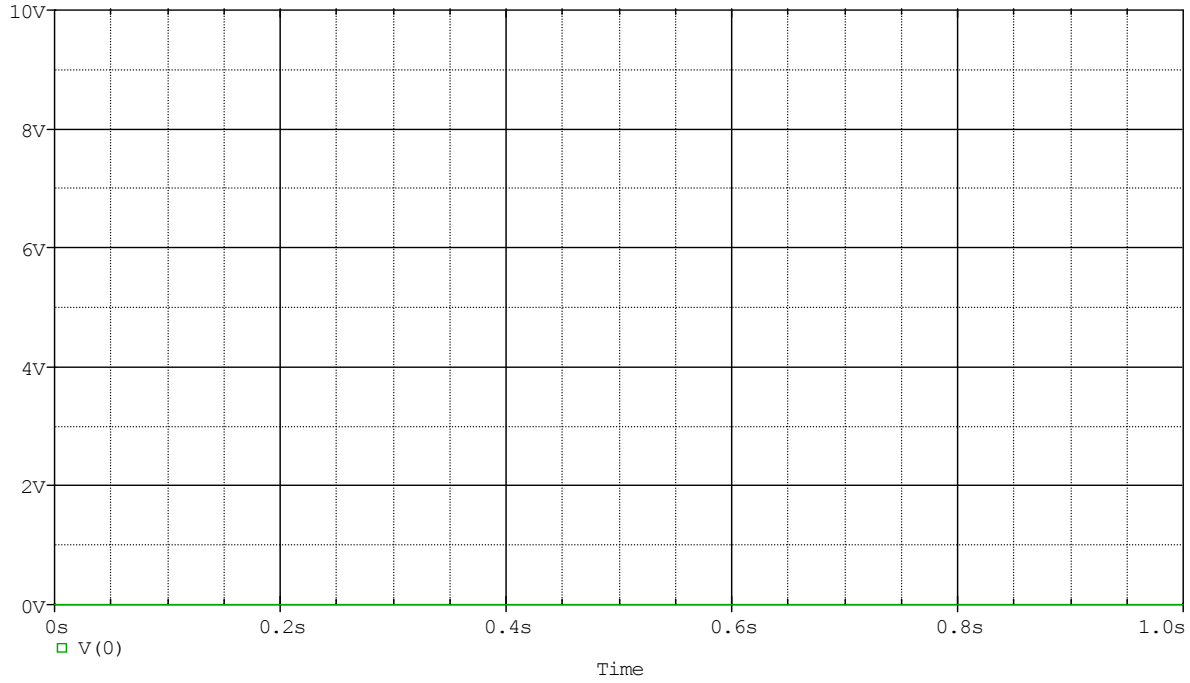
2. (4pt) Using a ratio of R1/R2 = 2 and with C1 = 50μF, calculate the values for R1 and R2 needed to yield a frequency of 5Hz.

3. (2pt) For an ideal 555, what are the maximum and minimum voltages on pin 2 above during normal operation?

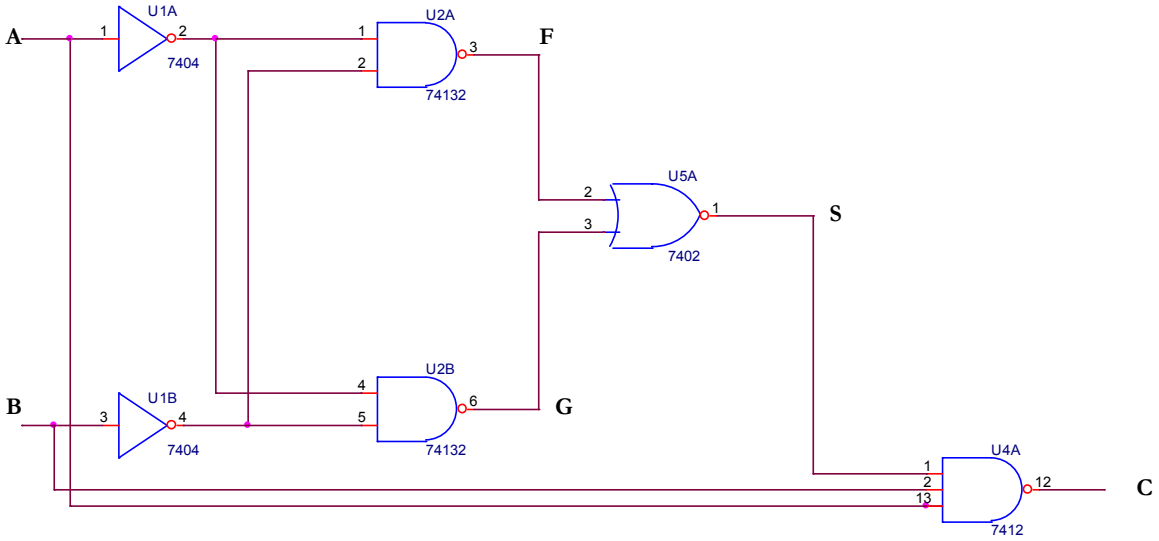
4. (4pt) For an ideal 555, what are the maximum and minimum voltages on pin 7 above during normal operation?

Question I – Astable Multivibrator (continued)

5. (6pt) Plot on the axes below the voltages on pins 2 and 7 of the circuit above and be sure to label each. HINT: you may want to find the Duty Cycle first.



Question II – Combinational Logic Circuits (15 points)



1. Complete the table below for the circuit above (***4 pts***: all or nothing, continuation of mistakes will be deducted)

A	B	F	G	S	C
0	0				
0	1				
1	0				
1	1				

2. A logic circuit (NOT the same as above) has the following truth table. Combining bits RST as a 3-bit binary number, fill in the decimal value in the table (***4 pts***)

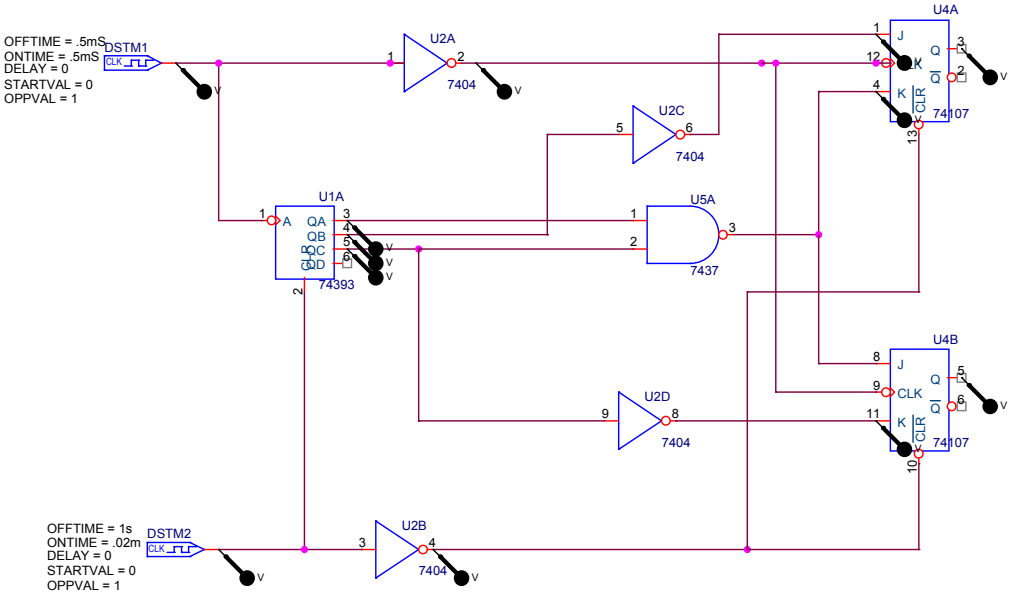
A	B	C	R	S	T	RST as a Decimal Number
0	0	1	0	0	1	
0	1	1	0	1	0	
1	0	1	0	1	0	
1	1	1	0	1	1	

Question II – Combinational Logic Circuits (continued)

3. If A, B, and C are treated as 1-bit binary number inputs, what ARITHMATIC operation is being performed in creating the output RST? (***4 pts***: continuation of mistake above will be deducted)

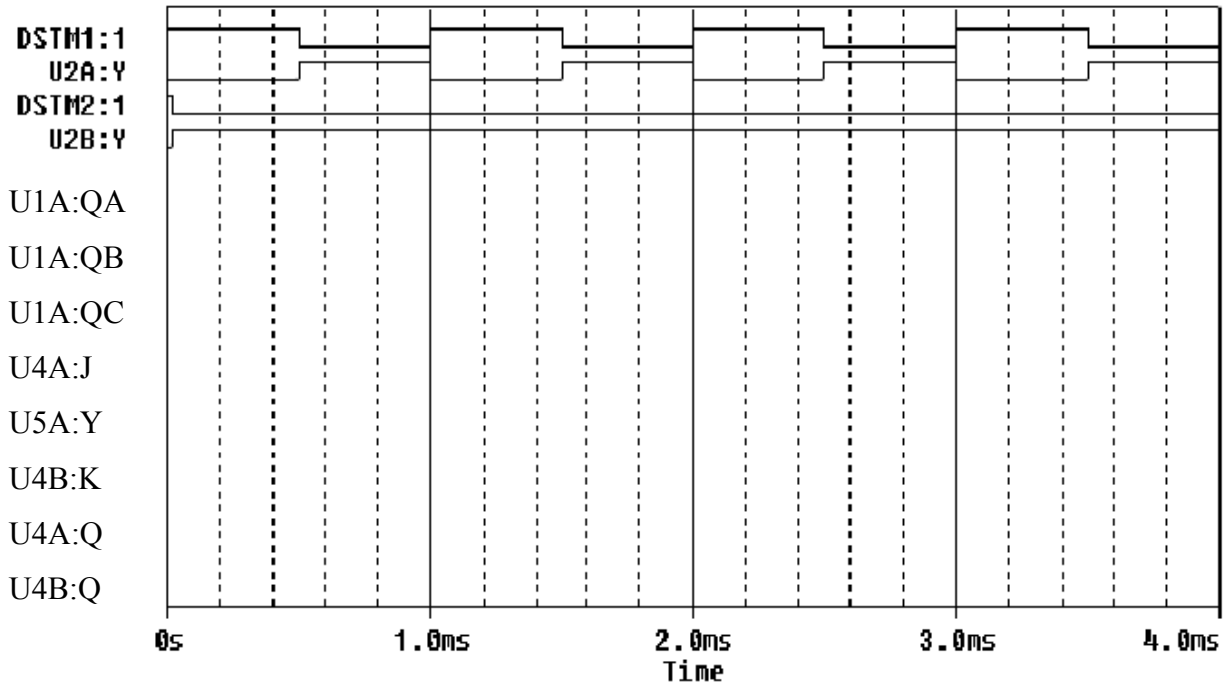
4. Of the basic 2-input logic gates, which could be used for the ARITHMATIC multiply operation of 1-bit binary numbers A and B. (***3 pts***)

Question III – Sequential Logic Circuits (20 points)



In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and two flip flops. The flip flops are clocked one half cycle after the counter to allow for propagation of the signals through the gates. (The counter changes on the negative edge of DSMT1 and the flop flops change on the negative edge of U2A:Y.) DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.

1. The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the counter (U1A:QA, U1A:QB, & U1A:QC); the output from the combinational logic (U2C:Y=U4A:J, U5A:Y=U4A:K=U4B:J, & U2D:Y=U4B:K); and the output from the flip flops (U4A:Q & U5A:Q). (2 pts per trace = ***16 pts***)



2. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 11 clock pulses? Clearly indicate the state of each signal. (***2 pts***)

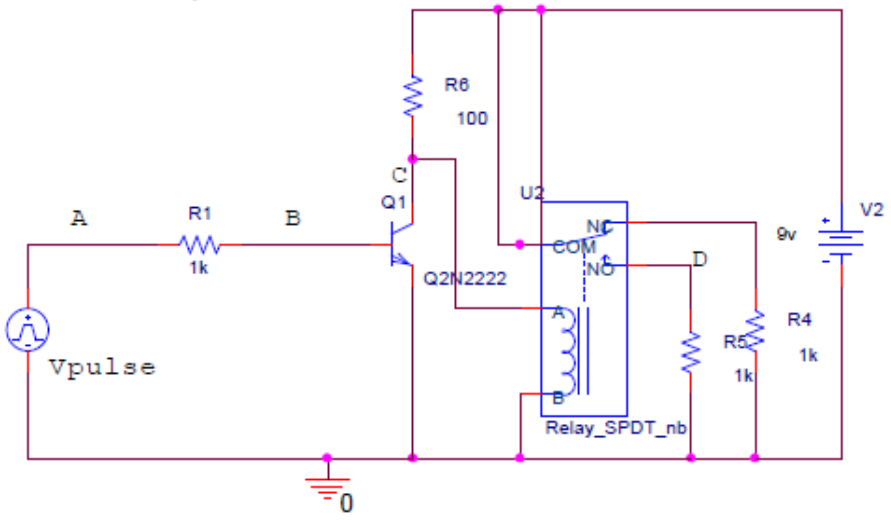
QD	QC	QB	QA

3. A 4-bit counter is cleared and then receives a string of clock pulses. What are QA, QB, QC and QD after 21 clock pulses? Clearly indicate the state of each signal. (***2pts***)

QD	QC	QB	QA

Question IV – Switching Circuits (20 points)

Transistor Switch – Relay Circuit



In the circuit above, the voltage source Vpulse puts out a sequence of pulses and the voltages at the source and three other points are monitored (marked A, B, C, and D). The relay model used by PSpice lists ***the resistance of the coil to be 100 ohms*** (***This is important!***):

1. If Vpulse is off:
   a) What is the voltage at point D? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

   b) What is the voltage at point C? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

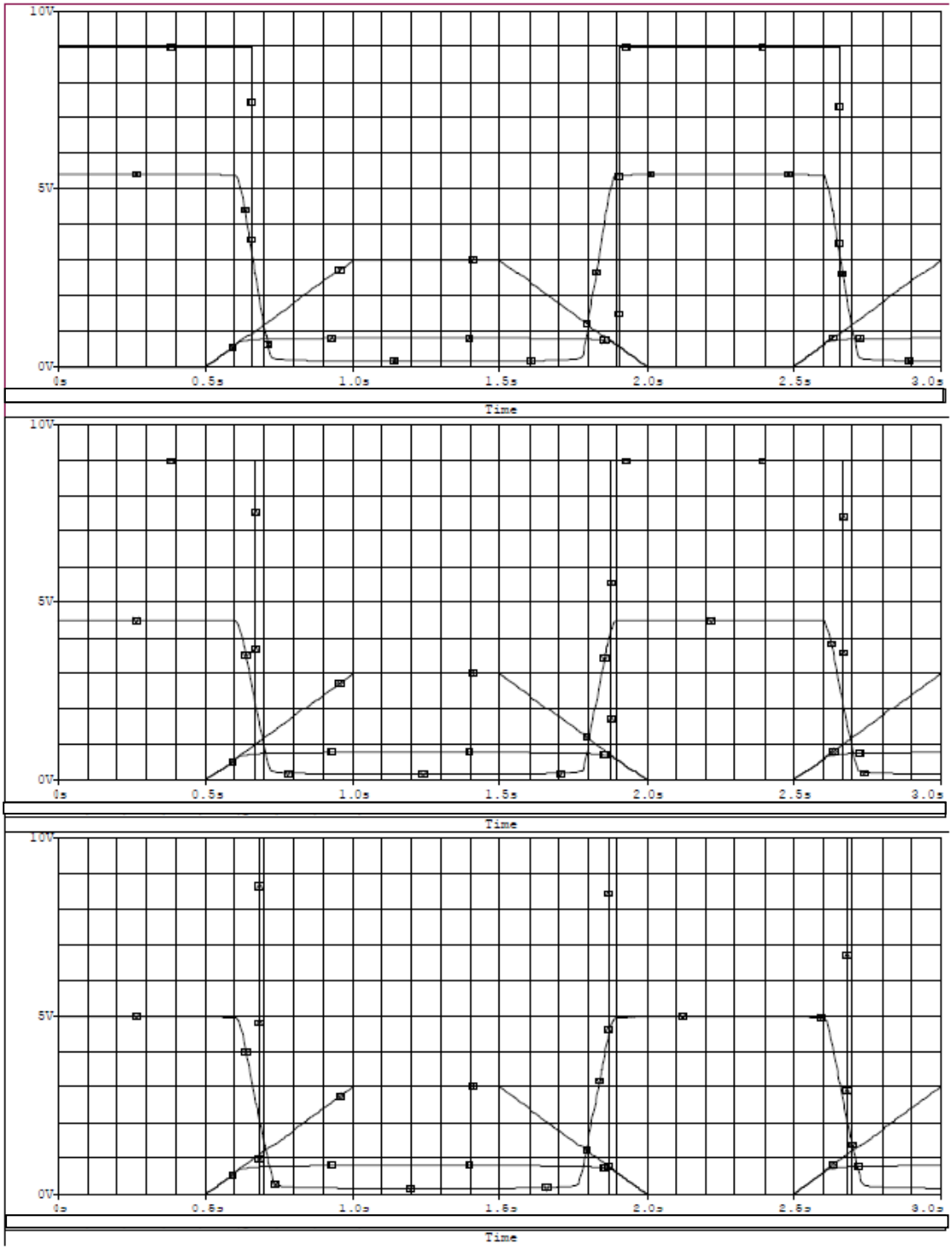
Question IV – Switching Circuits (continued)

2. If Vpulse is on (3V):
   a) What is the voltage at point D? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

   b) What is the voltage at point C? (***1 pt***) Explain why (circuit drawing with comments) (***1 pt***).

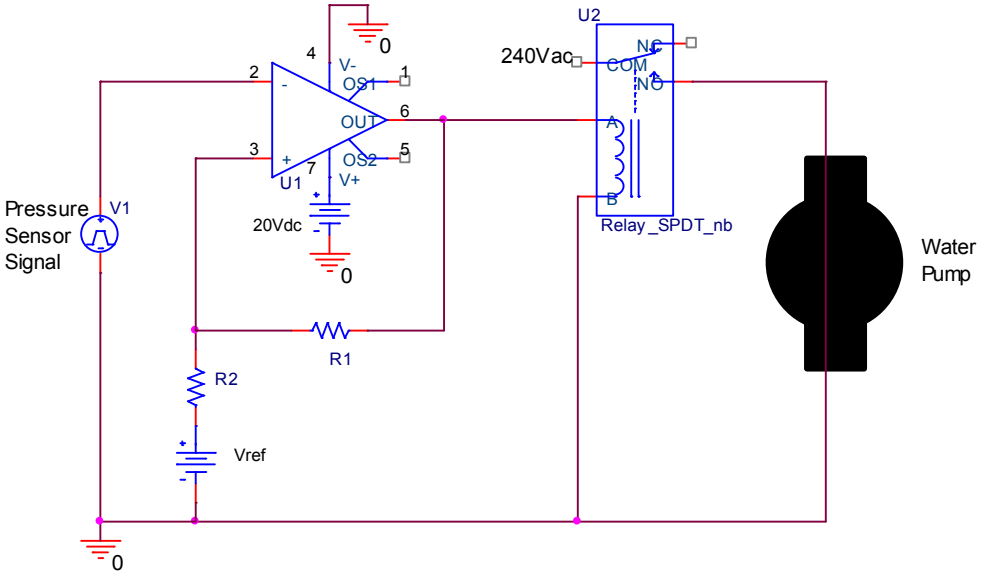
Question IV – Switching Circuits (continued)

3. Using this information and the overall circuit diagram, ***identify*** which of the following plots goes with this circuit (***4 pts***) ***AND label points A, B, C and D*** (***8 pts***) on the plot. (Mistakes will be carried over from parts b and c as a deduction).



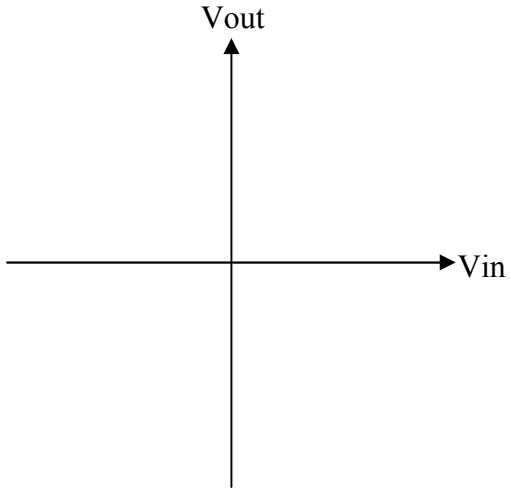
Question V – Comparators and Schmitt Triggers (25 points)

1. (2pt) A typical rural dwelling has a well, pump, and pressure tank to supply the household water. The system is designed to turn on the pump when the tank water pressure is 20psi and turn it off when it reaches 40psi. What is the name associated with a switching system exhibiting this behavior?



2. (3pt) Given a tank pressure sensor transducer circuit that outputs 0.5V/psi (V1 in the above circuit), what would be appropriate voltage thresholds for the high power ideal op-amp circuit to match the pump's two switching points?

3. (5pt) On the axes below sketch the input-output curve for the circuit in 1. Be sure to scale both axes.



Question V – Comparators and Schmitt Triggers (continued)

4. (6pt) Set up the equations to find appropriate values for R1, R2, and Vref in the circuit above in terms of the op-amp's supply voltages and the desired switch points for the water pump.

5. (4pt) Given that R2 = 1k, find the values of R1 and Vref. (hint: two equations two unknowns: simplify $v+_{high}$ and/or $v+_{low}$)

6. (5pt) If the circuit below is built (note: new op-amp V+ supply), what are the high and low pressure switching points, given the same pressure transducer?