ENGR-4300
Spring 2008
Test 3 Conflict

Name _____SOLUTION_____

Section   1(MR 8:00)   2(TF 2:00)   3(MR 6:00)
(circle one)

Question I (20 points) _____

Question II (20 points) _____

Question III (20 points) _____

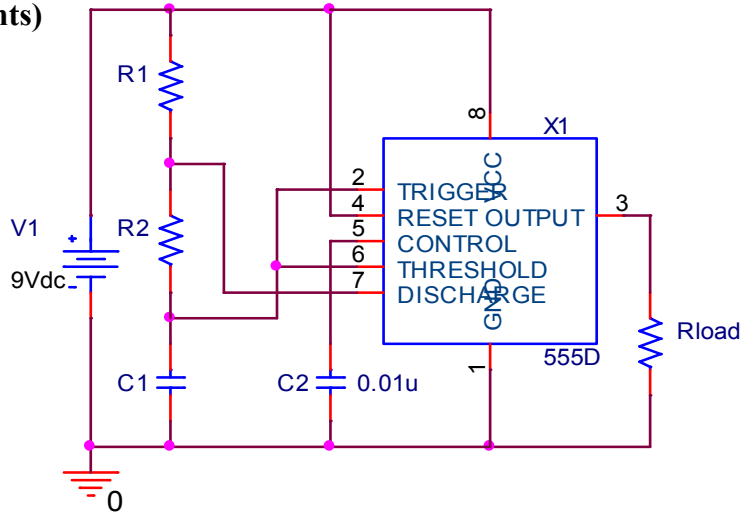Question IV (15 points) _____

Question V (25 points) _____

Total (100 points): _____

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES <u>AND UNITS</u>. No credit will be given for numbers that appear without justification.

Question I – Astable Multivibrator (20 points)

The 555 timer circuit shown is found to
have an output on pin 3 plotted below.
R1 = 2k, R2 = 10k, C1 = 19.68μF

1. (3pt) Calculate the period of the output
signal.

T = 0.693(R1 + 2xR2)C1
T = 0.693(22k)(19.68μ) = 0.300s

2. (3pt) Calculate the duty cycle of the
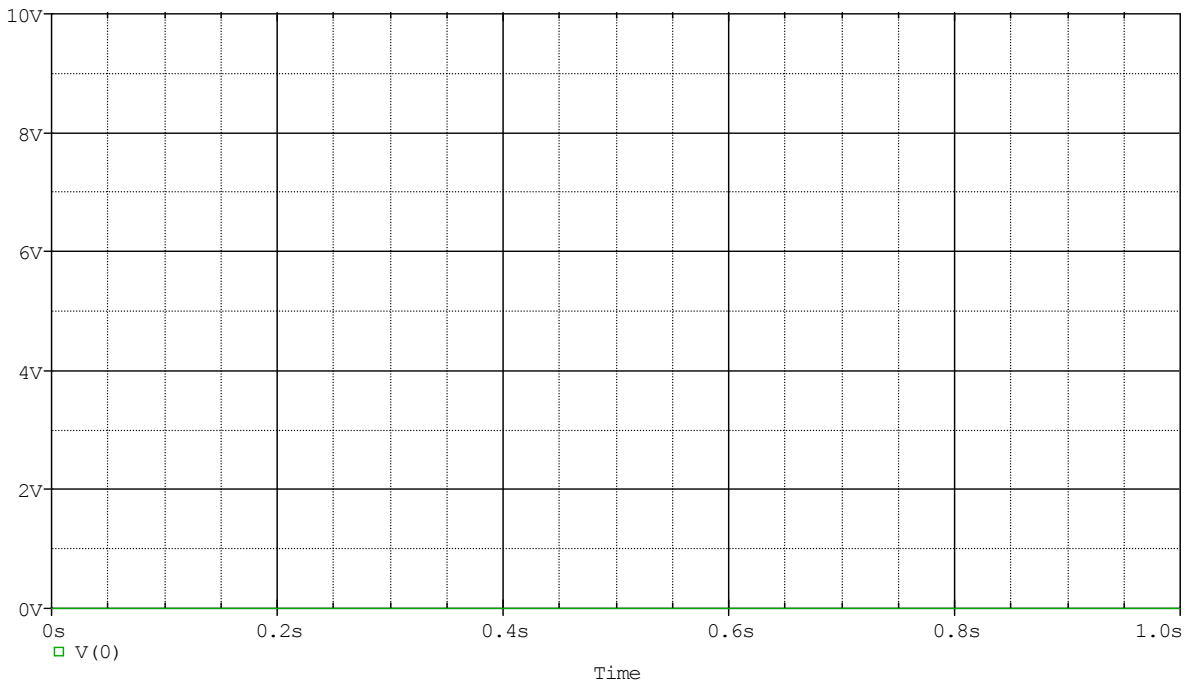output.

Duty cycle=T1/T=(R1+R2)/(R1+2R2)
= 12/21 = 54.5%

3. (1pt) If an LED were properly driven by pin 3 above, would your eye be able to detect the
flashing?

Frequency = 1/T = 1/0.3 = 3.33Hz   YES, slow enough to detect flashing with eye

4. (3pt) TRUE or FALSE: If R2 is decreased, both the frequency and duty cycle will increase.

TRUE   frequency will increase and duty cycle will increase too

5. (10pt) Add traces to the plot sketching the voltages on pin 2 and 3 of the circuit above and be
sure to label each.
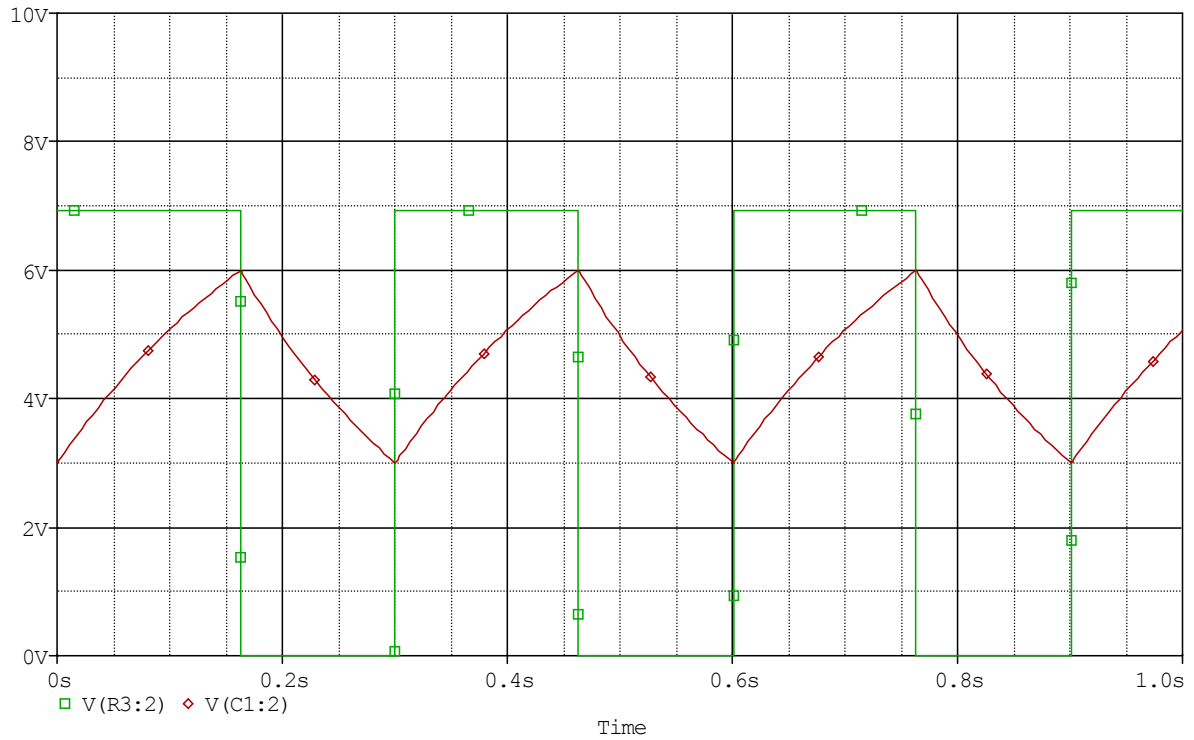
Vpin2 swings between 3V and 6V (1/3 & 2/3 of 9V)
Vpin3 is either grounded (0V) or 9V (actual voltage is ~7V)

Question II – Combinational Logic Circuits (20 points)

1. (8pt) For the following circuit, complete the truth table. That is, find the four outputs for all possible input conditions. Note that it is not necessary to fill out the entire table of values at all possible locations in the table, but this is the best way to solve this problem. It will also help us to understand where you may have gone wrong if your answers for the three outputs are not correct. Note that the circuit is very well labeled so you can easily identify which location goes with each letter.
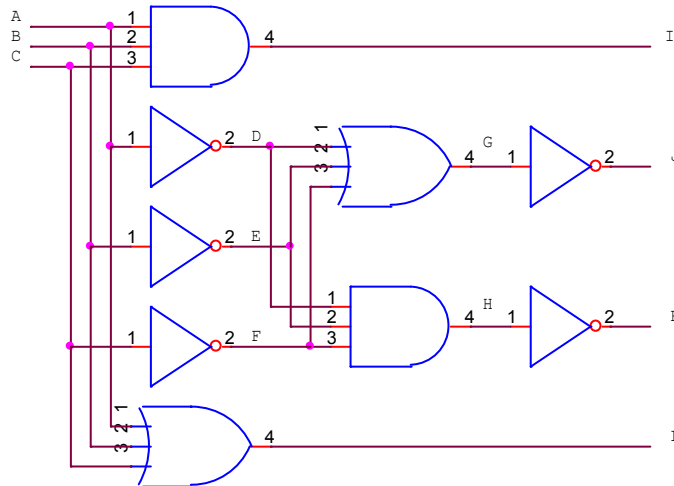
A	B	C	D	E	F	G	H	I	J	K	L
0	0	0	1	1	1	1	1	0	0	0	0
0	0	1	1	1	0	1	0	0	0	1	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0	0	0	1	1
1	0	0	0	1	1	1	0	0	0	1	1
1	0	1	0	1	0	1	0	0	0	1	1
1	1	0	0	0	1	1	0	0	0	1	1
1	1	1	0	0	0	0	0	1	1	1	1

NOTE FROM TABLE: I = J and K = L

Question II – Combinational Logic Circuits (continued)

2. (4pt) Write the Boolean expressions for I, J, K, and L in terms of A, B, and C, their inverses (overbars on variables), and logic operators AND, OR, and NOT.

$$I = A \bullet B \bullet C$$
$$J = \overline{\overline{A} + \overline{B} + \overline{C}}$$
$$K = \overline{\overline{A} \bullet \overline{B} \bullet \overline{C}}$$
$$L = A + B + C$$

3. (4pt) From columns I & J or K & L in the table, what property is being demonstrated or describe in words what can be observed about these logical expressions?

DeMorgan's Principal:
Inverting the inputs to an OR gate and inverting its output yields the same results as an AND gate
Inverting the inputs to an AND gate and inverting its output yields the same results as an OR gate

4. (4pt) For A = 0, B = 1, C = 1, D = 1, and E = 1, what is the value of the expression:
$(A \oplus B) + (\overline{C} \bullet D \bullet E) + \overline{A} \bullet (C + E) + B \bullet (A + D + \overline{E})$?
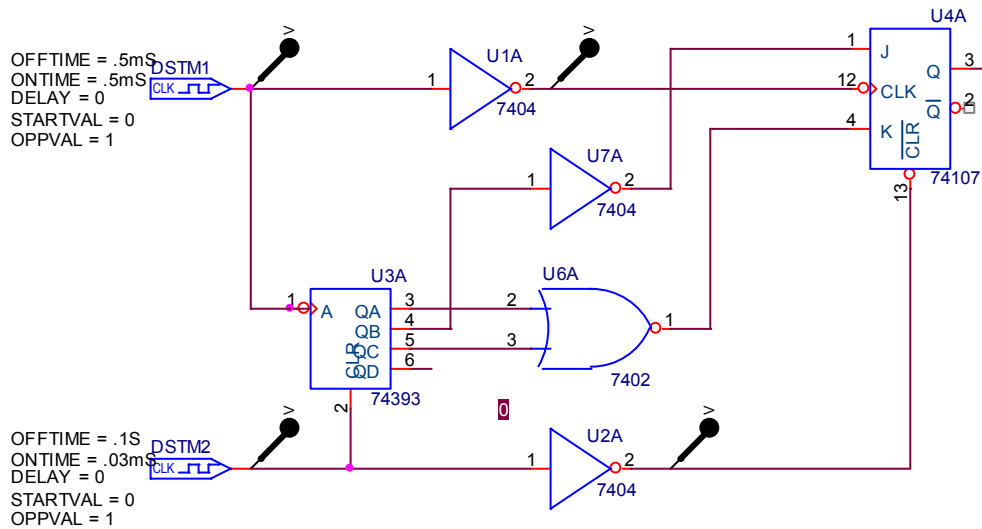
$$(A \oplus B) + (\overline{C} \bullet D \bullet E) + \overline{\overline{A}} \bullet (C + E) + B \bullet (A + D + \overline{E})$$
$$= (0 \oplus 1) + (0 \bullet 1 \bullet 1) + \overline{1 \bullet (1 + 1)} + 1 \bullet (0 + 1 + 0)$$
$$= 1 + 0 + 0 + 1$$
$$= 1$$

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Question III – Sequential Logic Circuits (20 points)

In the circuit pictured above, clock DSTM1 provides a clock signal to a counter and a flip flop. The flip flop is clocked one half cycle after the counter to allow for the propagation of the signals through the gates. (DSTM2 provides an initial reset pulse to both chips. This is required by PSpice to ensure that all sequential devices start in a known state.)

1. (14pt) The timing diagram below shows the reset pulses and the clock signals. Sketch the following signals in the space provided: the output from the timer (U3A:QA, U3A:QB, U3A:QC, and U3A:QD); the output from the combinational logic (U7A:Y and U6A:Y); and the output from the flip flop (U4A:Q).
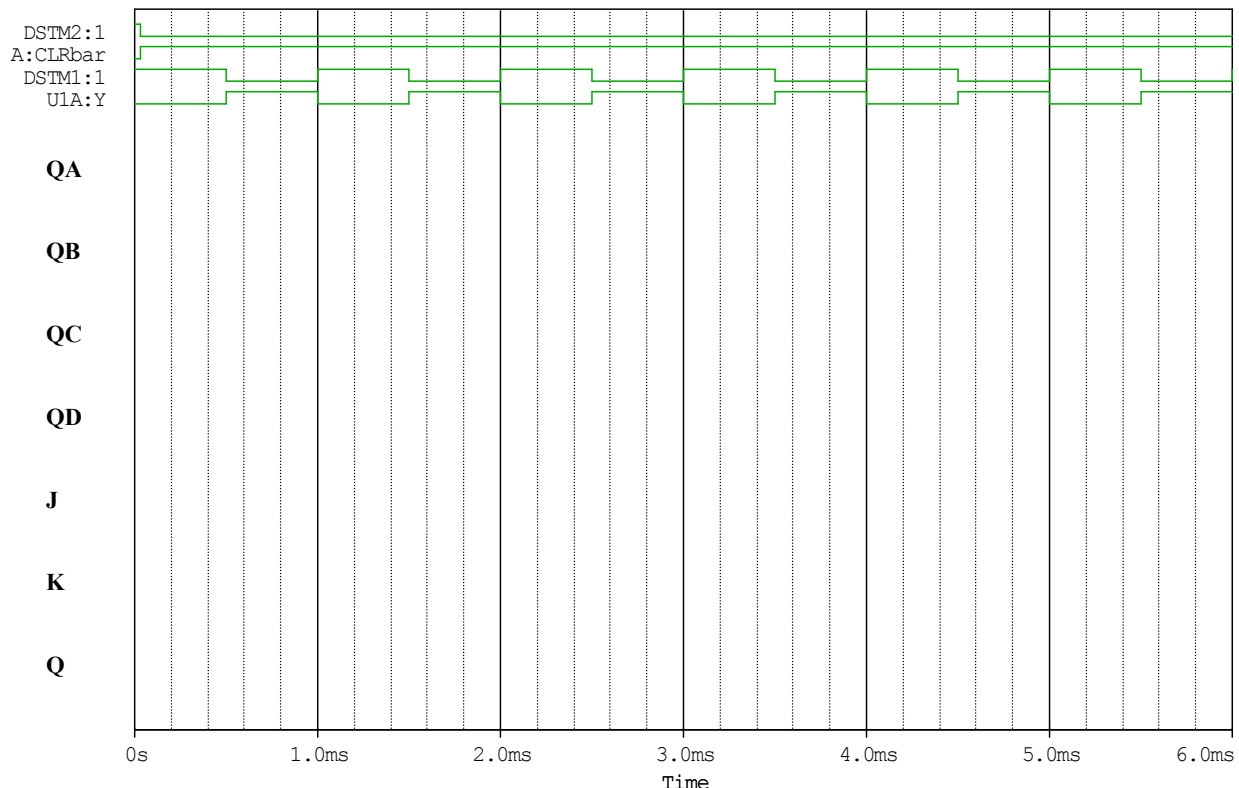
Question III – Sequential Logic Circuits (continued)

2. (2pt) From your knowledge of working with the 74393 counter in the studio, which output bit represents the 2^1 bit in a binary number formed from the four bits generated by the counter?

QB

3. (2pt) Assume that Q = 0 and J = K = 1. Based on the truth table of the J-K flip-flop above, how will the output Q behave when this device is clocked while pin 13 is false (low)?

Pin 13 is the low-active clear so the flip-flop will remain cleared as long as 13 is low. The output Q will remain low (= 0).
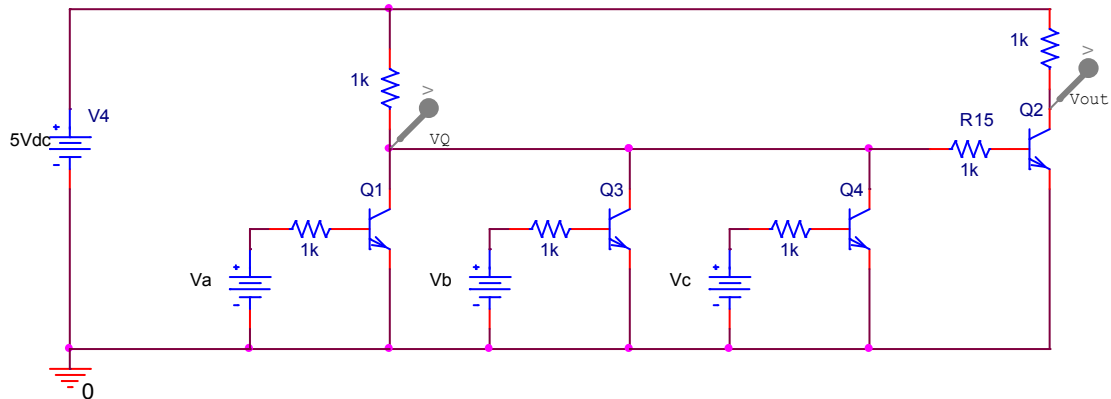
4. (2pt)A 4-bit 74393 counter's current state is 0110. It receives a string of clock pulses starting with a low to high transition. What are QA, QB, QC and QD after the 14th clock pulse's rising edge? Clearly indicate the state of each signal.

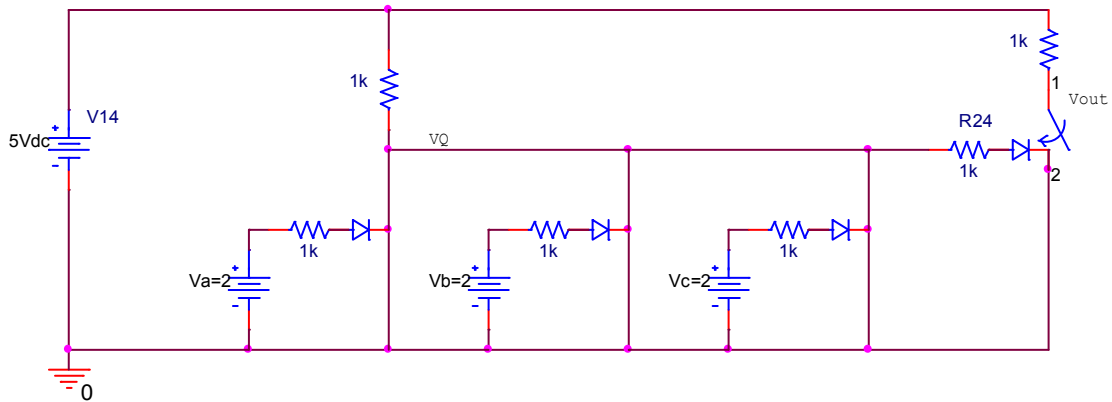| QD	QC	QB	QA
0	0	1	1

Only counts on falling edge of clock. 6 + 13 pulses = 19 => 0011
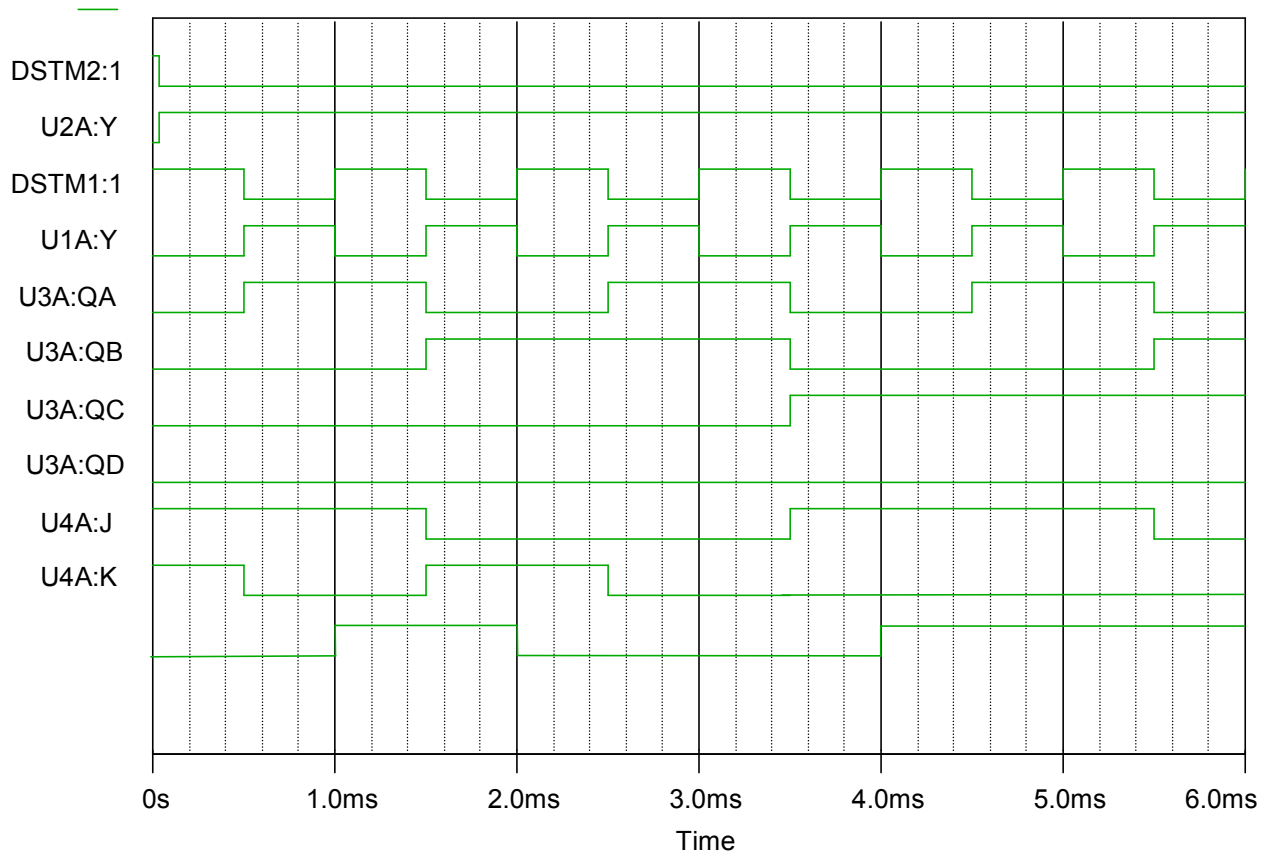
Question IV – Switching Circuits (15 points)

1. (4pt) Replacing the transistors in the above circuit with diodes and switches, redraw the above circuit when inputs Va = 2V, Vb = 2V, and Vc = 2V, replacing the open or closed switches with open or short circuits.

2. (2pt) Find the values of the voltages VQ and Vout for these inputs.

VQ = 0V
Vout = 5V

Question IV – Switching Circuits (continued)

3. (4pt) Replacing the transistors in the above circuit with diodes and switches, redraw the above circuit when inputs Va = 0V, Vb = 0V, and Vc = 0V, replacing the open or closed switches with open or short circuits.
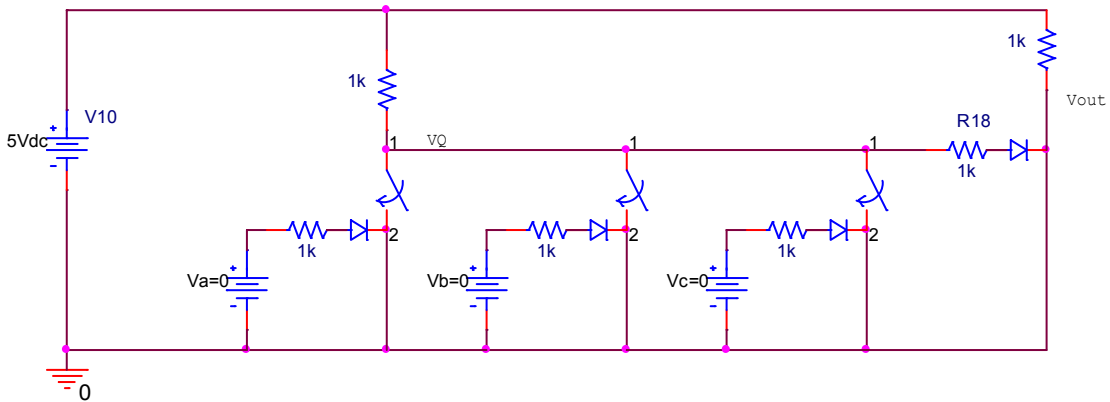

4. (4pt) Fill in the table below:

Va	Vb	Vc	VQ	Vout
0V	0V	0V	~2.5V	0V
0V	0V	2V	0V	5V
0V	2V	0V	0V	5V
0V	2V	2V	0V	5V
2V	0V	0V	0V	5V
2V	0V	2V	0V	5V
2V	2V	0V	0V	5V
2V	2V	2V	0V	5V

5. (1pt) What logic function does this circuit perform (assume 0V = 0 & >1V = 1)?

3-Input OR GATE

Question V – Comparators and Schmitt Triggers (25 points)

1. (4pt) Given the circuit below, find the reference voltage for the Schmitt Trigger if the desired switching voltages are +3V and -4.2V when R1 = 3k and R2 = 2k. Assume the op-amp output voltages will be equal to the supply voltages.
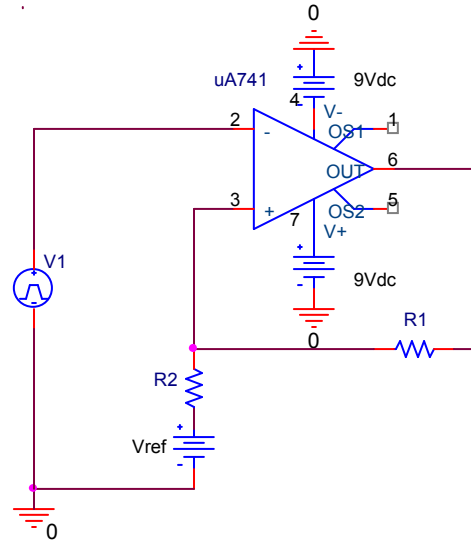
$$v+ = \frac{R2}{R1+R2}(v_{out} - V_{ref}) + V_{ref}$$

$$v+_{high} = \frac{2k}{3k+2k}(+9 - v_{ref}) + v_{ref} = +3V$$

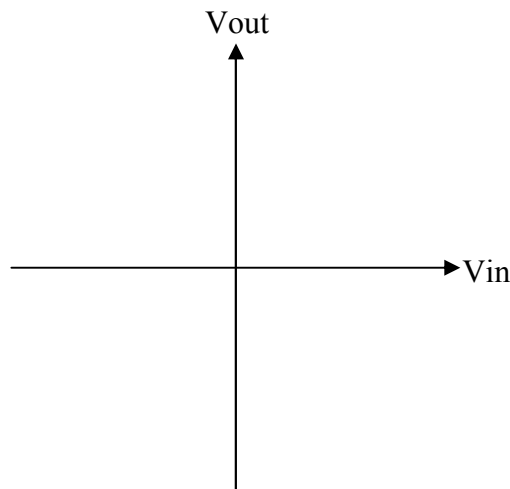$$v+_{low} = \frac{2k}{3k+2k}(-9 - v_{ref}) + v_{ref} = -4.2V$$

$$v+_{high} = \frac{2}{5}(+9 - v_{ref}) + v_{ref} = 3.6 + \frac{3}{5}v_{ref} = +3V$$

$$v_{ref} = -1V$$

$v_{ref} =$ _____

2. (4pt) On the axes below sketch the input-output curve for the circuit in1. Be sure to scale both axes.

Vout

Vin

3 (2pt) Find the width of the hysteresis band (include units) for the circuit above.

**Band = v+$_{high}$ – v+$_{low}$ = 3 – (-4.2) = 7.2V**

Question V – Comparators and Schmitt Triggers (continued)

4. (3pt) Given the comparator circuit on the right, assume the op-amps are powered by +5V and ground to provide a binary logic value on outputs DCBA. Assuming the standard low (0V) is a binary 0 and high (5V) is a binary 1, what is the expected binary output DCBA when Vin = 0V?

> **0V is below all the op-amp reference voltages so all outputs will be low (0V)**
> **DCBA = 0000**

5 (3pt) What is the expected binary output DCBA when Vin = 5V?

> **5V is above all the op-amp reference voltages (1V, 2V, 3V, & 4V for A, B, C, & D) so all outputs will be high (5V)**
> **DCBA = 1111**
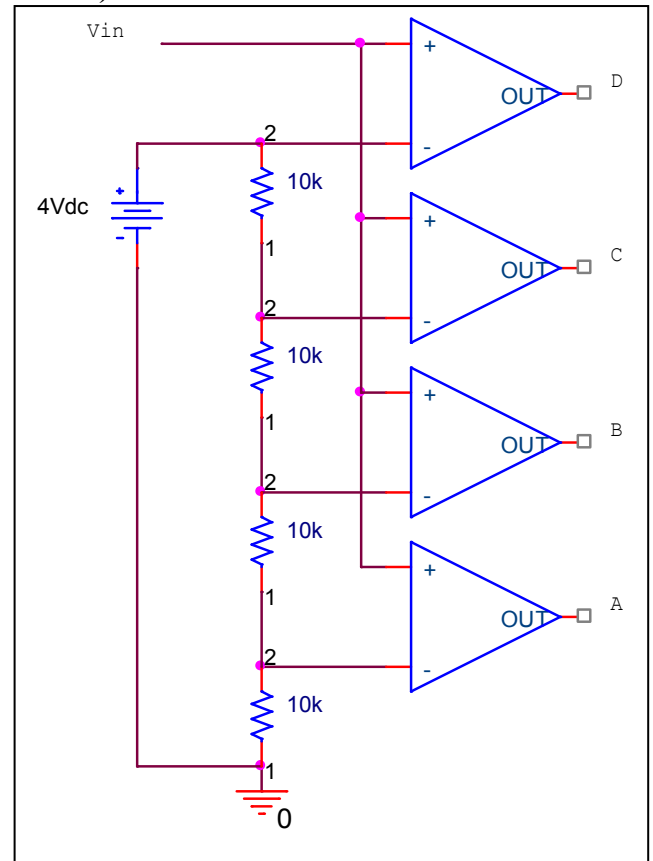
6. (6pt) What range of Vin would produce an output DCBA = 0111?

> **3V <Vin < 4V for A, B & C outputs HIGH (+5V) and D outputs LOW (0V)**

7. (3pt) Will this circuit produce a normal digital output for an increasing Vin from 0 to 5 V, i.e. a sequence of 0000, 0001, 0010, 0011, …? Explain why or why not.

> **NO, the binary output will be 0000, 0001, 0011, 0111, 1111 for increasing Vin. Once Vin exceeds the reference input for a given comparator, the output will stay at 1. This is called a "temperature gauge" binary output.**