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## Question 1 -- Flip Flops and Counters (20 points)


a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (counter clock), the second trace shown is DSTM3 (flip flop clock), and DSTM2 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0 . Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2) (3 points each $=18$ points)

b) To what value does the counter count in the time frame indicated? (2 points)

110 (binary) = 6 (decimal)
(The highest order bit is not pictured.)
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$\qquad$
Question 2 - Logic Gates (20 points)

a) Match the gate on the left with an equivalent circuit on the right. (10 points)

$$
\begin{aligned}
& A=1 \quad B=2 \quad C=5 \quad \boldsymbol{D}=4 \boldsymbol{E}=3 \\
& 1 \text { and } 5 \text { are DeMorgan's Laws } \\
& 3 \text { is } \sim(A \text { and } A)=\sim A \sim(A \text { or } A)=\sim A \text { too } \\
& 2 \text { is } \sim(\sim A \text { or } \sim B)=\sim \sim(A \text { and } B) \text { by DeMorgan's Law }=(A \text { and } B) \\
& 4 \text { is } \sim(\sim A \text { and } \sim B)=\sim \sim(A \text { or } B) \text { by Demorgan's Law }=(A \text { or } B)
\end{aligned}
$$

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$\qquad$
b) Fill in the truth table for the circuit below. (6 points)


| A | B | U2A:Y | U1A:Y | U3A:Y | Q |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| 0 | 1 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| 1 | 0 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| 1 | 1 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |

c) Write the Boolean expression for the circuit in b. Do not simplify. (4 points)
$Q=\{(\overline{A \bullet \bar{A}})+\{(B \bullet(\overline{A \bullet \bar{A}}))\}$

Extra credit (1 point): Simplify the Boolean expression in c) using the rules of Boolean algebra on your crib sheet.

$$
\begin{array}{ll}
Q=\{(\overline{A \bullet \bar{A}})+[(B \bullet(\overline{A \bullet \bar{A}}))\} & \text { From part c) } \\
Q=\{(\bar{A}+\overline{\bar{A}})+[(B \bullet(\bar{A}+\overline{\bar{A}})]\} & \text { DeMorgan's Law } \\
Q=\{(\bar{A}+A)+[(B \bullet(\bar{A}+A))\} & \overline{\bar{X}}=X \\
Q=\{1+[(B \bullet 1)]\} & \bar{X}+X=1 \\
Q=\{1+B\} & X \bullet 1=X \\
Q=1 & X+1=1
\end{array}
$$

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## Question 3 -- Schmitt Trigger (20 points)

The following circuit was configured to study Schmitt Triggers. It includes the Schmitt trigger device (7414) we studied in Experiment 10 and the op-amp configuration assembled to produce a Schmitt Trigger circuit.


The voltage source is a combination of two sinusoidal sources at two different frequencies. The higher frequency source is coupled in through a capacitor, since this is what must be done in a real circuit. The voltage levels for the op-amp Schmitt Trigger circuit are higher than for the commercial Schmitt Trigger. Thus, two resistors and a voltage source are used to change the input voltages to levels appropriate for a logic circuit. Note that we are also operating the op-amp in an unbalanced mode with the negative voltage source set to zero.

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The voltage signals measured at points $\mathbf{A}, \mathbf{B}, \mathbf{C}, \& \mathbf{D}$ in the circuit look like:


The voltage scale on the top plot ranges from 0 to 4 Volts, while the scale on the lower plot varies from 0 to 15 Volts.
a. Label each of the four signals with the letter $\mathbf{A}, \mathbf{B}, \mathbf{C}$, or $\mathbf{D}$ indicating where it is measured. (4 points)
b. Based on the properties of the voltage sources, what range of times is shown in these plots? Assume time starts at zero (as is shown). Label the rest of the time scale. (4 points)

The time scale is given. The lower frequency signal is 500 Hz , which has a period of 2 ms . Three periods is 4 ms , which is the maximum time.
c. At what voltages do the two circuits switch output states? Be as accurate as possible. (2 points each - 8 points)

Top plot (High to Low): 1.7V Top plot (Low to High): 0.9V
Bottom plot (High to Low): 7.3V Bottom plot (Low to High): 3.9V
Note that acceptable voltages can be within $0.3 V$ of these values for the bottom plot and $.2 V$ for the top plot. However, careful reading of the plots at the point where the voltage switches, should give these values. See an expanded version of the bottom plot on the next page.
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d. Assuming, as is shown, that $\mathrm{R} 2=10 \mathrm{k}$ Ohms, what must the value of R3 be to cause the output measured across R4 to switch at these voltages? (4 points)

For the case where the output is high (15V) the switch point is $7.3=5+(R 4 /(R 4+10 \mathrm{k})) * 10$ and where the output is low (0V) the switch point is $3.9=5 *(10 k /(R 4+10 k))$. Solving these two expressions gives $R 4=3 k$ and $2.8 k$, respectively. Thus, $3 k$ is probably the correct answer.

## $3 k$ is exactly the correct answer.

Given the range of voltages, any value from $2 k$ to $4 k$ is fine.
$\qquad$
$\qquad$

## Question 4 -- Digital-to-Analog Converter (20 points)

The circuit below converts digital signals into analog signals. This circuit produces an analog output voltage equal to the binary word DCBA in terms of the four inputs. Please assume that the input voltage levels for this circuit is 5 Volts for a logic of "one" and 0 Volts for a logic "zero" and that $\mathrm{R} 5=5 \mathrm{~K} \Omega$, R6 $=2 \mathrm{~K} \Omega$ and R7 $=30 \mathrm{~K} \Omega$.

a) Select values for R1, R2, R3, and R4 so that the output voltage will be the decimal equivalent of DCBA. For example, if $\mathrm{DCBA}=1010$, or equivalently $\mathrm{VD}=\mathrm{VB}=5 \mathrm{~V}$, $\mathrm{VA}=\mathrm{VC}=0 \mathrm{~V}$, then Vout $=10 \mathrm{~V}$. The circuit should work for all possible DCBA combinations. (12 points)

$$
\begin{aligned}
& V 1=(-R 5)[(V A / R 1)+(V B / R 2)+(V C / R 3)+(V D / R 4)] \quad \text { Vout }=(-R 7 / R 6) V 1 \\
& V o u t=(R 5 * R 7 / R 6)[(V A / R 1)+(V B / R 2)+(V C / R 3)+(V D / R 4)] \\
& (R 5 * R 7 / R 6)=(5 K * 30 K) / 2 K=75 K
\end{aligned}
$$

| Vout | $V A$ | $V B$ | $V C$ | $V D$ | plug in | solve |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | $5 V$ | 0 | 0 | 0 | $75 K(5 / R 1)=1$ | $R 1=375 \mathrm{~K}$ |
| 2 | 0 | $5 V$ | 0 | 0 | $75 K(5 / R 2)=2$ | $R 2=187.5 \mathrm{~K}$ |
| 4 | 0 | 0 | $5 V$ | 0 | $75 K(5 / R 3)=4$ | $R 3=93.75 \mathrm{~K}$ |
| 8 | 0 | 0 | 0 | $5 V$ | $75 K(5 / R 4)=8$ | $R 4=46.875 \mathrm{~K}$ |

$$
R 1=375 K \quad R 2=187.5 K \quad R 3=93.75 K \quad R 4=46.875 K
$$

Name: $\qquad$
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b) Show that the circuit correctly converts binary input 0111 to an AC voltage. What decimal number does 0111 represent? (4 points)

```
Vout=(R5*R7/R6)[(VA/R1)+(VB/R2)+(VC/R3)+(VD/R4)]
Vout =(75K)[(5/375K)+(5/187.5K)+(5/93.75K)+(0/46.875K)]
Vout = 1+2+4=7 volts
0111 = 7 decimal
```

c) Explain one way you could modify the values of the resistors in this circuit so that the output voltage gives $4 * \mathrm{~N}$ (rather than N ), when N is the digital number at the input . For example, when the input is $\mathrm{DCBA}=1010$, then Vout $=4 * 10 \mathrm{~V}$ or 40 V . You can modify any of the resistors R1-R7.(4 points)

The easiest way to do this is to modify one of the gain resistors:
$R 5=4 * R 5=20 K$
or
$R 7=4 * R 7=120 K$
or
$R 6=R 6 / 4=1.25 K$

You could also modify the four input resistors:
$R 1=R 1 / 4=93.75$ and $R 2=R 2 / 4=46.875 K$ and
$R 3=R 3 / 4=23.47$ and $R 4=R 4 / 4=11.73 \mathrm{~K}$

A combination which changes the gain would work also:
$R 5=R 5 * 2=10 K$ and $R 6=R 6 / 2=2.5 K$

Name: $\qquad$
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## 5. Transistor Switches

A simple logic circuit with two inputs and one output is configured as shown. The input voltages and the output voltages are plotted below.

a. Label which of these plots is the input V3 and the input V4. Also label which is the output measured across R5. (2 points each -6 points)

$\qquad$
$\qquad$
b. Based on the voltages displayed on the previous page, complete the following truth table for this configuration by putting a 0 or 1 in each of the output cells. (4 points)

| Input V3 | Input V4 | Output |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

c. What kind of device is this circuit? (2 points)

## NAND GATE

d. Under exactly the same conditions shown above, the voltages on either side of resistor R1 are displayed below. Again, identify which of the voltages traces is which by labeling them 'left' and 'right,' respectively. The time scale is the same as for the plots above and the voltage ranges from 0 to 5 Volts. (2 points each - 4 points)

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e. Explain your choice for d above: (4 points)

Case 1: left is 4.7 V and right is .7V. For this case, both diodes are off and the transistor is on so that the base voltage must be .7 V . Since the right point is connected to the base of the transistor, it must be the lower voltage.

Case 2: left is .6 V and right is -.9 V . For this case, either diode is on, which connects the left voltage point to ground through the diode. Since it takes .6 V to turn on the diode, the left must be at . 6 V

Extra Credit - Explain in detail how this circuit works for each of the four input combinations. (1 point)

Case 1: Both inputs high. For this case, the diodes must be off. Then we have the simple voltage divider circuit between 6 V and .7 V . The right voltage must be the voltage required to turn on the transistor ( .7 V ) while the left voltage must be $.7 \mathrm{~V}+(15 / 20) *(6-.7)=4.7 \mathrm{~V}$
Case 2: Either input low or both low. For these cases, at least one of the diodes must be on. Then the left voltage must be . 6 V to keep the diode(s) on. The right voltage is determined from the voltage divider relation $.6 \mathrm{~V}+(15 / 65) *(-6.6)=-.9 \mathrm{~V}$.
(see more detail on the next page)
$\qquad$
$\qquad$


Step 1) Note the values of the voltage sources.
The voltage source V3 generates a pulse which varies between 0 V and 5 V . Therefore point A can have a voltage of 0 V or 5 V . Similarly, the voltage source V4 generates a pulse which varies between 0 V and 5 V . Therefore point B can have a voltage of 0 V or 5 V . Point D is attached to a +6 voltage source, so it will always be at 6 V and point F is attached to a -6 voltage source (note source is upside down), so it will always have a voltage of -6 V .

Step 2) Determine when the diodes will be on and off.
The diodes are facing towards the sources, V3 and V4. This means that in order for diode D 1 to be on, the voltage at C must exceed the voltage at A by 0.6 volts. Similarly, in order for diode D2 to be on, the voltage at C must exceed the voltage at $B$ by 0.6 volts. We need to determine the voltage at point C. We can estimate this voltage by considering what the circuit would look like without V4, V3, D1 and D2 in it. In this case, the voltage at C is determined by a voltage divider. This voltage divider divides up the voltage between point D and point F . (The current going into the transistor at the base is always small, so we will ignore it.) The voltage between D and F is $(6 \mathrm{~V}-(-6 \mathrm{~V}))=12 \mathrm{~V}$. The drop over R3 is $(5 \mathrm{k} / 70 \mathrm{k}) * 12 \mathrm{~V}=0.8 \mathrm{~V}$. Therefore, the voltage at C can be estimated at $6-0.8=5.2$ volts. When the voltage at A is 5 volts, C does not exceed A by more than 0.6 volts ( $5.2-5=0.2$ ), so D 1 is off. When the voltage at A is 0 volts, $C$ does exceeed $A$ by over 0.6 volts ( $5.2-0=5.2 \mathrm{~V}$ ), and D 1 is on. The case is similar between B and C. B is 5 volts, D2 is off. B is 0 V , D2 is on. When either diode is on, the actual voltage at C is determined by the voltage drop between the diode (0.6) and the voltage source (which is ground when the input is 0 ).

| A | B | C (expected) | C-A | C-B | D1 | D2 | C (actual) |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 5.2 | 5.2 | 5.2 | on | on | 0.6 |
| 0 | 5 | 5.2 | 5.2 | 0.2 | on | off | 0.6 |
| 5 | 0 | 5.2 | 0.2 | 5.2 | off | on | 0.6 |
| 5 | 5 | 5.2 | 0.2 | 0.2 | off | off | 5.2 |

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Step 3) Determine the output when either diode is on.
If any diode is on, then point $C$ is essentially grounded through the diode to the source and its voltage is held to 0.6 V , C (actual) in chart above. Point E will turn the transistor on and off. In order to determine the voltage at E , we can use a voltage divider to divide up the voltage between C and F . C-F $=(0.6)-(-6)=6.6$ volts. The voltage over R 1 is $6.6(15 \mathrm{k}) /(65 \mathrm{k})=1.5 \mathrm{~V}$. Therefore, the voltage at point E is 0.6 -$1.5=-0.9 \mathrm{~V}$. The diode in the transistor will turn on when the voltage at E exceeds the voltage at H by 0.6 V . Since $\mathrm{E}-\mathrm{H}=-0.9$ volts, the transistor switch will remain open. When the transistor switch is open, the voltage at point $G$ (the output) will be the input voltage at $\mathrm{D}, 6 \mathrm{~V}$.

| A | B | C (actual) | C-F | E | Q1 | G |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0.6 | 6.6 | -0.9 | off | 6 |
| 0 | 5 | 0.6 | 6.6 | -0.9 | off | 6 |
| 5 | 0 | 0.6 | 6.6 | -0.9 | off | 6 |

Step 4) Determine the voltage at the output when both diodes are off.
If both diodes are off, the voltage at point C is unaffected by the two input sources because the diodes are both open switches. This means that this voltage will remain at the expected voltage of 5.2 volts. We can use the voltage divider again to determine the voltage at point $\mathrm{B} . \mathrm{C}-\mathrm{F}=5.2-(-6)=11.2 \mathrm{~V}$. The expected voltage drop over R1 is $(11.2)(15 \mathrm{k}) /(65 \mathrm{k})=2.6 \mathrm{~V}$. This makes the expected voltage at $\mathrm{B}=11.2-2.6$ $=8.6 \mathrm{~V}$. This is more than 0.6 volts, so the diode in the transistor turns on and the switch closes. When this switch closes, two things happen. The voltage at point $G$ (the output) is connected to ground and the voltage at point E is connected through the diode in the transistor to ground. This changes the output voltage at G to 0 volts. The voltage at point E drops to 0.6 volts and there is also a voltage loss at point C . The actual voltage at C can be determined by a voltage divider. $\mathrm{D}-\mathrm{E}=6-0.6=5.4$ volts. The voltage drop across R3 $=(5 \mathrm{k} / 20 \mathrm{k})(5.4)=1.3 \mathrm{~V} . \mathrm{C}=6-1.3=4.7 \mathrm{~V}$. This is the voltage shown in the output.

| A | B | C (expected) | C-F | B(expected) | Q1 | G | B(actual) | C(actual) |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 5 | 5 | 5.2 | 11.2 | 8.6 | on | 0 | 0.6 | 4.7 |

