Question 1 -- Flip Flops and Counters (20 points)
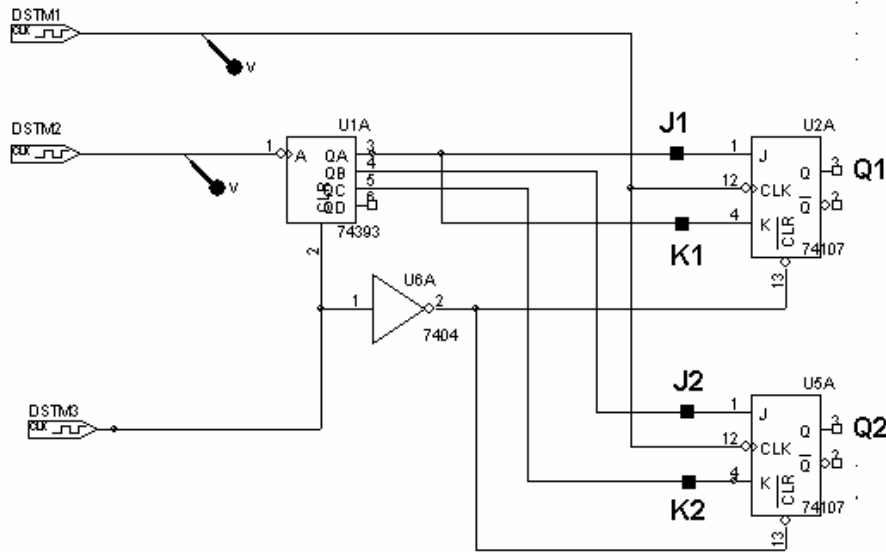

a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (flip flop clock), the second trace shown is DSTM2 (counter clock), and DSTM3 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0 and that all three devices change on the falling edge of the clock..   Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2)
(3 points each = 18 points)
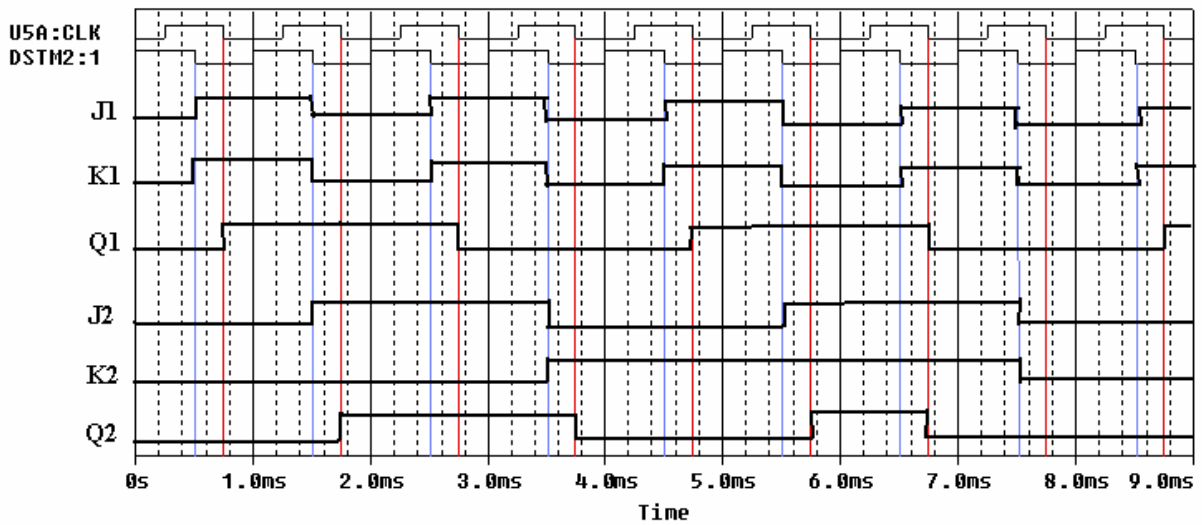
b) To what value does the counter count in the time frame indicated? *(2 points)*

$1001 = $ **9**

Question 2 – Logic Gates (20 points)
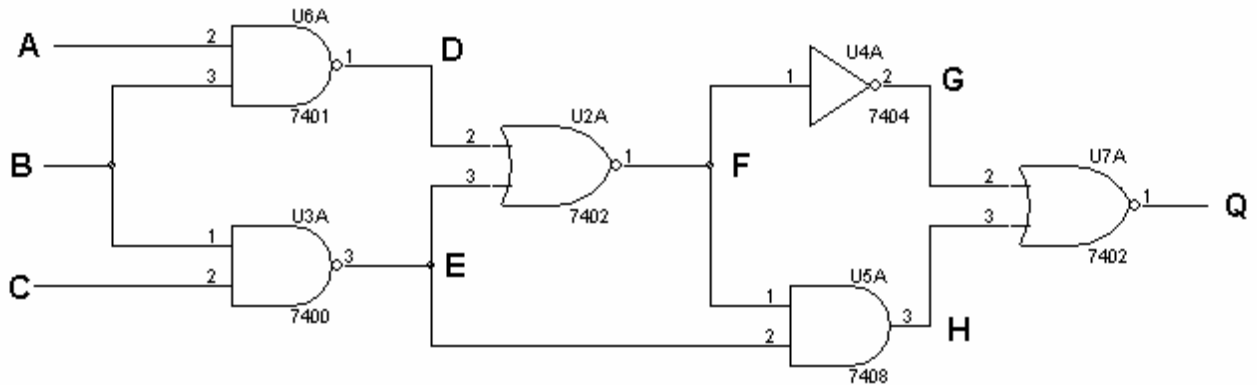
a)   Fill in the truth table for the circuit above: *(12 points)*

A	B	C	D	E	F	G	H	Q
0	0	0	*1*	*1*	*0*	*1*	*0*	*0*
0	0	1	*1*	*1*	*0*	*1*	*0*	*0*
0	1	0	*1*	*1*	*0*	*1*	*0*	*0*
0	1	1	*1*	*0*	*0*	*1*	*0*	*0*
1	0	0	*1*	*1*	*0*	*1*	*0*	*0*
1	0	1	*1*	*1*	*0*	*1*	*0*	*0*
1	1	0	*0*	*1*	*0*	*1*	*0*	*0*
1	1	1	*0*	*0*	*1*	*0*	*0*	*1*

b) Write the Boolean expression for the circuit in a). Do not simplify. *(6 points)*

Q = ~{G + H} = ~{~F + (F&E)} = ~{~~(D+E) + (~(D+E)&E)}
G = ~F H=F&E
F=~(D+E)
E= ~(B&C) D=~(A&B)

Q = ~{ [~~(~(A&B) + ~(B&C))] + [~(~(A&B)+~(B&C)) & ~(B&C)] }

c) What type of gate could the above circuit be replaced with to give the same results for
Q based on A, B and C? *(2 points)*

   1) ***Three input AND gate***

   2) Three input OR gate

   3) Three input NOR gate

   4) Three input NAND gate

   5) none of the above

Extra credit *(1 point):* Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.

<u>expression</u>   <u>rule</u>

$Q=\sim\{[\sim\sim(\sim(A\&B) + \sim(B\&C))] + [\sim(\sim(A\&B)+\sim(B\&C)) \& \sim(B\&C)]\}$ *given*

$Q=\sim\{[(\sim A\&B) + \sim(B\&C)] + [\sim(\sim(A\&B)+\sim(B\&C)) \& \sim(B\&C)]\}$ $\sim\sim X = X$

$Q=\sim\{\sim[(A\&B) \& (B\&C)] + [\sim\sim(A\&B \& B\&C)) \& \sim(B\&C)]\}$ $\sim X\&\sim Y=\sim(X\&Y)$

$Q=\sim\{\sim[A\&B\&B\&C] + [(A\&B\&B\&C) \& \sim(B\&C)]\}$ $\sim\sim X = X$

$Q=\sim\{\sim[A\&B\&C] + [(A \& (B\&C) \& \sim(B\&C)]\}$ $X\&X=X$

$Q=\sim\{\sim[A\&B\&C] +[A\&0]\}$ $X\&\sim X=0$

$Q=\sim\{\sim[A\&B\&C] + 0 \}$ $X\&0=0$

$Q=\sim\sim\{A\&B\&C\}$ $X+0=X$

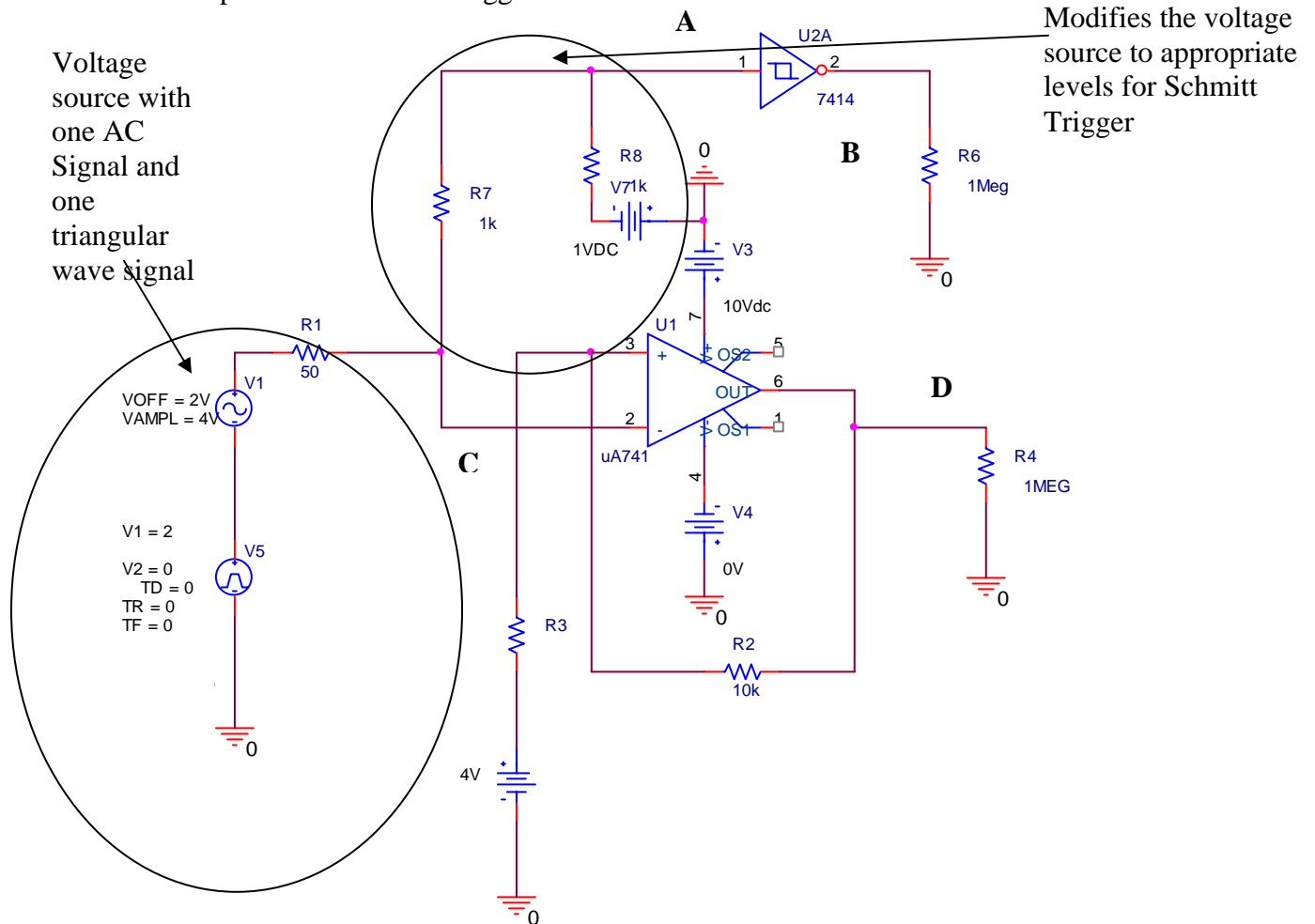**$Q= A\&B\&C$** $\sim\sim X=X$

QED

3. Schmitt Trigger

The following circuit was configured to study Schmitt Triggers. It includes the Schmitt trigger device (7414) we studied in Experiment 10 and the op-amp configuration assembled to produce a Schmitt Trigger circuit.

A

Modifies the voltage source to appropriate levels for Schmitt Trigger

U2A

7414

Voltage source with one AC Signal and one triangular wave signal

R8
V7 1k

R7
1k

1VDC

B
R6
1Meg

0

0

V3

10Vdc

R1
50

U1
3
+
2
-
uA741

OS2   5

OUT   6

OS1   1

7

4

D

R4
1MEG

0

V1
VOFF = 2V
VAMPL = 4V

C

V4
0V

0

V1 = 2
V2 = 0
 TD = 0
TR = 0
TF = 0

V5

R3

R2
10k

0

4V

0

The voltage source is a combination of two sources – one is sinusoidal and one is a triangular wave The latter source has the higher frequency. The voltage levels for the op-amp Schmitt Trigger circuit are higher than for the commercial Schmitt Trigger. Thus, two resistors and a voltage source are used to change the input voltages to levels appropriate for a logic circuit. Note that we are also operating the op-amp in an unbalanced mode with the negative voltage source set to zero.

The voltage signals measured at points **A, B, C,** & **D** in the circuit look like:
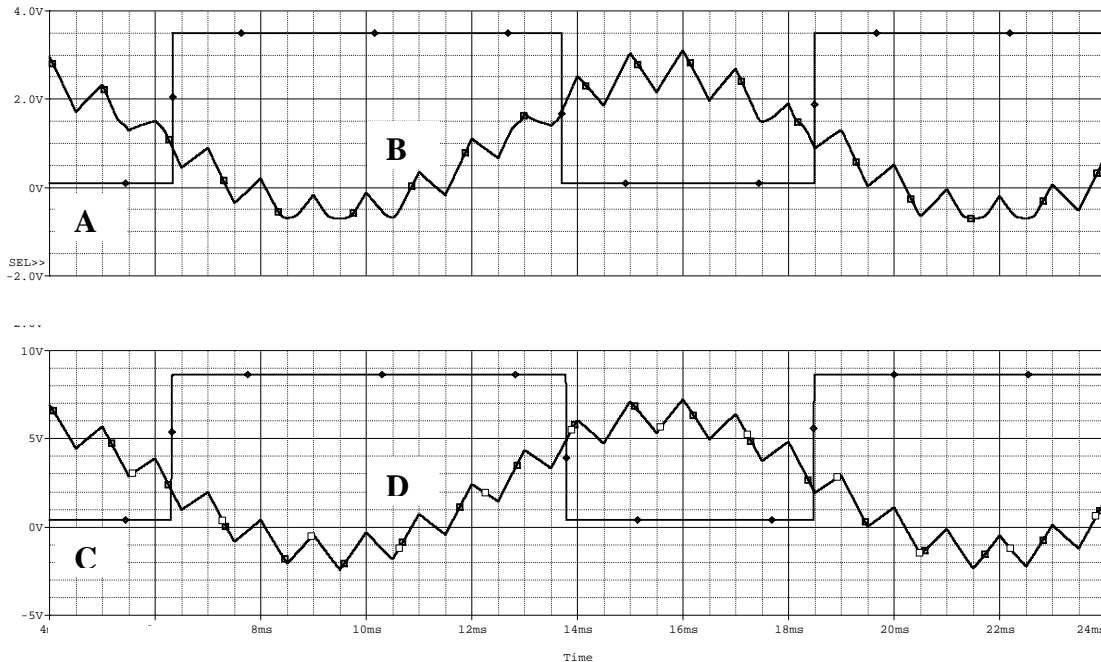
The voltage scale on the bottom plot ranges from -5 to 10 Volts, while the scale on the top plot varies from -2 to 4 Volts.

   a. Label each of the four signals with the letter **A, B, C,** or **D** indicating where it is measured. *(4 points)*

   b. What are the frequencies for both sources? *(4 points)*
The sinusoidal source operates at 800Hz. The triangular wave source has a frequency of 20kHz.

   c. At what voltages do the two circuits switch output states? *(8 points)*
     For the top plot, the output goes high at an input of .9V and goes back low at 1.7V. (These are consistent with the typical values quoted in the TI spec sheet. For the bottom plot the output goes high at 2.13V and low at 4.87V. Note that acceptable voltages can be within 0.3V of these values for the bottom plot and .2V for the top plot. However, careful reading of the plots at the point where the voltage switches, should give these values. See an expanded version of the bottom plot on the next page.

Top plot (Low to High): ***0.9V***   Top plot (High to Low): ***1.7V***

Bottom Plot (Low to High): ***2.13V***   Bottom plot (High to Low): ***4.87V***

d. Assuming, as is shown, that R2 = 10k Ohms, what must the value of R3 be to
   cause the output measured across R4 to switch at these voltages? *(4 points)*

*For the case where the output is high (8.6V) the switch point is
4.87=(10k/(R3+10k))*3+(R3/(R3+10k))*8.6 and where the output is low (.4V) the
switch point is 2.13=3*(10k/(R3+10k))+(R3/(10k+R3))*.4. Solving these two
expressions gives R3 about 5k. Reading the numbers less accurately off of the graph
will result in two different answers, but both should be near 5k. Given the range of
voltages, any value from 4k to 6k is fine.*
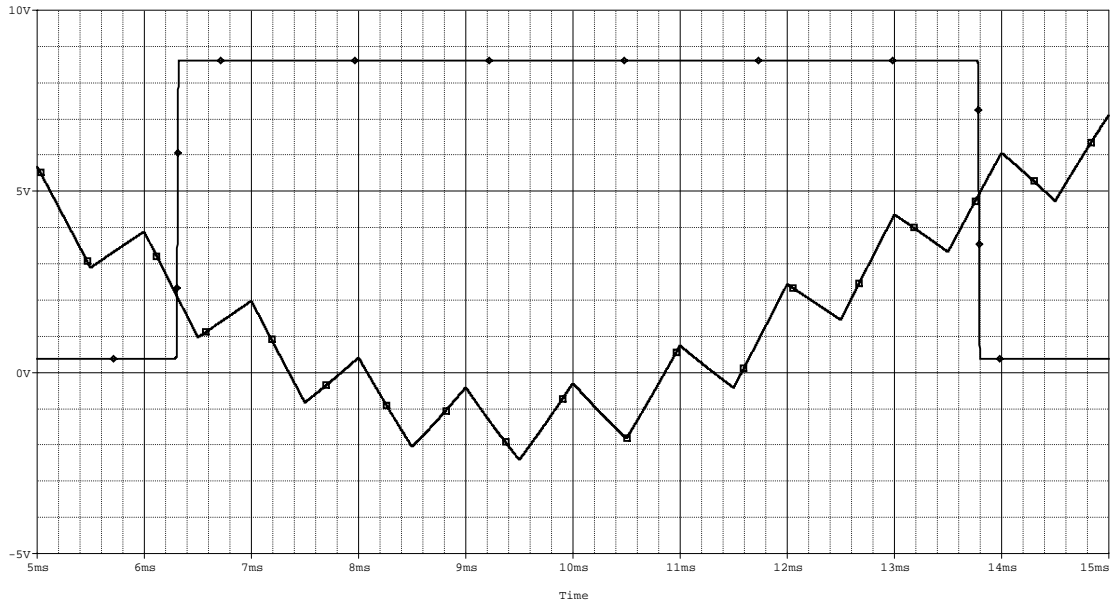

Expanded version of lower plot

Question 4 -- Digital-to-Analog Converter (20 points)

For a computer or other digital device to interface with external analog circuits and devices, a digital-to-analog converter (DAC) is required. The most common DAC is a R-2R resistor ladder network, which requires only two precision resistor values R and 2R. A 4-bit R-2R resistor ladder network is shown below:
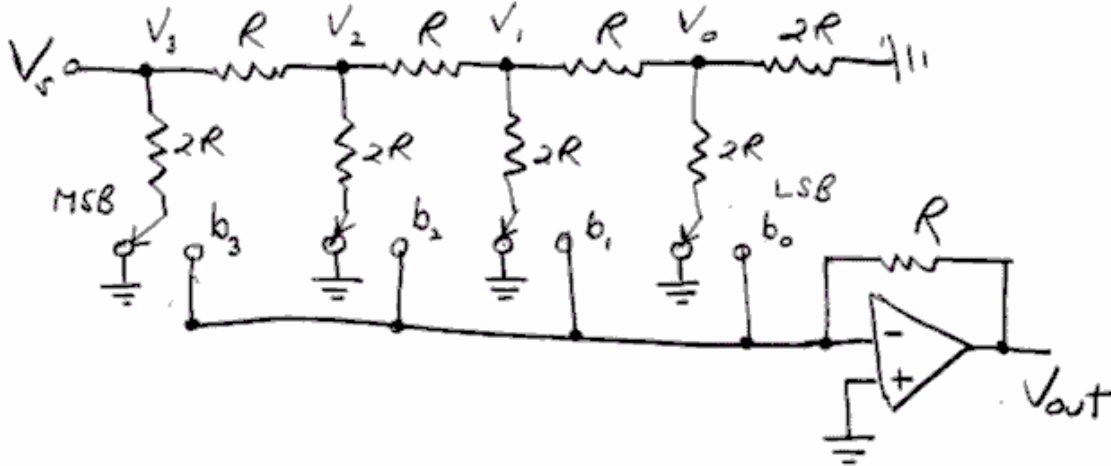
The digital input to the DAC is a 4-bit binary number represented by bits b0, b1, b2 and b3, where b0 is the least significant bit (LSB) and b3 is the most significant bit (MSB). Each bit in the circuit controls a switch between ground and the *inverting* input op amp. When a bit is 1, the corresponding switch is connected to the op-amp; when a bit is zero, the corresponding switch is connected to ground.

a) If we assume this is an ideal op-amp, we can analyze the voltage levels in the circuit by removing the op amp. Below is a picture of the circuit when all bits are zero. Use the simplified circuit below to determine the voltage levels at V0, V1, V2 and V3 in terms of the source voltage, Vs. *(8 points)*
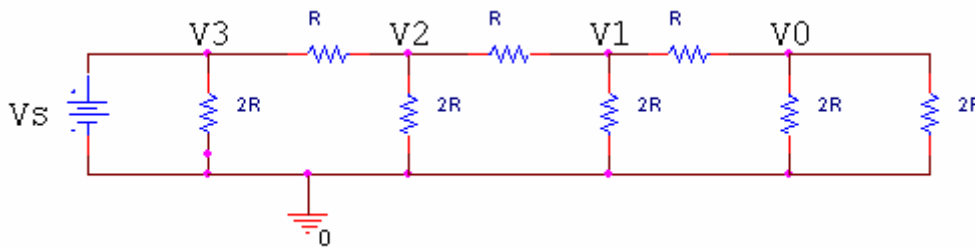
See following page for circuit analysis. When you combine 2 2R resistors in parallel, you get (2R*2R)/(2R+2R) = R. If you do this to the two 2R resistors in parallel at V0, you get a voltage divider that divides V1 in half. If you add the 2 1R resistors and combine them in parallel with the 2R resistor at V1, you get another voltage divider that divides V2 in half. You can continue this process until you get the voltage divider that divides V3 into half to get V2. You know that V3 is Vs. Therefore, V2 is Vs/2. You can then apply the relationships in reverse to get all the voltages.
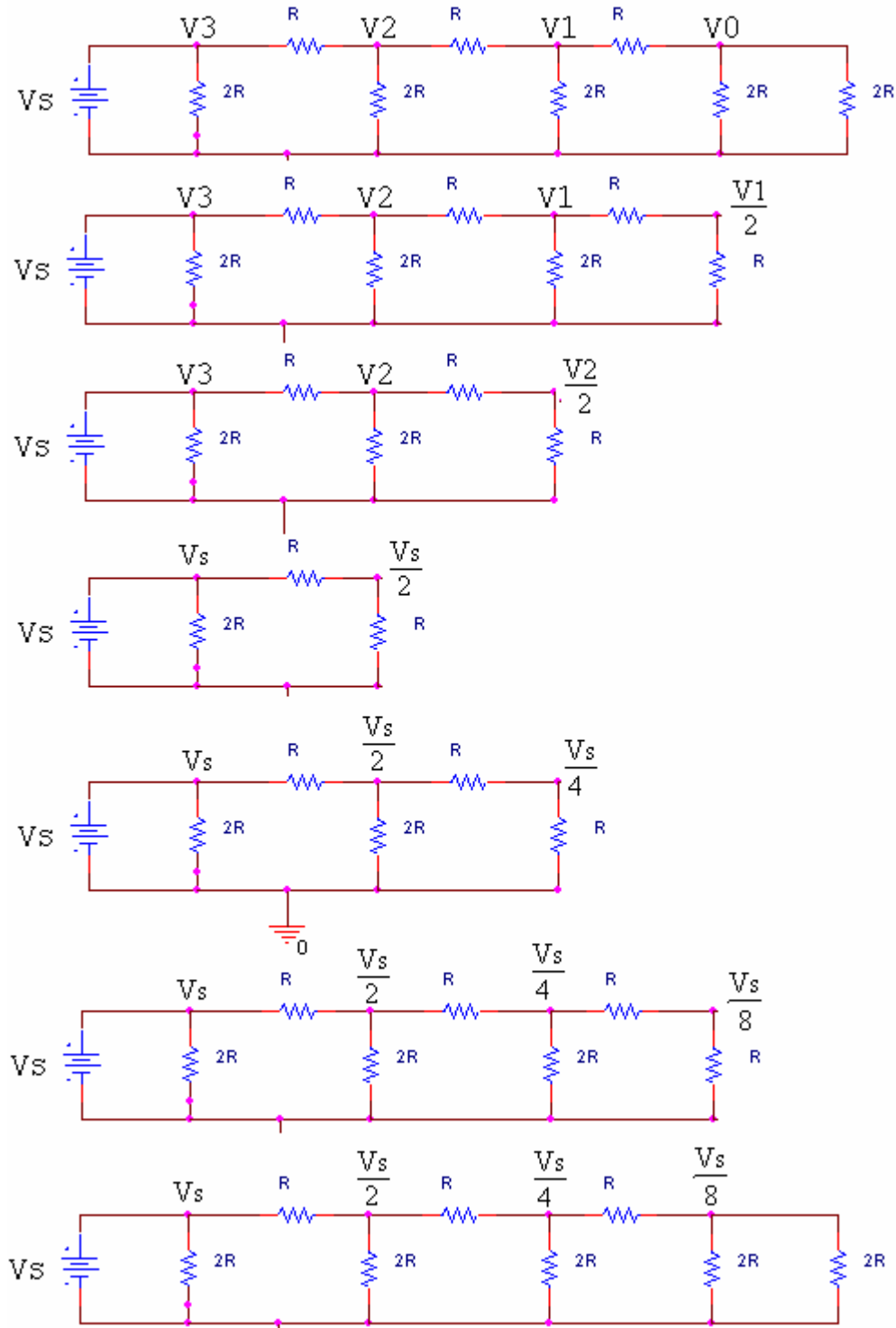
b) If we assume that closing switches has negligible effect on the voltage levels we found in part a), what will be the output of the DAC circuit, Vout (in terms of Vs), when the input (b3 b2 b1 b0) is: *(10 points)*

This assumption can be made because the op-amp is ideal and it tries to keep the voltages at the inputs the same. The positive input is grounded, therefore, the negative input is ground and the input circuit does not change regardless of the position of the switches. The value of Vout is determined by the inverting op-amp, which is acting on the input voltage of the corresponding bit with an input resistance of 2R and a feedback resistance or R.

0001: *Vout = -(R/2R)V0 = (-1/2)(Vs/8)*   **Vout = -(1/16)Vs**

0010: *Vout = -(R/2R)V1 = (-1/2)(Vs/4)* **Vout = -(1/8)Vs**

0100: *Vout = -(R/2R)V2 = (-1/2)(Vs/2)* **Vout = -(1/4)Vs**

1000: *Vout = -(R/2R)V3 = (-1/2)(Vs)* **Vout = -(1/2)Vs**

1111: [Hint: Use principal of superposition.]
        Vout = -(1/16)Vs + -(1/8)Vs + -(1/4)Vs + -(1/2) Vs
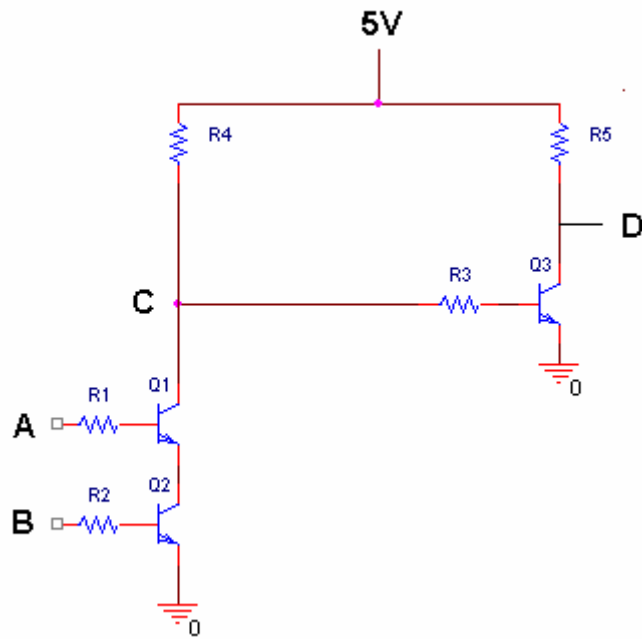   *Vout = -(1/16+2/16+4/15+8/16)Vs*

        Vout = -(15/16)Vs

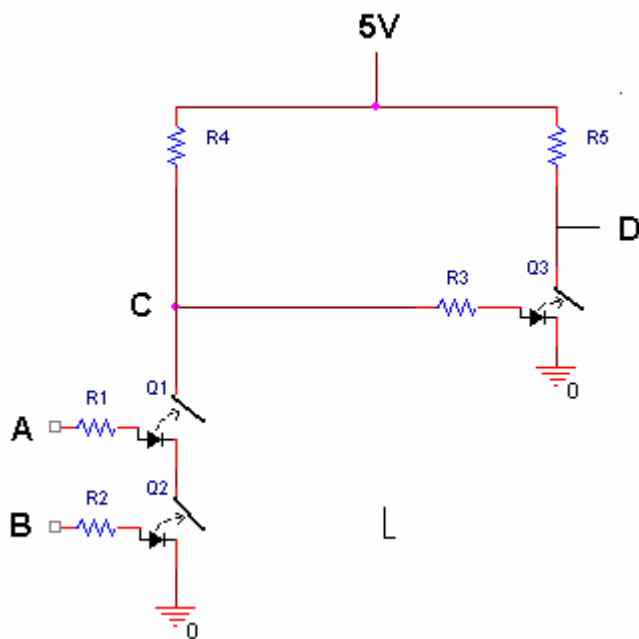
c) In terms of Vs, what is the range of the analog output for a 4 bit binary input? (ie. If the input ranges from 0000 to 1111, what is the output range?) *(2 points)*

The range of outputs is from 0 volts to –(15/16)Vs.

Question 5) Transistors (20 points)

a) Redraw the figure above with the transistors modeled as a switch and a diode. (*7 points*)

c) Fill in the following table of C and D as a function of A and B based on the model you gave in part a). *(8 points)*

A	B	C	D
0V	0V	*5V*	*0V*
0V	5V	*5V*	*0V*
5V	0V	*5V*	*0V*
5V	5V	*0V*	*5V*

b) If we assume the output of this gate is measured at D, what kind of gate is it? *(5 points)*

    a. *AND*
    b. NAND
    c. OR
    d. NOR
    e. XOR
    f. None of the above