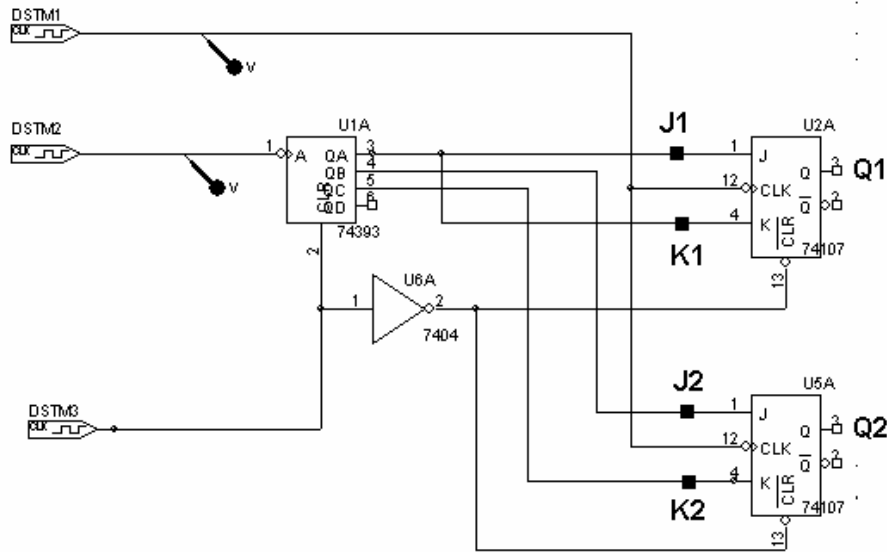
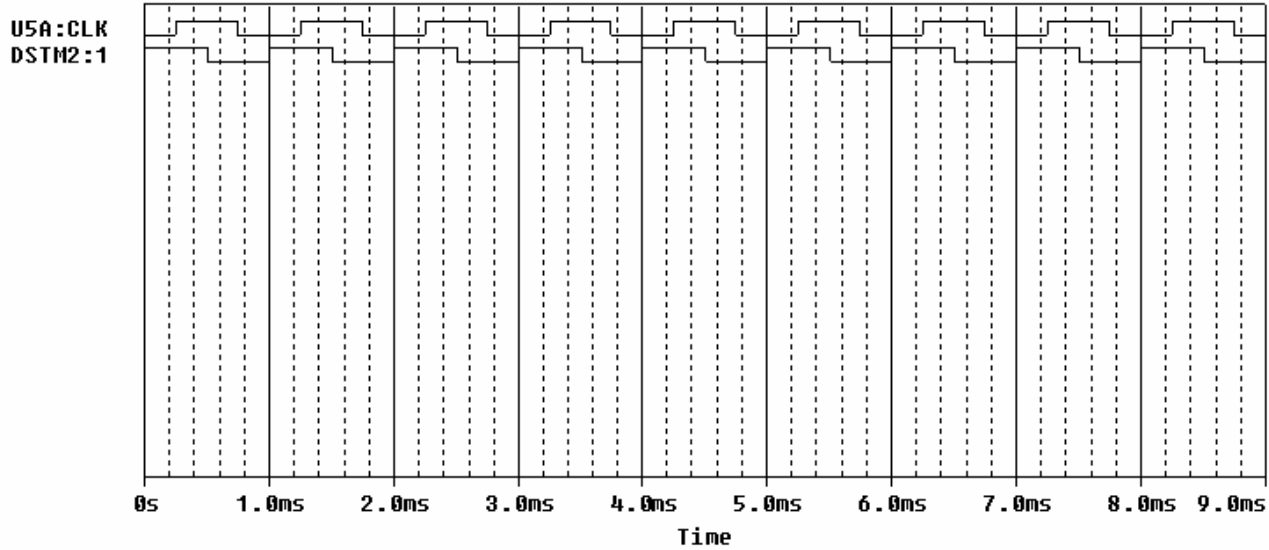


**Question 1 -- Flip Flops and Counters (20 points)**



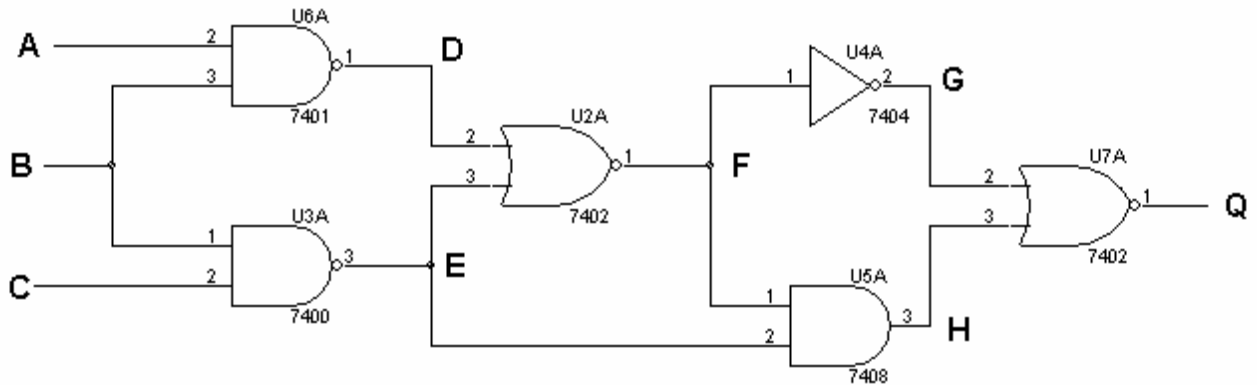
a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (flip flop clock), the second trace shown is DSTM2 (counter clock), and DSTM3 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0 and that all three devices change on the falling edge of the clock.. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2)

(3 points each = 18 points)



b) To what value does the counter count in the time frame indicated? (2 points)

**Question 2 – Logic Gates (20 points)**



a) Fill in the truth table for the circuit above: (12 points)

A	B	C	D	E	F	G	H	Q
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

b) Write the Boolean expression for the circuit in a). Do not simplify. (6 points)

c) What type of gate could the above circuit be replaced with to give the same results for Q based on A, B and C? (2 points)

- 1) Three input AND gate
- 2) Three input OR gate
- 3) Three input NOR gate
- 4) Three input NAND gate
- 5) none of the above

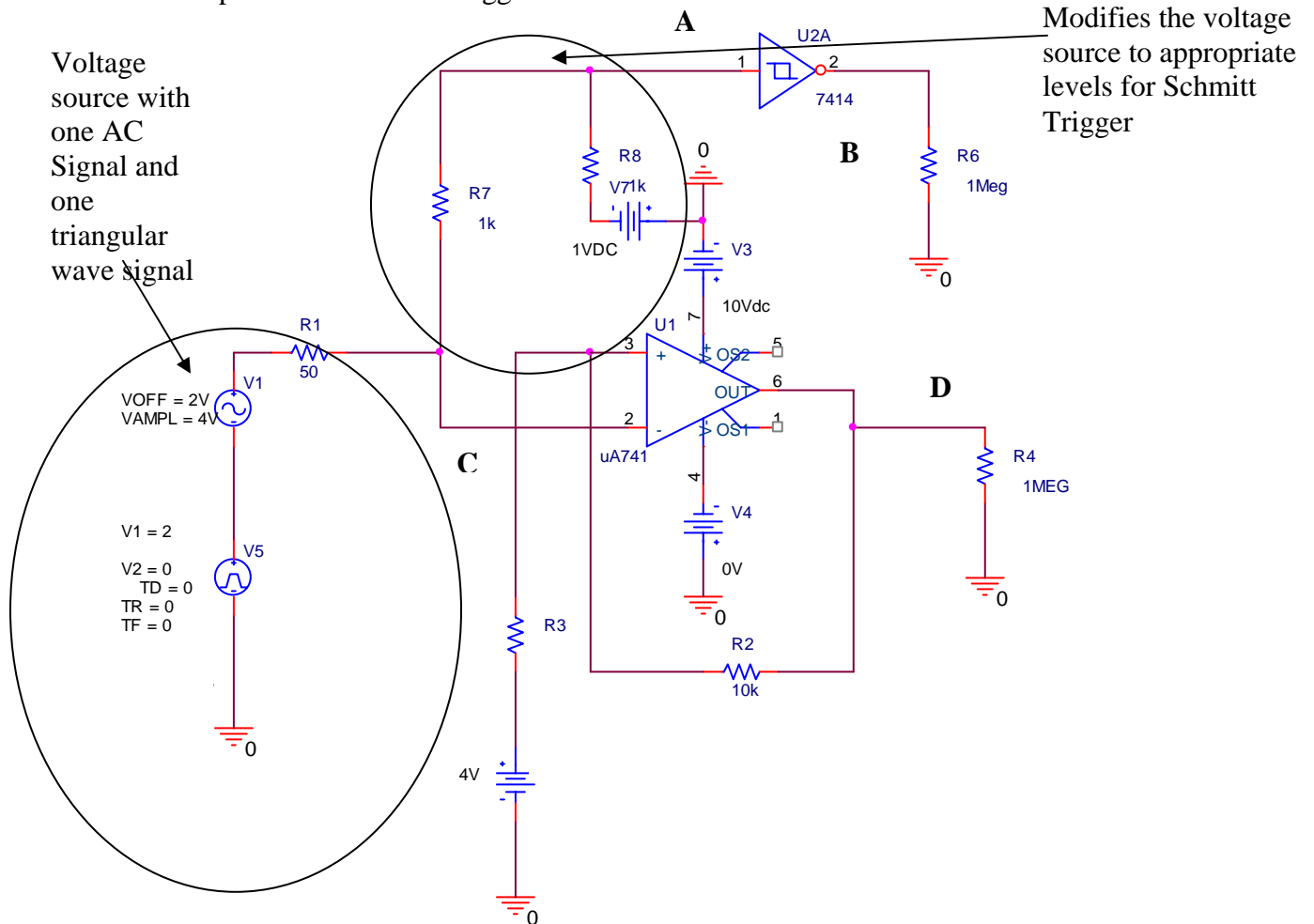
Name: \_\_\_\_\_

Section \_\_\_\_\_

Extra credit (*1 point*): Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.

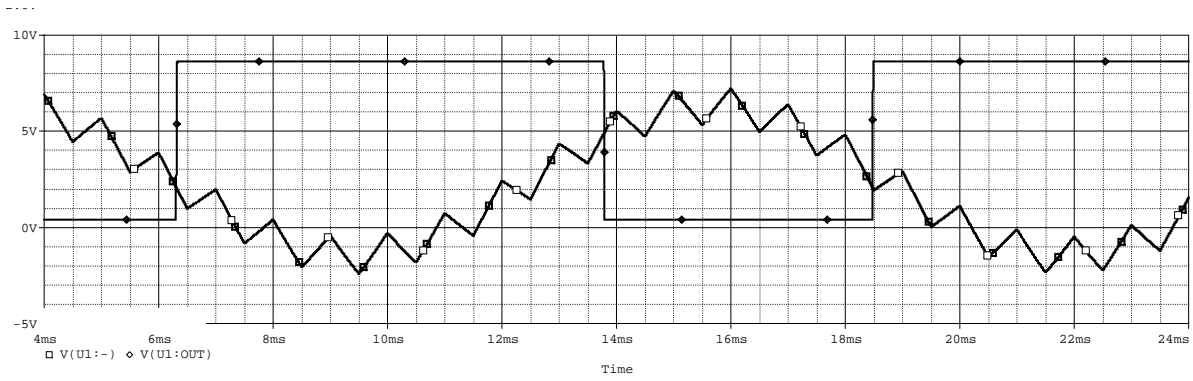
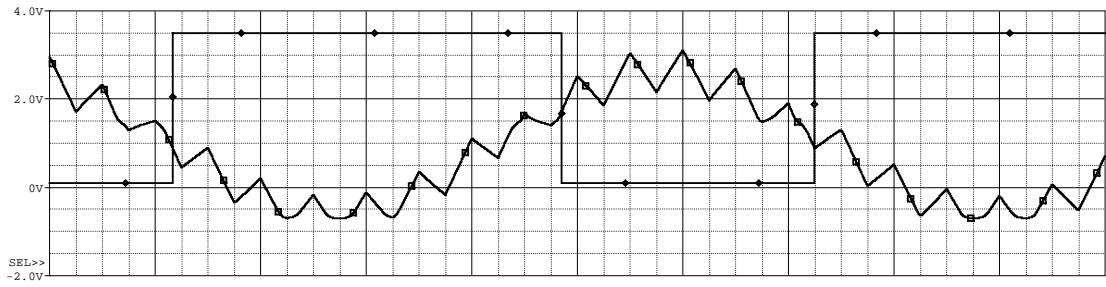
### 3. Schmitt Trigger

The following circuit was configured to study Schmitt Triggers. It includes the Schmitt trigger device (7414) we studied in Experiment 10 and the op-amp configuration assembled to produce a Schmitt Trigger circuit.



The voltage source is a combination of two sources – one is sinusoidal and one is a triangular wave. The latter source has the higher frequency. The voltage levels for the op-amp Schmitt Trigger circuit are higher than for the commercial Schmitt Trigger. Thus, two resistors and a voltage source are used to change the input voltages to levels appropriate for a logic circuit. Note that we are also operating the op-amp in an unbalanced mode with the negative voltage source set to zero.

The voltage signals measured at points **A**, **B**, **C**, & **D** in the circuit look like:



The voltage scale on the bottom plot ranges from -5 to 10 Volts, while the scale on the top plot varies from -2 to 4 Volts.

- a. Label each of the four signals with the letter **A**, **B**, **C**, or **D** indicating where it is measured. (4 points)
  
- b. What are the frequencies for both sources? (4 points)
  
- c. At what voltages do the two circuits switch output states? (8 points)

Top plot (Low to High):

Top plot (High to Low):

Bottom Plot (Low to High):

Bottom plot (High to Low):

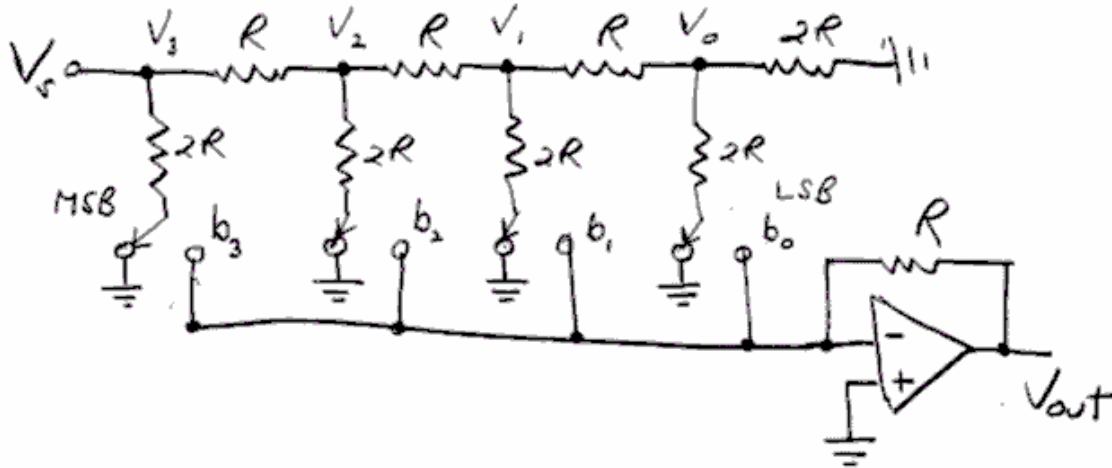
Name: \_\_\_\_\_

Section \_\_\_\_\_

- d. Assuming, as is shown, that  $R_2 = 10\text{k Ohms}$ , what must the value of  $R_3$  be to cause the output measured across  $R_4$  to switch at these voltages? (*4 points*)

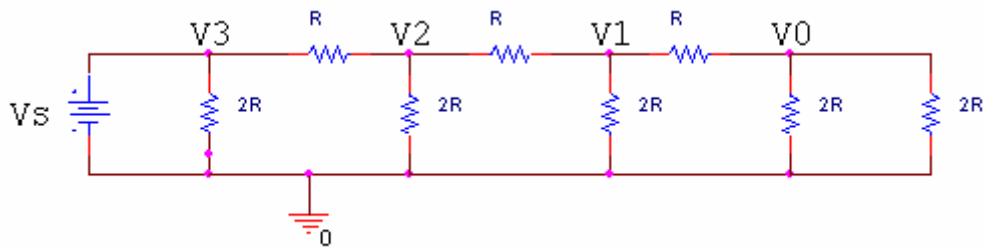
**Question 4 -- Digital-to-Analog Converter (20 points)**

For a computer or other digital device to interface with external analog circuits and devices, a digital-to-analog converter (DAC) is required. The most common DAC is a R-2R resistor ladder network, which requires only two precision resistor values R and 2R. A 4-bit R-2R resistor ladder network is shown below:



The digital input to the DAC is a 4-bit binary number represented by bits  $b_0$ ,  $b_1$ ,  $b_2$  and  $b_3$ , where  $b_0$  is the least significant bit (LSB) and  $b_3$  is the most significant bit (MSB). Each bit in the circuit controls a switch between ground and the *inverting* input op amp. When a bit is 1, the corresponding switch is connected to the op-amp; when a bit is zero, the corresponding switch is connected to ground.

a) If we assume this is an ideal op-amp, we can analyze the voltage levels in the circuit by removing the op amp. Below is a picture of the circuit when all bits are zero. Use the simplified circuit below to determine the voltage levels at  $V_0$ ,  $V_1$ ,  $V_2$  and  $V_3$  in terms of the source voltage,  $V_s$ . (8 points)



b) If we assume that closing switches has negligible effect on the voltage levels we found in part a), what will be the output of the DAC circuit,  $V_{out}$  (in terms of  $V_s$ ), when the input ( $b_3 b_2 b_1 b_0$ ) is: (*10 points*)

0001:

0010:

0100:

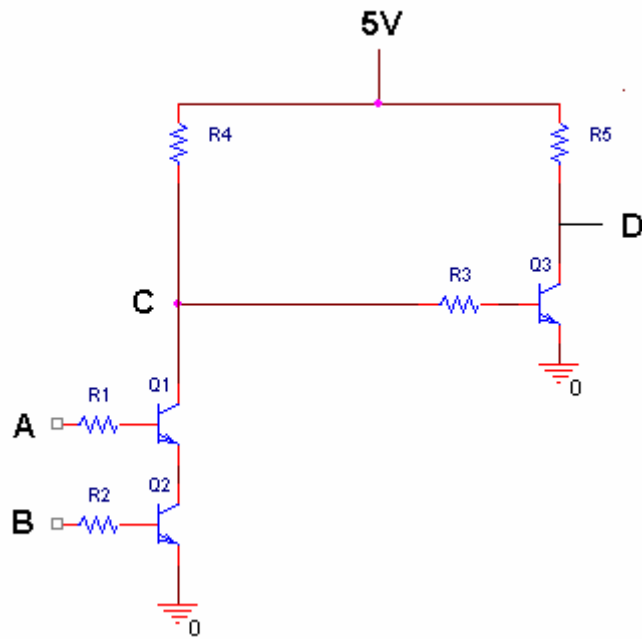
1000:

1111: [Hint: Use principal of superposition.]

c) In terms of  $V_s$ , what is the range of the analog output for a 4 bit binary input? (ie. If the input ranges from 0000 to 1111, what is the output range?) (*2 points*)



**Question 5) Transistors (20 points)**



- a) Redraw the figure above with the transistors modeled as a switch and a diode. (7 points)

Name: \_\_\_\_\_

Section \_\_\_\_\_

c) Fill in the following table of C and D as a function of A and B based on the model you gave in part a). (8 points)

A	B	C	D
0V	0V		
0V	5V		
5V	0V		
5V	5V		

- b) If we assume the output of this gate is measured at D, what kind of gate is it? (5 points)
- AND
  - NAND
  - OR
  - NOR
  - XOR
  - None of the above