ENGR-4300
Spring 2008
Test 4 Conflict

Name _______SOLUTION_______

Section 1(MR 8:00) 2(TF 2:00) 3(MR 6:00)
(circle one)

Question I (24 points) ___________

Question II (16 points) ___________

Question III (15 points) ___________

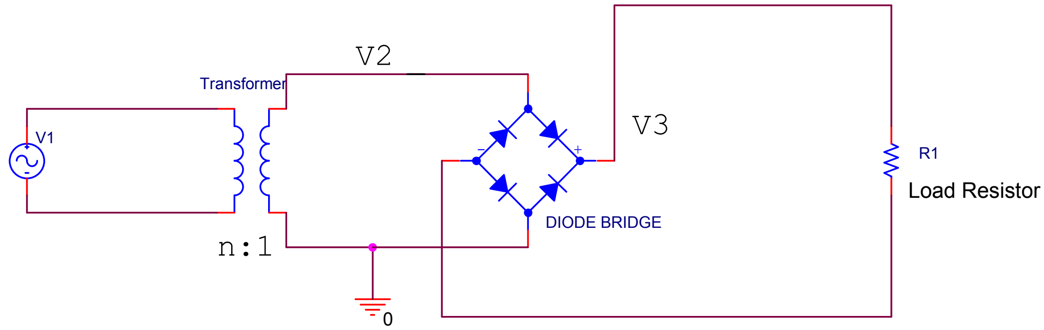
Question IV (20 points) ___________

Question V (25 points) ___________

Total (100 points): ______________

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question I – Diode Rectifier Circuits (24 points)



The diagram above shows the application of a diode bridge for performing rectification of the voltage from the output of the transformer. The sinusoidal source voltage V1 = $240V_{RMS}$ and R1 = 5kΩ.

1. (4pt) Knowing that the voltage amplitude is $\sqrt{2}$ larger than the RMS voltage, what transformer turns ratio n:1 will give as close as possible to an 8V amplitude at V2? (n should be rounded to an integer.)

n = (240 x 1.414)/8 = 42.42 => 42 n:1 = 42:1

2. (4pt) What will the actual peak voltage be on the output of the full wave bridge (across R1). Let the idealized diodes have V_{on} = 0.6V and V2 is the voltage from the turns ratio in question 1?

V = (240 x 1.414)/42 – 2x(0.6) = 6.88V

3. (3pt) Given R1 above, what is the peak current that will flow through any of the 4 diodes?

I = V/R = 6.88/5k = 1.38mA

Question I – Diode Rectifier Circuits (continued)

4. (4pt) For a 60Hz input voltage V1 a capacitor is added in parallel with R1 to reduce the ripple in the voltage across the load resistance so that the droop is less than 0.7V. Which of the following values is the minimum capacitance necessary to achieve this?

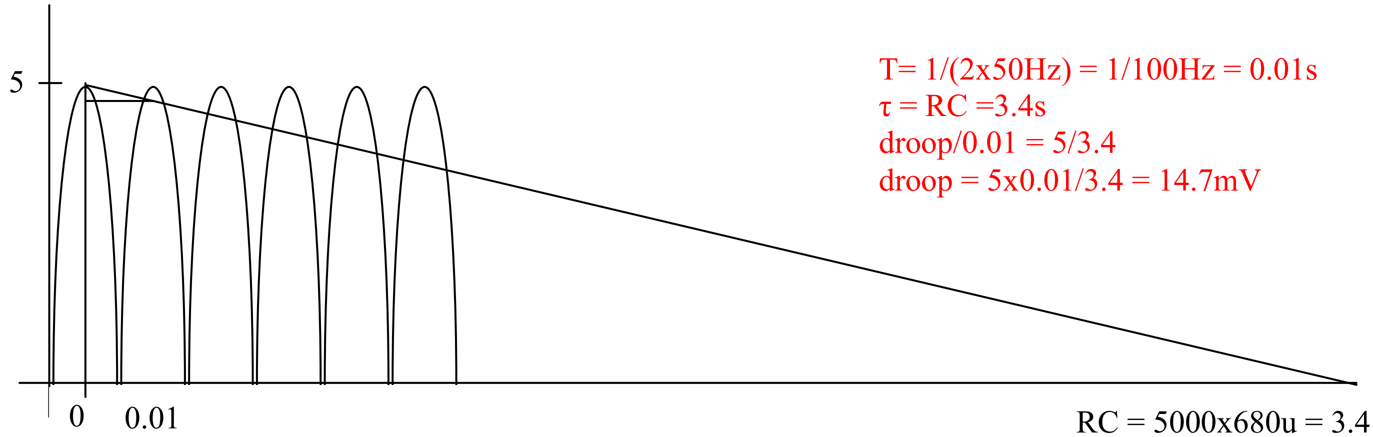
a) 1μF b) 17μF c) 33μF d) 100μF

Droop = 0.7/6.88 = 0.10
T = 1/120Hz = 8.3ms
τ = RC = 0.0083/0.10 = 0.083 C > 0.083/5000 = 16.6μF

5. (3pt) It is decided to use a 680μF capacitor to filter the supply voltage. What 3 digit code will be written on this capacitor to indicate its value?

687 => 68 x 10^7pF = 68 x 10^7 x 10^{-12} = 68 x 10^{-5} = 0.00068F

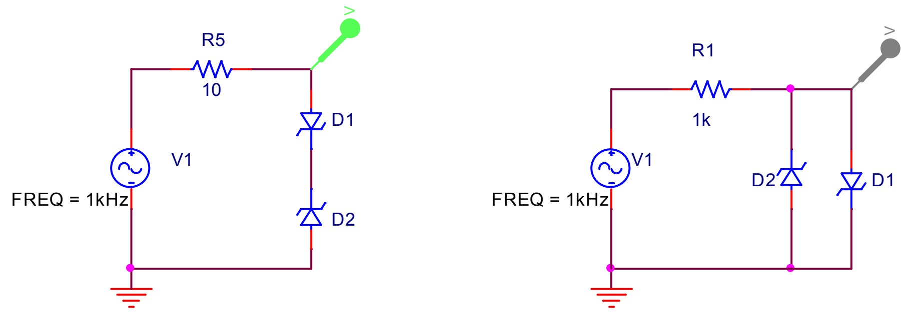
6. (6pt) For a quick calculation of the voltage droop with the 680μF capacitor and 5kΩ load resistance, assume a 5V amplitude 50Hz sine wave has been ideally full wave rectified (V_{on} = 0V). Use the period between adjacent peaks as the maximum droop time and assume the exponential decay can still be modeled as a straight line in this interval. With these simplifications, how much will the voltage droop from its 5V maximum value?



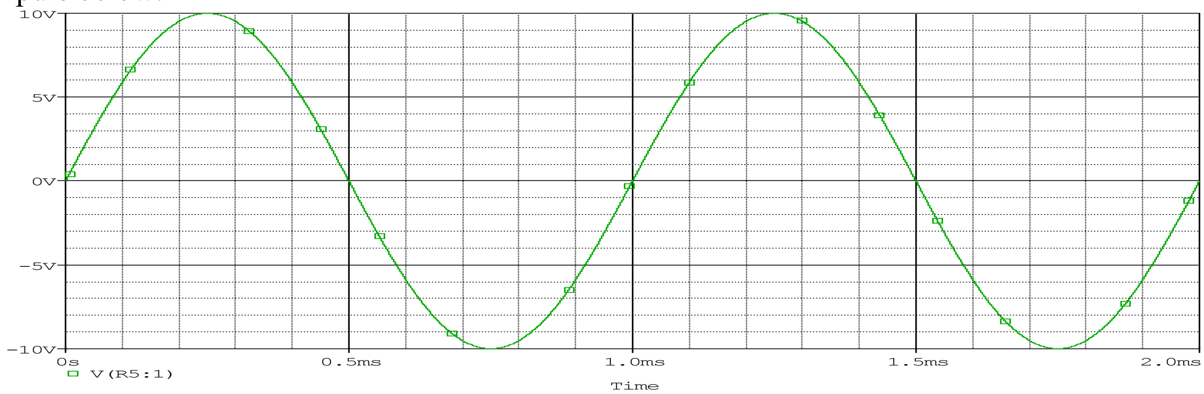
T= 1/(2x50Hz) = 1/100Hz = 0.01s
τ = RC =3.4s
droop/0.01 = 5/3.4
droop = 5x0.01/3.4 = 14.7mV

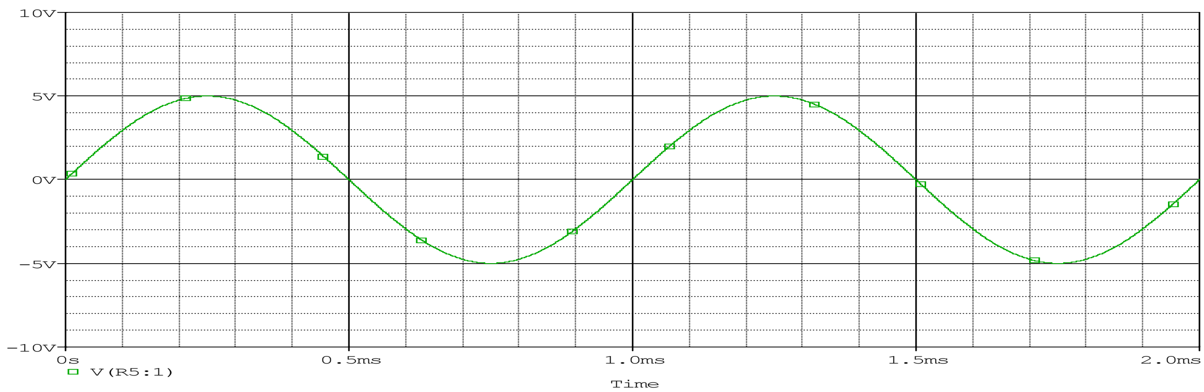
Question II – Zener Diode Circuits (16 points)

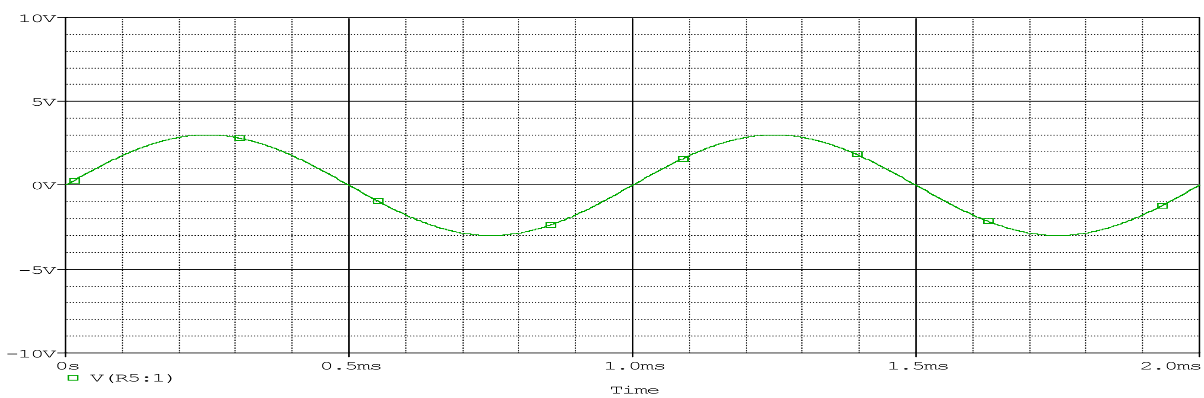
Below are 2 Zener diode limiter circuits. Vz = 3V for D1 and Vz = 8V for D2.



1. (6pt) For the left-hand circuit, on the axes below sketch the output voltage at the probe for the 3 inputs below.

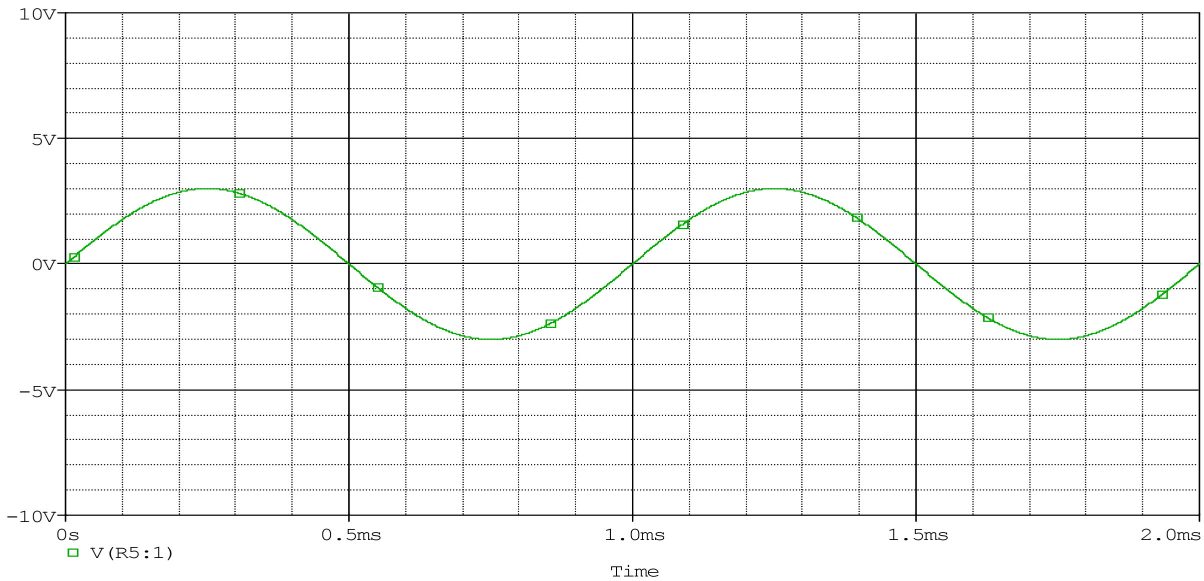


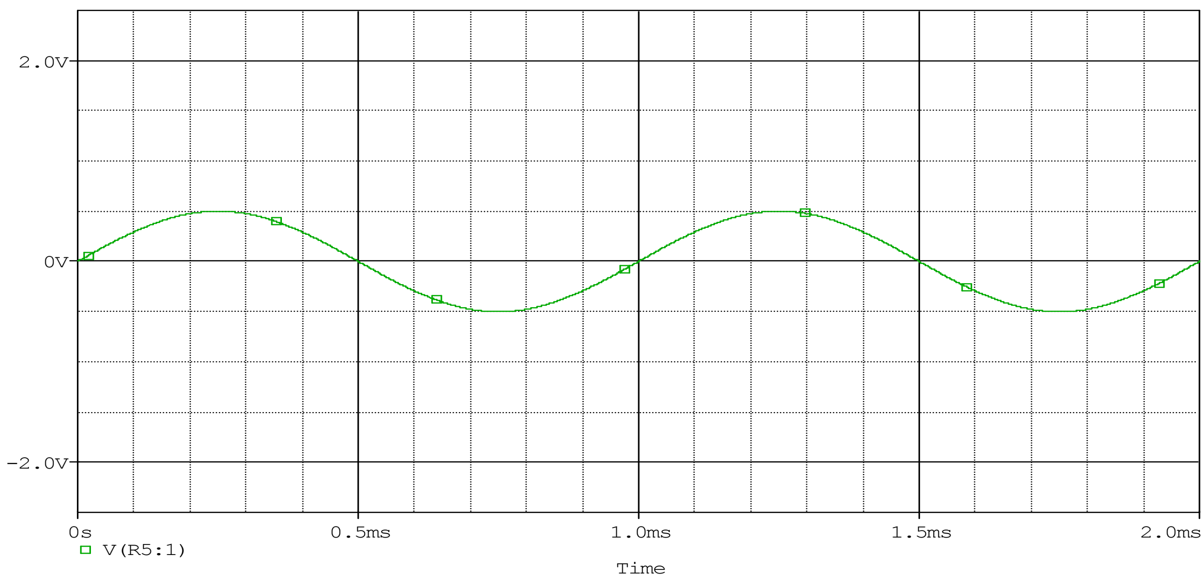




Question II – Zener Diode Circuits (continued)

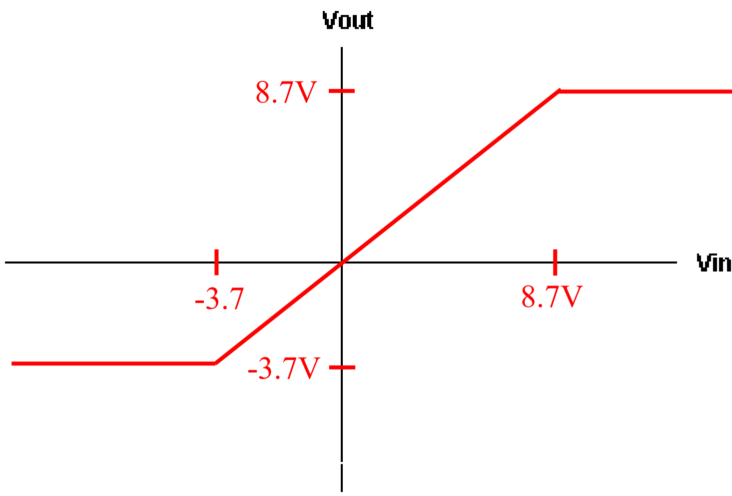
2. (4pt) For the right-hand circuit, on the axes below sketch the output voltage at the probe for the 2 inputs below.





Question II – Zener Diode Circuits (continued)

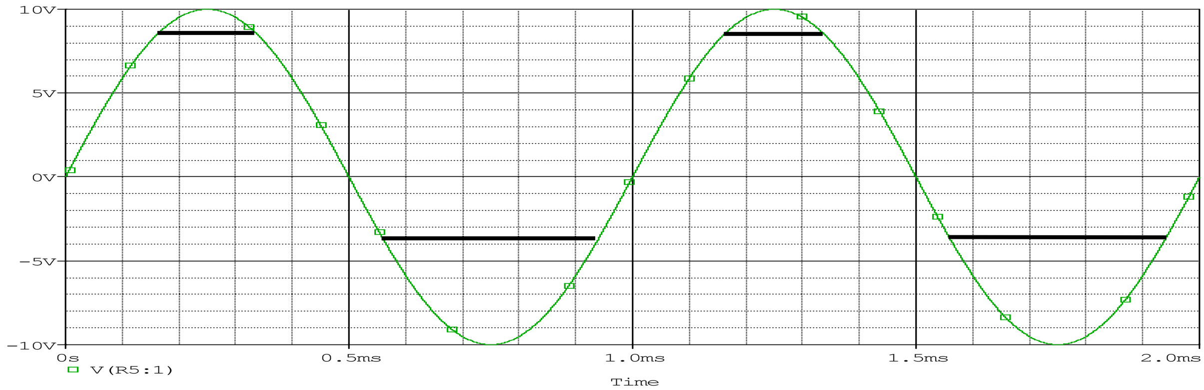
3. (4pt) Sketch the voltage input-output curve for the left-hand circuit above. Be sure to scale the axes.



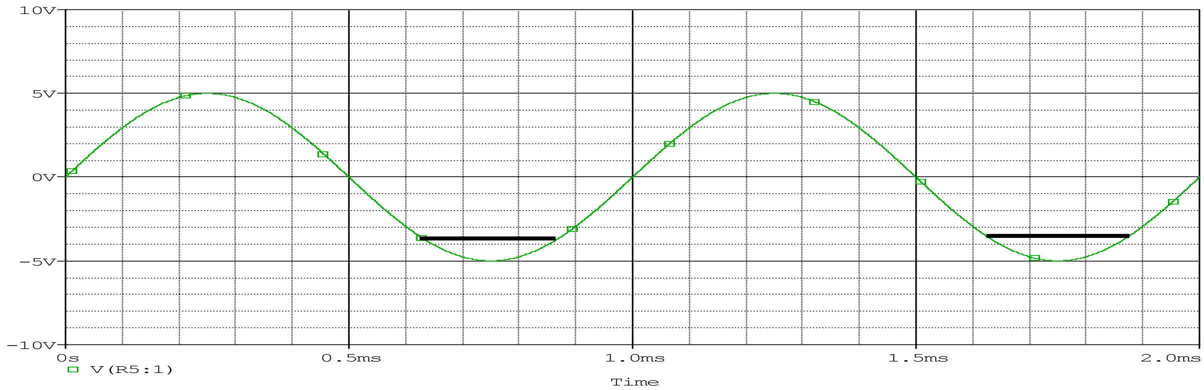
$V^+ = 8 + 0.7 = +8.7V$ $V^- = -3 - 0.7 = -3.7V$

4. (2pt) TRUE or FALSE: A full wave bridge rectifier with all the diodes replaced with Zener diodes (Vz = 5V) would still be able to rectify a 6.4V amplitude input sine wave (V2 on the circuit in question I-1) with the same output waveform as with regular diodes (assuming the V_{on} voltages are all 0.7V).

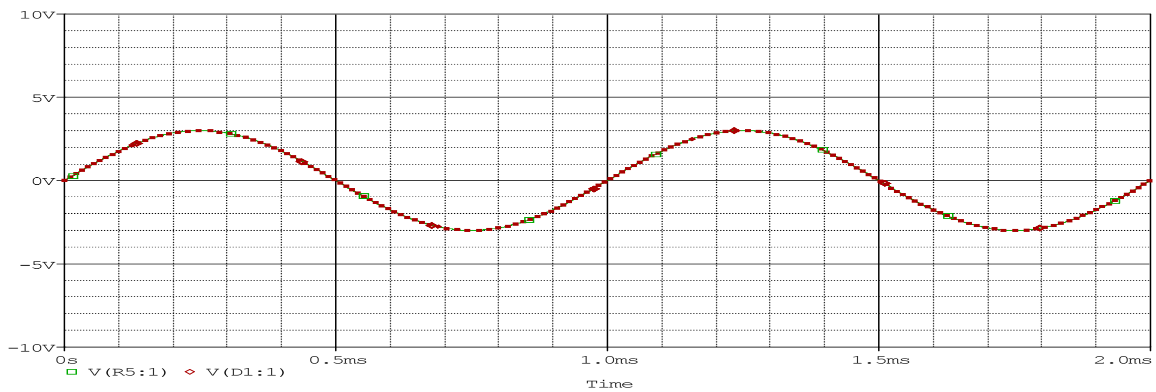
Input amplitude must < 5 +0.7 = 5.7V



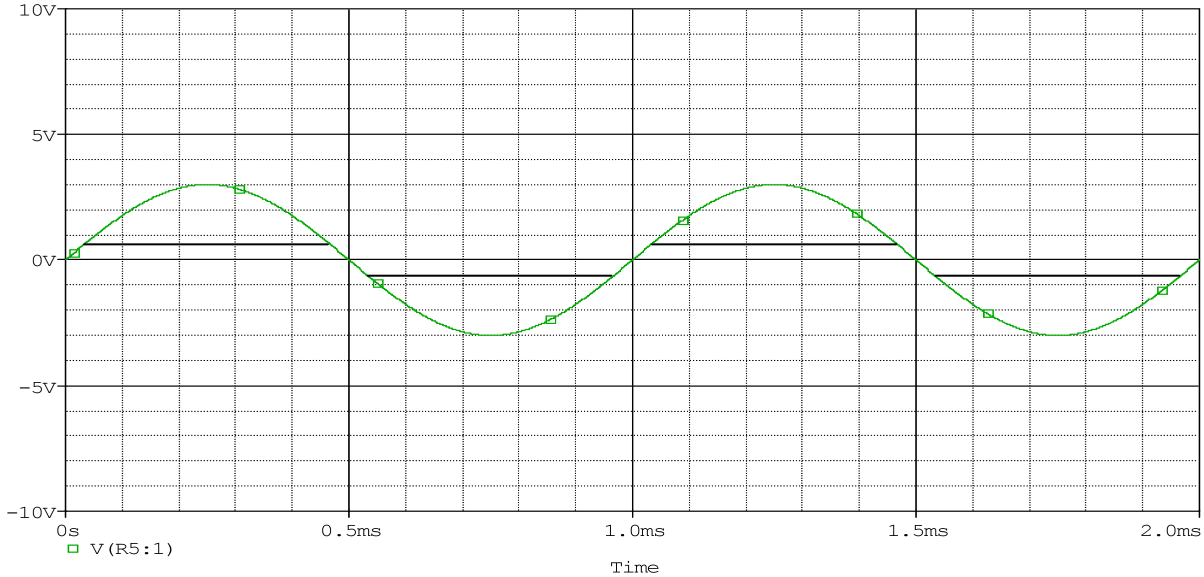
Clipped at 8 + 0.7 = +8.7V and -3 – 0.7 = -3.7V



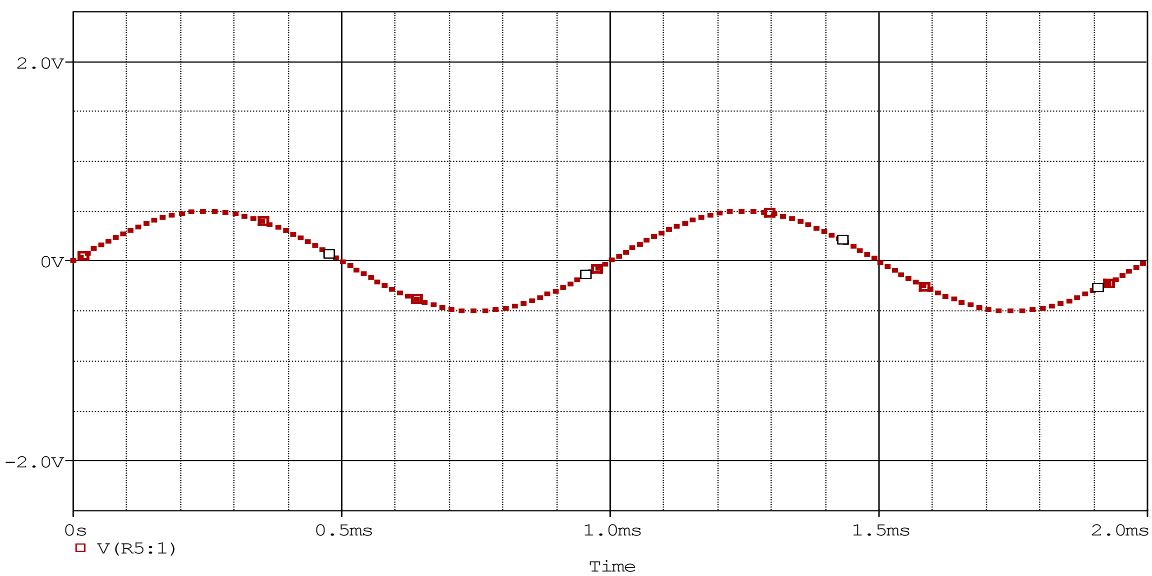
Clipped only at -3 - 0.7 = -3.7V



No clipping

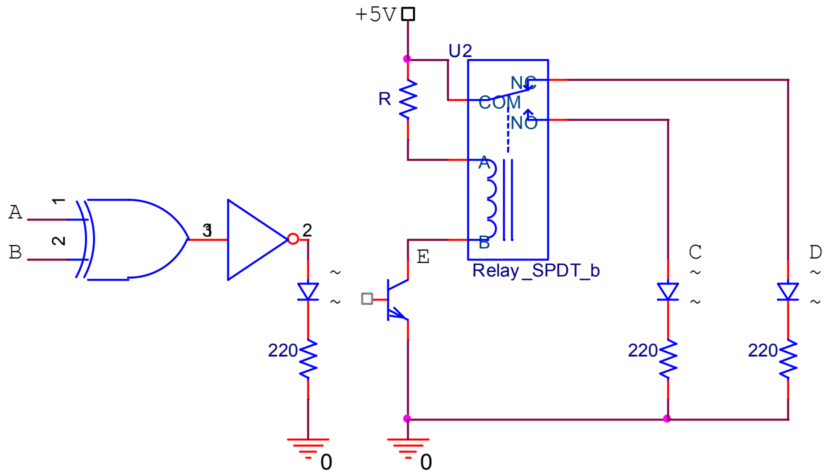


Clipping at +0.7V and -0.7V



No clipping

Question III – LEDs and Phototransistor Circuits (15 points)



Above is a typical optical isolation circuit with an LED/phototransistor pair. The logic gate and inputs may be in a cage whose reference voltage is 5kV higher than the phototransistor and relay circuit, but the "optical isolation" removes the danger of high voltage getting through.

1. (6pt) Fill in the following table:

A	B	Relay (on or off?)	LED C (on or off?)	LED D (on or off?)
0	0	ON	ON	OFF
0	1	OFF	OFF	ON
1	0	OFF	OFF	ON
1	1	ON	ON	OFF

2. (5pt) Assuming the resistance of the relay coil is negligible but 100mA is needed to turn it on, what is the maximum resistance value R can be if the on-resistance of the phototransistor is 20Ω?

Answer: 5V/100mA = 20 + R *R = 5/0.2 – 20 = 30Ω*

3. (4pt) Using the phototransistor on-resistance of 20Ω, setting R = 15Ω and assuming the phototransistor behaves like an ideal switch when it is turned off, what are the minimum and maximum voltages at E, the collector of the transistor?

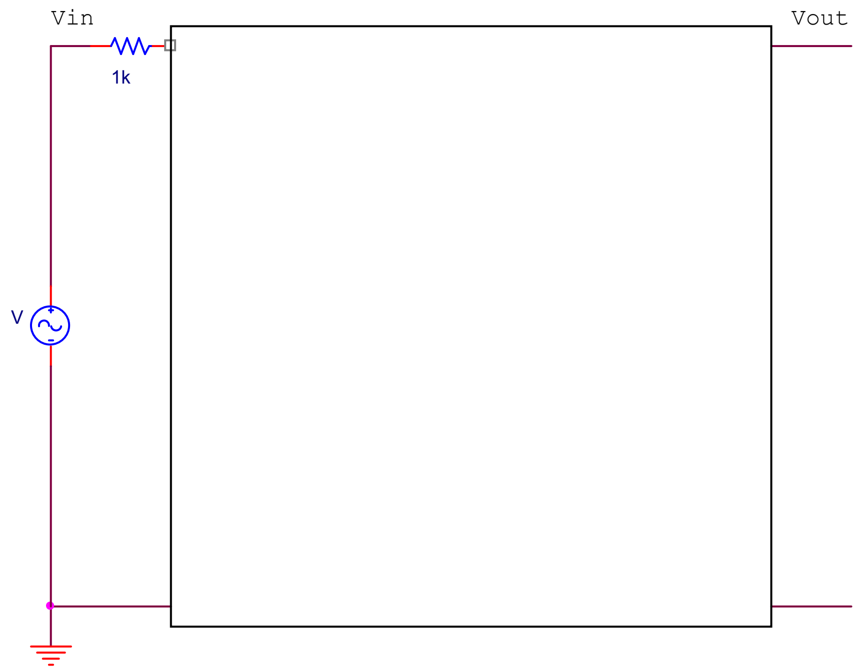
Answer:

$$Minimum = 5\frac{20}{20+15} = 5\frac{20}{35} = 2.86V$$

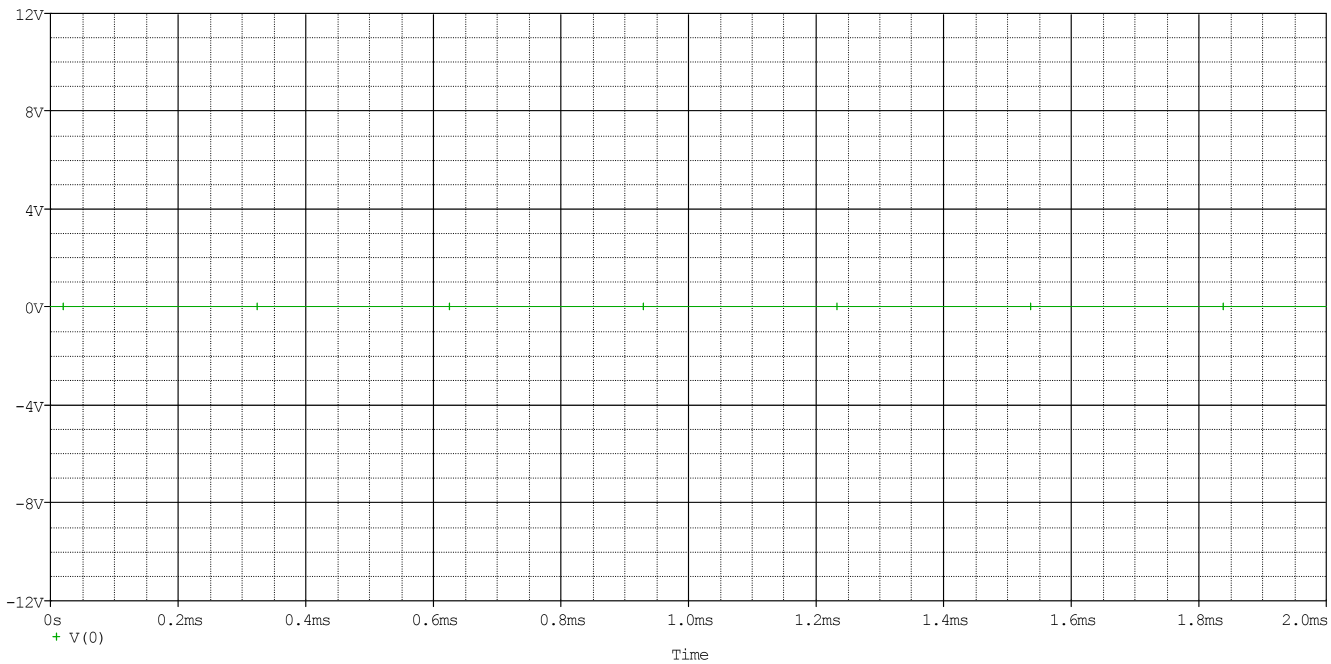
$$Maximum = 5V$$

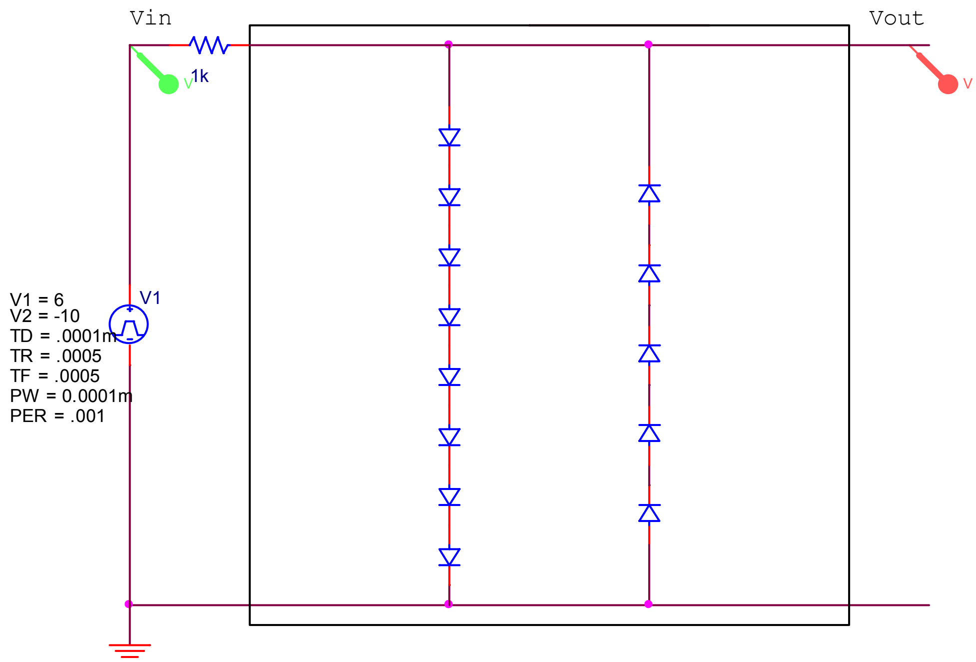
Question IV - Diode Limiter Circuits (20 points)

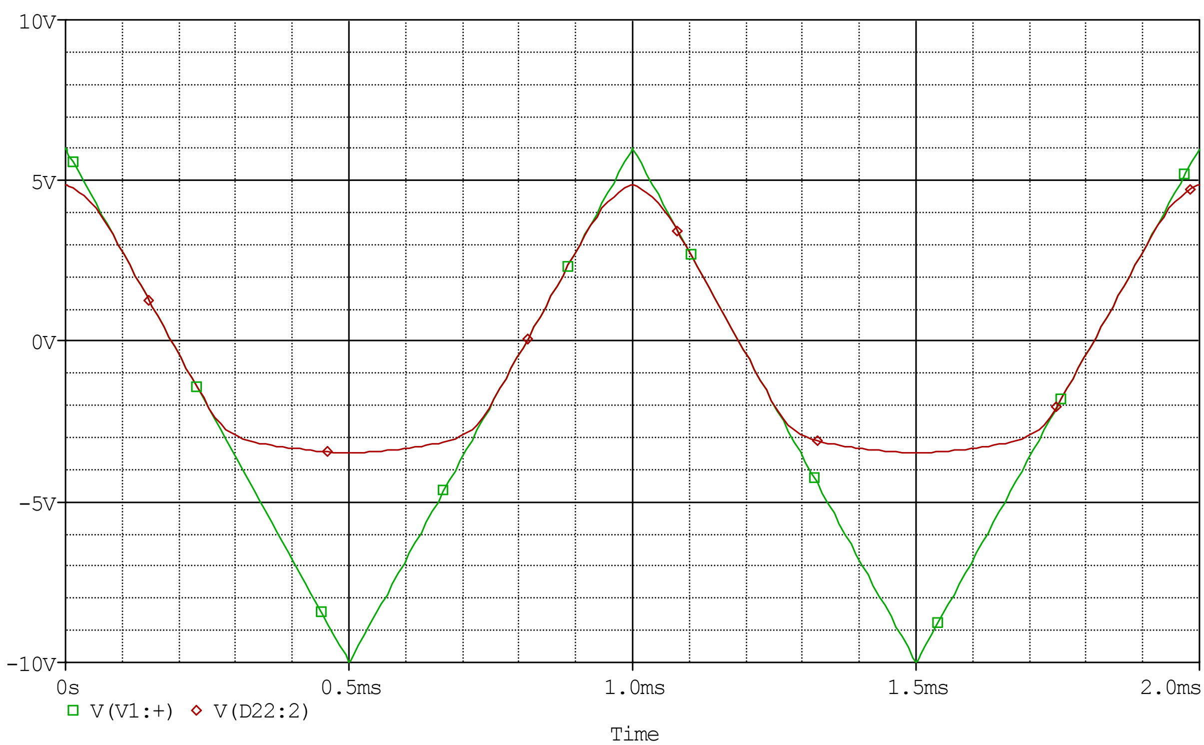
1 (6pt) Design a diode limiter circuit in the square, using stacked series standard Silicon diodes, that limits Vout to a maximum of +5.6V and a minimum of -3.5V.



2. (4pt) Sketch Vin and Vout when Vin is a 1kHz triangle wave with an 8V amplitude and a -2V offset.







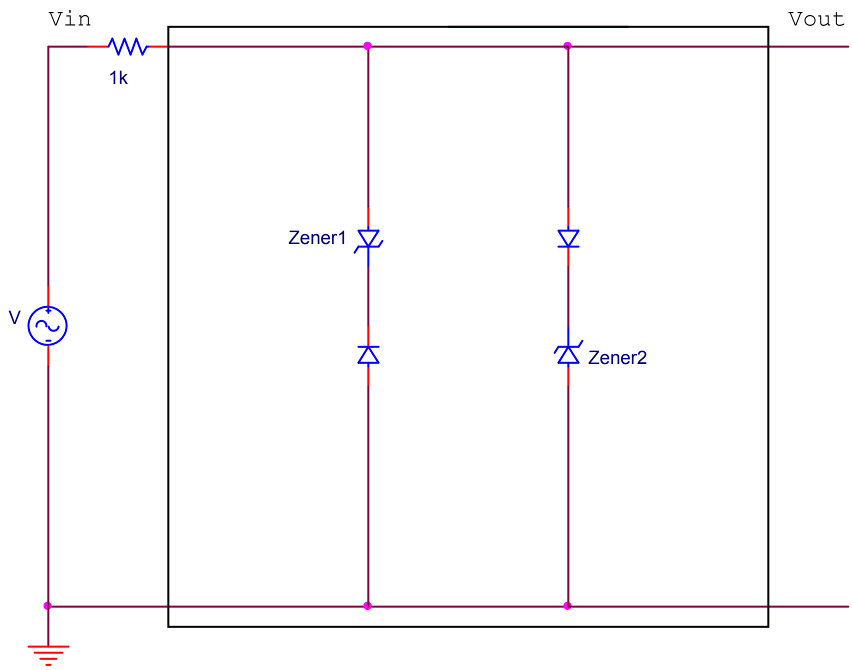
Approximate answers will be flat clipped at +5.6V and -3.5V

Question IV - Diode Limiter Circuits (continued)

3. (4pt) If all the diodes in this limiter circuit were replaced with diodes whose forward bias voltages (V_{on}) are 0.6V, what would the maximum and minimum output voltages become?

Vmax = 5 x 0.6 = +3.0V
Vmin = -8 x 0.6 = -4.8V

4. (6pt) Can the circuit below, with appropriate values for Vz, be made to match the requirements in question IV-1? If not, explain why not. If so, what values are needed as Vz for Zener 1 and Zener 2? V_{on} for all diodes is the same as in IV-1 above.

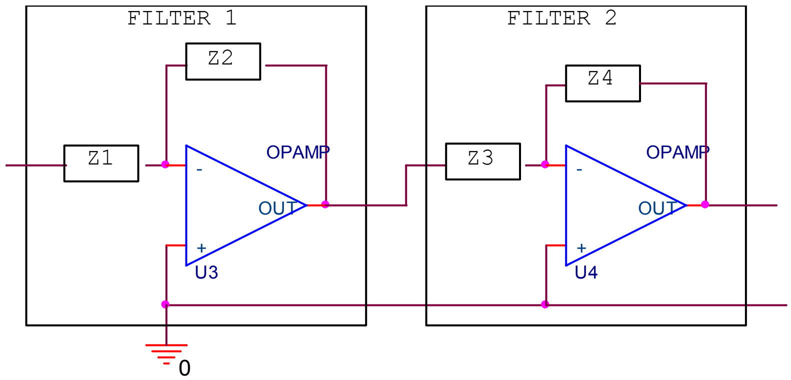


Yes:

+5.6V = Vz2 + 0.7V   Vz2 = 4.9V
-3.5V = -Vz1 – 0.7V   Vz1 = 2.8V

Question V – Signal Modulation and Filtering (25 points)

A modulated signal is to be filtered to remove the effects of the modulation and other noise. The desired signal is from 100Hz – 8kHz. The undesired parts of the signal are below 50Hz and above 10kHz. Design a combination of filter types (low pass and/or high pass) that will remove everything except the desired signal. It has been decided that the filters should be in series (cascaded) as shown below. The Zs in the op-amp circuits represent complex impedances and may be combinations of resistors and capacitors. (Hint: one of these filters was used in Project 4.)



1. (4pt) For each filter determine the appropriate type.

Filter 1: ___LOW PASS_________ Filter 2: ___HIGH PASS_________

Order of filters may be switched around

2. (6pt) For each filter determine the corner frequency.

Filter 1 f_c: ___~9kHz_________ Filter 2 f_c: ___~70Hz_____________

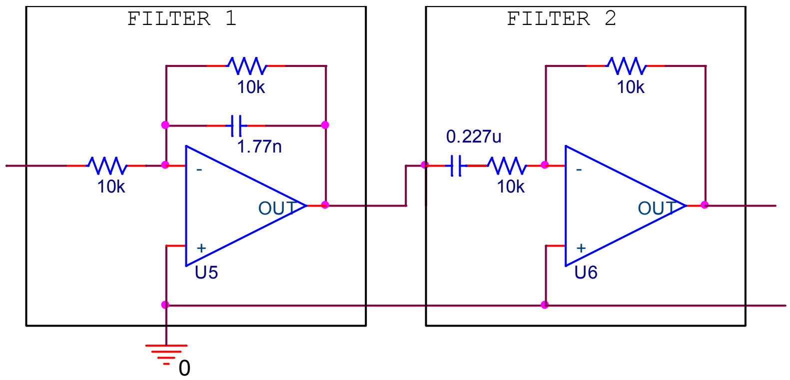
8kHz – 10kHz OK 50Hz – 100Hz OK

Question V – Signal Modulation and Filtering (continued)

3. (8pt) Using 10kΩ resistors and whatever capacitor values are necessary, draw the circuits for Filter 1 and Filter 2 with the correct components replacing the Zs above.

LPF Filter 1: $\omega = 2\pi f = \frac{1}{R_f C_f} \Rightarrow C_f = \frac{1}{R_f 2\pi f} = \frac{1}{10{,}000 \cdot 2\pi 9k} = 1.77nF$

HPF Filter 2: $\omega = 2\pi f = \frac{1}{R_i C_i} \Rightarrow C_i = \frac{1}{R_i 2\pi f} = \frac{1}{10{,}000 \cdot 2\pi 70} = 0.227\mu F$



4. (4pt) Write down the transfer function, H(jω), for each filter with numerical values for the coefficients.

LPF Filter 1:

$$H(j\omega) = -\frac{R_f}{R_i(1 + j\omega R_f C_f)}$$

$$= -\frac{1}{1 + j\omega 17.7x10^{-6}}$$

HPF Filter 2:

$$H(j\omega) = -\frac{j\omega R_f C_i}{1 + j\omega R_i C_i}$$

$$= -\frac{j\omega 2.27x10^{-3}}{1 + j\omega 2.27x10^{-3}}$$

5. (3pt) Which type of filters, Miller integrators or practical differentiators, have problems due to inherent noise in signals?

Practical Differentiators: they greatly amplify high frequency noise