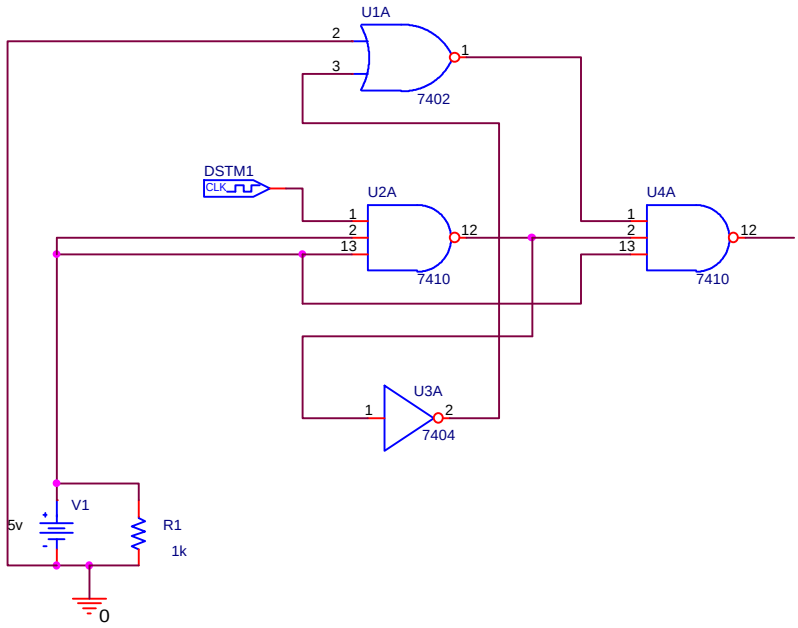
Quiz 4 – Fall 1998
Answers

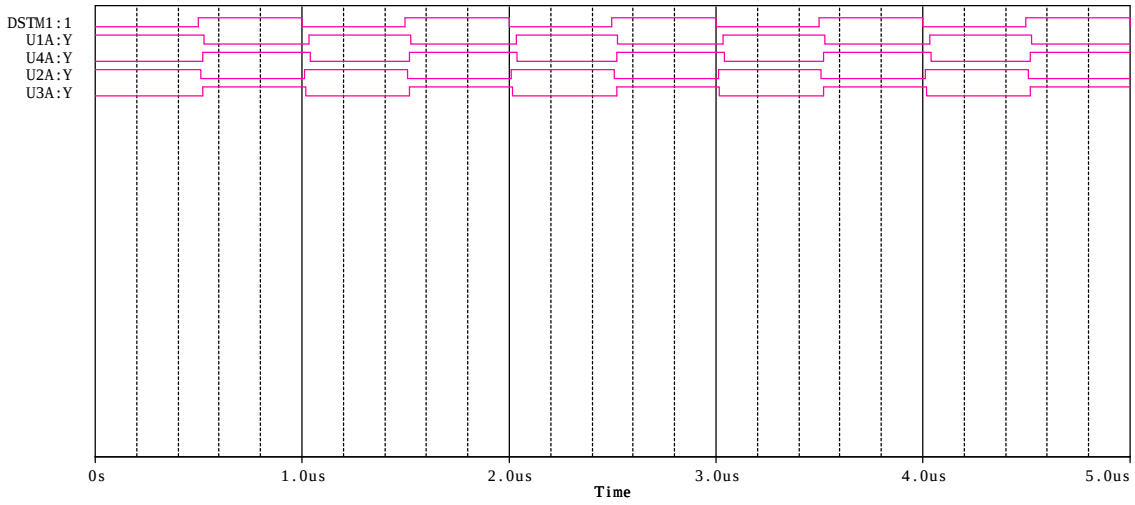
1. Logic Gates



In this circuit, there is a NOR gate (U1), two NAND gates (U2 & U4) and an invertor (U3). Input 2 to the NOR is LO, inputs 2 and 13 to the first NAND are HI, input 1 of the first NAND goes HI and LO (clock), the input to the invertor is the output from the NAND, the output from the invertor is input 3 of the NOR, input 13 of the last NAND is HI, input 2 is the output from the first NAND and input 1 is the output from the NOR.

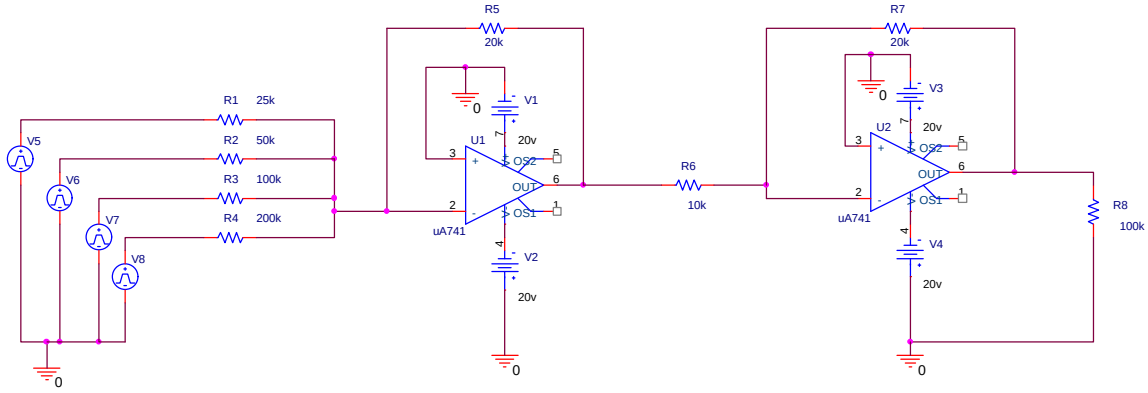
U1-2	U1-3	U2-1	U2-2	U2-13	U3-1	U4-1	U4-2	U4-13	U4-12
0	0	0	1	1	1	1	1	1	0
1	1	1	1	1	0	0	0	1	1

The correct simulation (not in the same order as in the quiz) is

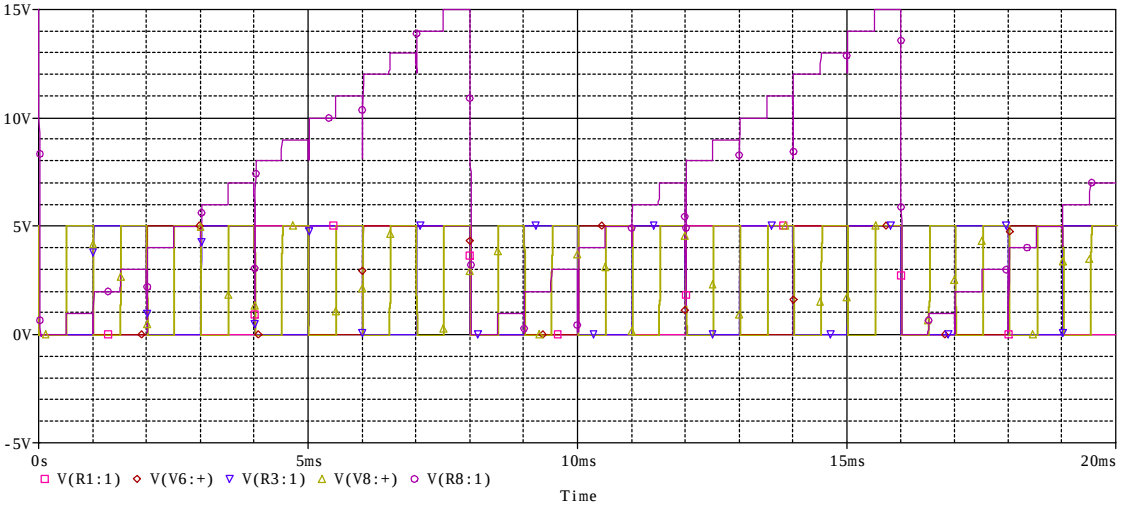


2. Digital-to-Analog Convertor

The configuration shown is one of the two types of DACs discussed in the write up linked from the discussion of quiz 4 on our main web page. Be sure that you read this through. For the conditions given (inputs of 0 and 5 volts) this circuit will convert the digital number ABCD to a decimal number if the configuration looks like the following:



To show that this works, the pulse sources at the left were configured to count from 0 to 15 with the inputs and outputs shown.



You can see that it does indeed count from 0 to 15 as it should for TTL input levels.

3. Combinational Logic

To do a problem like this, label every single input and output and then generate the truth table. The correct answer is the third table.

4. NAND Gate Logic

This combination makes an XOR (see page 18 of the Radio Shack book on Digital Logic). The method is the same as for question 3.

5. Transistor Switch

When the voltage to the base is small, the switch will be open. Then the voltage across the load resistor (R5) should be half the power voltage (9v) or 4.5v. After the base voltage is high enough to turn on the transistor, the voltage should drop to near zero. Thus, the very last case is the correct one.