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$\qquad$
Questions about Logic Gates
Fall 2004
Question 2: NAND Gate Circuit (16 points)
Below is a picture of a series of NAND gates hooked together to form one of the basic gates we have studied and the PSpice output for the circuit

a) Fill in the truth table for the circuit (10 points)

| A | B | C | D | E | F | G |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 |  |  |  |  |  |
| 0 | 1 |  |  |  |  |  |
| 1 | 0 |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |

b) This circuit is a model for one of the gates we have seen in class. What single gate does it represent (2 points)?
c) Write a boolean expression for this circuit. Do not simplify. (4 points)
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Fall 2004 Solution (not available)
$\qquad$ Section $\qquad$

## Spring 2004

Question 2 - Logic Gates (20 points)

a) Fill in the truth table for the circuit above: (12 points)

| A | B | C | D | E | F | G | H | Q |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 |  |  |  |  |  |  |
| 0 | 0 | 1 |  |  |  |  |  |  |
| 0 | 1 | 0 |  |  |  |  |  |  |
| 0 | 1 | 1 |  |  |  |  |  |  |
| 1 | 0 | 0 |  |  |  |  |  |  |
| 1 | 0 | 1 |  |  |  |  |  |  |
| 1 | 1 | 0 |  |  |  |  |  |  |
| 1 | 1 | 1 |  |  |  |  |  |  |

b) Write the Boolean expression for the circuit in a). Do not simplify. (6 points)
c) What type of gate could the above circuit be replaced with to give the same results for Q based on A, B and C? (2 points)

1) Three input AND gate
2) Three input OR gate
3) Three input NOR gate
4) Three input NAND gate
5) none of the above
$\qquad$ Section $\qquad$

Extra credit (1 point): Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.
$\qquad$ Section $\qquad$

## Spring 2004 solution

## Question 2 - Logic Gates (20 points)


b) Fill in the truth table for the circuit above: (12 points)

| A | B | C | D | E | F | G | H | Q |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 0 | 0 | 1 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 0 | 1 | 0 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 0 | 1 | 1 | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 1 | 0 | 0 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 1 | 0 | 1 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 1 | 1 | 0 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ |
| 1 | 1 | 1 | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ |

b) Write the Boolean expression for the circuit in a). Do not simplify. (6 points)
$\mathrm{Q}=\sim\{\mathrm{G}+\mathrm{H}\}=\sim\{\sim \mathrm{F}+(\mathrm{F} \& \mathrm{E})\}=\sim\{\sim \sim(\mathrm{D}+\mathrm{E})+(\sim(\mathrm{D}+\mathrm{E}) \& \mathrm{E})\}$
$\mathrm{G}=\sim \mathrm{F} \quad \mathrm{H}=\mathrm{F} \& \mathrm{E}$
$\mathrm{F}=\sim(\mathrm{D}+\mathrm{E})$
$\mathrm{E}=\sim(\mathrm{B} \& \mathrm{C}) \mathrm{D}=\sim(\mathrm{A} \& \mathrm{~B})$
$Q=\sim\{[\sim \sim(\sim(A \& B)+\sim(B \& C))]+[\sim(\sim(A \& B)+\sim(B \& C)) \& \sim(B \& C)]\}$
c) What type of gate could the above circuit be replaced with to give the same results for Q based on A, B and C? (2 points)

1) Three input AND gate
2) Three input OR gate
3) Three input NOR gate
$\qquad$
$\qquad$
4) Three input NAND gate
5) none of the above

Extra credit (1 point): Simplify the Boolean expression in b) using the rules of Boolean algebra on your crib sheet.

| expression | rule |
| :--- | :--- |
| $Q=\sim\{[\sim(\sim(A \& B)+\sim(B \& C))]+[\sim(\sim(A \& B)+\sim(B \& C)) \& \sim(B \& C)]\}$ | given |
| $Q=\sim\{[(\sim A \& B)+\sim(B \& C)]+[\sim(\sim(A \& B)+\sim(B \& C)) \& \sim(B \& C)]\}$ | $\sim \sim X=X$ |
| $Q=\sim\{\sim[(A \& B) \&(B \& C)]+[\sim \sim(A \& B \& B \& C)) \& \sim(B \& C)]\}$ | $\sim X \& \sim Y=\sim(X \& Y)$ |
| $Q=\sim\{\sim[A \& B \& B \& C]+[(A \& B \& B \& C) \& \sim(B \& C)]\}$ | $\sim \sim X=X$ |
| $Q=\sim\{\sim[A \& B \& C]+[(A \&(B \& C) \& \sim(B \& C)]\}$ | $X \& X=X$ |
| $Q=\sim\{\sim[A \& B \& C]+[A \& 0]\}$ | $X \& \sim X=0$ |
| $Q=\sim\{\sim\{A \& B \& C]+0\}$ | $X \& 0=0$ |
| $Q=\sim \sim\{A \& B \& C\}$ | $X+0=X$ |
| $Q=A \& B \& C$ | $\sim \sim X=X$ |

QED
$\qquad$
$\qquad$
Fall 2003
Question 2 - Logic Gates (20 points)

a) Match the gate on the left with an equivalent circuit on the right. (10 points)
$\qquad$
$\qquad$
b) Fill in the truth table for the circuit below. (6 points)


| A | B | U2A:Y | U1A:Y | U3A:Y | Q |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 |  |  |  |  |
| 0 | 1 |  |  |  |  |
| 1 | 0 |  |  |  |  |
| 1 | 1 |  |  |  |  |

c) Write the Boolean expression for the circuit in b. Do not simplify. (4 points)

Extra credit (1 point): Simplify the Boolean expression in c) using the rules of Boolean algebra on your crib sheet.
$\qquad$
$\qquad$
Fall 2003 Solution
Question 2 - Logic Gates (20 points)

a) Match the gate on the left with an equivalent circuit on the right. (10 points)

$$
\begin{aligned}
& A=1 \quad B=2 \quad C=5 \quad \boldsymbol{D}=4 \boldsymbol{E}=3 \\
& 1 \text { and } 5 \text { are DeMorgan's Laws } \\
& 3 \text { is } \sim(A \text { and } A)=\sim A \sim(A \text { or } A)=\sim A \text { too } \\
& 2 \text { is } \sim(\sim A \text { or } \sim B)=\sim \sim(A \text { and } B) \text { by DeMorgan's Law }=(A \text { and } B) \\
& 4 \text { is } \sim(\sim A \text { and } \sim B)=\sim \sim(A \text { or } B) \text { by Demorgan's Law }=(A \text { or } B)
\end{aligned}
$$

$\qquad$
$\qquad$
b) Fill in the truth table for the circuit below. (6 points)


| A | B | U2A:Y | U1A:Y | U3A:Y | Q |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| 0 | 1 | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |
| 1 | 0 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| 1 | 1 | $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{1}$ |

c) Write the Boolean expression for the circuit in b. Do not simplify. (4 points)

$$
Q=\{(\overline{A \bullet \bar{A}})+\{(B \bullet(\overline{A \bullet \bar{A}}))\}
$$

Extra credit (1 point): Simplify the Boolean expression in c) using the rules of Boolean algebra on your crib sheet.

$$
\begin{array}{ll}
Q=\{(\overline{A \bullet \bar{A}})+[(B \bullet(\overline{A \bullet \bar{A}})\} & \text { From part c }) \\
Q=\{(\bar{A}+\overline{\bar{A}})+[(B \bullet(\bar{A}+\overline{\bar{A}})]\} & \text { DeMorgan's Law } \\
Q=\{(\bar{A}+A)+[(B \bullet(\bar{A}+A))\} & \overline{\bar{X}}=X \\
Q=\{1+[(B \bullet 1)]\} & \bar{X}+X=1 \\
Q=\{1+B\} & X \bullet 1=X \\
Q=1 & X+1=1
\end{array}
$$

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Spring 2003
Question 1) Logic Gates ( 20 pts )

a) In the circuit above, form the truth table for all marked points. (2 pts each)

| A | B | C | D | E | F | G | H | I | J |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 |  |  |  |  |  |  |  |
| 0 | 0 | 1 |  |  |  |  |  |  |  |
| 0 | 1 | 0 |  |  |  |  |  |  |  |
| 0 | 1 | 1 |  |  |  |  |  |  |  |
| 1 | 0 | 0 |  |  |  |  |  |  |  |
| 1 | 0 | 1 |  |  |  |  |  |  |  |
| 1 | 1 | 0 |  |  |  |  |  |  |  |
| 1 | 1 | 1 |  |  |  |  |  |  |  |

b) Based on the truth table you formed, write a Boolean expression for D as a function of A. ( 1 pt )
c) Based on the truth table you formed, write a Boolean expression for H as a function of D and E. Your answer should involve only one gate operation. (2 pts)
d) Based on the truth table you formed, write a Boolean expression for J as a function of A, B and C. Your answer should involve only one gate operation. (3 pts)
$\qquad$
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Spring 2003 solution (not available)
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Fall 2002

## Question 2) NAND Gate Circuit (15 points)

Below is a picture of a series of NAND gates hooked together to form one of the basic gates we have studied and the PSpice output for the circuit.

a) Fill in the truth table for the circuit ( 9 pts ).

| A | B | C | D | E | F |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |

b) What gate does this represent ( 2 pts )?
c) Write a boolean expression for this circuit. Do not simplify. (4 pts).
$\qquad$ Section $\qquad$
Fall 2002 Solution
Question 2) NAND Gate Circuit (15 points)
Below is a picture of a series of NAND gates hooked together to form one of the basic gates we have studied and the PSpice output for the circuit.

a) Fill in the truth table for the circuit ( 9 pts ).

| A | B | C | D | E | F |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 |

b) What gate does this represent (2 pts)?

## XOR

a) Write a boolean expression for this circuit. Do not simplify. (4 pts).

$$
\overline{\overline{(A \bullet B)} \bullet A]} \cdot[\overline{(A \bullet B) \bullet B}]
$$

$\qquad$
$\qquad$
Spring 2002

1) Logic Gates (20 points)

You should recognize the digital gates in the following circuit as the ones introduced in the lab and/or in class.

a) What kind of gate is U2A? (2 points)
b) What is the truth table for gate U2A? (6 points)
c) Indicate which of the three plots on the following page represents the output of the circuit. Show any work below for partial credit. (12 points)
$\qquad$ Section $\qquad$

Circuits for question 1 part c).
A.

B.

C.

DSTM1:1
U2A: A U1A: B U1A: $Y$

$\qquad$ Section $\qquad$

## 1) Logic Gates ( 20 points)

You should recognize the digital gates in the following circuit as the ones introduced in the lab and/or in class.

a) What kind of gate is U2A? (2 points)

Answer: U2A is a three input NOR gate
b) What is the truth table for gate U2A? (6 points)

Answer:

| $\boldsymbol{A}$ | $\boldsymbol{B}$ | $\boldsymbol{C}$ | $\boldsymbol{Y}$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

c) Indicate which of the three plots on the following page represents the output of the circuit. Show any work below for partial credit. (12 points)
work:

| DSTM1 | U2A: $\boldsymbol{Y}$ | U5A: $\boldsymbol{Y}$ | U3A: $\boldsymbol{Y}$ | U1A: $\boldsymbol{Y}$ |
| :--- | :--- | :--- | :--- | :--- |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |

Note: U1A:B is the same as U3A:Y
$\qquad$ Section $\qquad$

Circuits for question 1 part c).
A.

DSTM1:1 U2A: Y U1A: Y U1A: B

B. Answer: This one is CORRECT.

C.

DSTM1:1
U2A: A U1A: B U1A: Y

$\qquad$
$\qquad$
2) NAND Gate Circuits ( 20 points)

It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.

a. On the following plot, identify which signal goes with which location (6 points).

b. Draw a truth table for the circuit, showing the inputs, the output and as many steps in between as you need to determine how it works ( 10 points).
c. Which single type of gate is this circuit equivalent to (4 points)?
$\qquad$
$\qquad$
2) NAND Gate Circuits ( 20 points)

It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.

a. On the following plot, identify which signal goes with which location (6 points).


Answer: order from top to bottom: F,A,B,C,D,E
b. Draw a truth table for the circuit, showing the inputs, the output and as many steps in between as you need to determine how it works ( 10 points).

Answer:

| $\boldsymbol{A}$ | $\boldsymbol{B}$ | $\boldsymbol{C}$ | $\boldsymbol{D}$ | $\boldsymbol{E}$ | $\boldsymbol{F}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |

c. Which single type of gate is this circuit equivalent to (4 points)?

Answer: two input NOR gate
$\qquad$
$\qquad$

## 3) Combinational Logic ( 20 points)



Draw the truth table for the circuit above:

| A | B | C | D | E | F | G | H | I | Q |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |

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## 3) Combinational Logic ( 20 points)



Draw the truth table for the circuit above:
Answer:

| A | B | C | D | E | F | G | H | I | Q |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

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Spring 2002
Sample Question: Boolean Algebra
It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.

a. Identify which trace belongs to which point in the circuit.

b. Write a boolean expression for this circuit (Do not simplify).
$\qquad$ Section $\qquad$

| a. Properties of Operations | b. Rules of Combination | c. DeMorgan's Laws |
| :---: | :---: | :---: |
| (a1) $\mathrm{A} \cdot 0=0$ | (b1) $\mathrm{A} \cdot \mathrm{B}=\mathrm{B} \cdot \mathrm{A}$ | (c1) $\sim(\mathrm{A} \cdot \mathrm{B})=\sim \mathrm{A}+\sim \mathrm{B}$ |
| (a2) $\mathrm{A}+0=\mathrm{A}$ | (b2) $\mathrm{A}+\mathrm{B}=\mathrm{B}+\mathrm{A}$ | (c2) $\sim(\mathrm{A}+\mathrm{B})=\sim \mathrm{A} \cdot \sim \mathrm{B}$ |
| (a3) $\mathrm{A} \cdot 1=\mathrm{A}$ | (b3) $\mathrm{A} \cdot(\mathrm{B}+\mathrm{C})=(\mathrm{A} \cdot \mathrm{B})+(\mathrm{A} \cdot \mathrm{C})$ |  |
| (a4) $\mathrm{A}+1=1$ | (b4) $\mathrm{A} \cdot(\mathrm{B} \cdot \mathrm{C})=(\mathrm{A} \cdot \mathrm{B}) \cdot \mathrm{C}$ | d. Other Rules |
| (a5) $\mathrm{A} \cdot \mathrm{A}=\mathrm{A}$ | (b5) $\mathrm{A}+(\mathrm{B}+\mathrm{C})=(\mathrm{A}+\mathrm{B})+\mathrm{C}$ | (d1) $\mathrm{A}_{i} \mathrm{~B}=\sim \mathrm{A} \cdot \mathrm{B}+\mathrm{A} \cdot \sim \mathrm{B}$ |
| (a6) $\mathrm{A}+\mathrm{A}=\mathrm{A}$ | (b6) $\mathrm{A}+(\mathrm{A} \cdot \mathrm{B})=\mathrm{A}$ | (d1)A xor $\mathrm{B}=\sim$ AandB + Aand~B |
| (a7) $\mathrm{A} \cdot \sim \mathrm{A}=0$ | (b7) $\mathrm{A} \cdot(\mathrm{A}+\mathrm{B})=\mathrm{A}$ | (d2) $\sim\left(\mathrm{A}_{i} \quad \mathrm{~B}\right)=\sim \mathrm{A} \cdot \sim \mathrm{B}+\mathrm{A} \cdot \mathrm{B}$ |
| (a8) $\mathrm{A}+\sim \mathrm{A}=1$ | (b8) $\mathrm{A} \cdot(\sim \mathrm{A}+\mathrm{B})=\mathrm{A} \cdot \mathrm{B}$ | $(\mathrm{d} 2) \sim(\mathrm{A} \text { xoR } B)=\sim \text { Aand } \sim B+$ AandB |
| (a9) $\sim(\sim A)=A$ | (b9) $\mathrm{A}+(\sim \mathrm{A} \cdot \mathrm{B})=\mathrm{A}+\mathrm{B}$ |  |
|  | (b10) $\sim \mathrm{A}+(\mathrm{A} \cdot \mathrm{B})=\sim \mathrm{A}+\mathrm{B}$ |  |
|  | (b11) $\sim \mathrm{A}+(\mathrm{A} \cdot \sim \mathrm{B})=\sim \mathrm{A}+\sim \mathrm{B}$ |  |

Note that the NOT operation is indicated here by $\sim$ instead of as a bar over the letter.
You are free to use either notation. You can indicate the rule by the letter.
[Note to students: Unfortunately, the PDF writer has trouble with the symbol font. In the above chart, the ? in sections $\mathrm{a}, \mathrm{b}$ and c are AND symbols and the meaning of the ? in section $d$ can be found in the restatement of the rule.]
c. Using the Boolean Algebra rules shown above, prove that this combination of gates works as a NOR gate.
$\qquad$
$\qquad$
Spring 2002 solution
Sample Question: Boolean Algebra ** ANSWER **
It is possible to configure all standard gates using just NAND gates. The figure below show one such combination of NANDS.

a. Identify which trace belongs to which point in the circuit.

$A=$ Clock1; $B=$ Clock2; $C=\sim A=X ; D=\sim B=Y ; E=\sim($ Xand $Y)=Z ; F=\sim E=W$
b) Write a boolean expression for this circuit (Do not simplify).
$F=\sim[\sim(\sim A$ and $\sim B)]$
$\qquad$ Section $\qquad$

| a. Properties of Operations | b. Rules of Combination | c. DeMorgan's Laws |
| :---: | :---: | :---: |
| (a1) $\mathrm{A} \cdot 0=0$ | (b1) A $\cdot \mathrm{B}=\mathrm{B} \cdot \mathrm{A}$ | (c1) $\sim(\mathrm{A} \cdot \mathrm{B})=\sim \mathrm{A}+\sim \mathrm{B}$ |
| (a2) $\mathrm{A}+0=\mathrm{A}$ | (b2) $\mathrm{A}+\mathrm{B}=\mathrm{B}+\mathrm{A}$ | (c2) $\sim(\mathrm{A}+\mathrm{B})=\sim \mathrm{A} \cdot \sim \mathrm{B}$ |
| (a3) $\mathrm{A} \cdot 1=\mathrm{A}$ | (b3) $\mathrm{A} \cdot(\mathrm{B}+\mathrm{C})=(\mathrm{A} \cdot \mathrm{B})+(\mathrm{A} \cdot \mathrm{C})$ |  |
| (a4) $\mathrm{A}+1=1$ | (b4) $\mathrm{A} \cdot(\mathrm{B} \cdot \mathrm{C})=(\mathrm{A} \cdot \mathrm{B}) \cdot \mathrm{C}$ | d. Other Rules |
| (a5) $\mathrm{A} \cdot \mathrm{A}=\mathrm{A}$ | (b5) $\mathrm{A}+(\mathrm{B}+\mathrm{C})=(\mathrm{A}+\mathrm{B})+\mathrm{C}$ | (d1) $\mathrm{A}_{i} \mathrm{~B}=\sim \mathrm{A} \cdot \mathrm{B}+\mathrm{A} \cdot \sim \mathrm{B}$ |
| (a6) $\mathrm{A}+\mathrm{A}=\mathrm{A}$ | (b6) $\mathrm{A}+(\mathrm{A} \cdot \mathrm{B})=\mathrm{A}$ | $\text { (d1)A xor B }=\sim \text { AandB }+$ Aand~B |
| (a7) $\mathrm{A} \cdot \sim \mathrm{A}=0$ | (b7) $\mathrm{A} \cdot(\mathrm{A}+\mathrm{B})=\mathrm{A}$ | (d2) $\sim\left(\mathrm{A}_{i} \quad \mathrm{~B}\right)=\sim \mathrm{A} \cdot \sim \mathrm{B}+\mathrm{A} \cdot \mathrm{B}$ |
| (a8) $\mathrm{A}+\sim \mathrm{A}=1$ | (b8) $\mathrm{A} \cdot(\sim \mathrm{A}+\mathrm{B})=\mathrm{A} \cdot \mathrm{B}$ | $(\mathrm{d} 2) \sim(\mathrm{A} \text { xor } \mathrm{B})=\sim \text { A and } \sim B+$ AandB |
| (a9) $\sim(\sim A)=A$ | (b9) $\mathrm{A}+(\sim \mathrm{A} \cdot \mathrm{B})=\mathrm{A}+\mathrm{B}$ |  |
|  | (b10) $\sim \mathrm{A}+(\mathrm{A} \cdot \mathrm{B})=\sim \mathrm{A}+\mathrm{B}$ |  |
|  | (b11) $\sim \mathrm{A}+(\mathrm{A} \cdot \sim \mathrm{B})=\sim \mathrm{A}+\sim \mathrm{B}$ |  |

Note that the NOT operation is indicated here by $\sim$ instead of as a bar over the letter.
You are free to use either notation. You can indicate the rule by the letter.
[Note to students: Unfortunately, the PDF writer has trouble with the symbol font. In the above chart, the ? in sections $\mathrm{a}, \mathrm{b}$ and c are AND symbols and the meaning of the ? in section $d$ can be found in the restatement of the rule.]
c. Using the Boolean Algebra rules shown above, prove that this combination of gates works as a NOR gate.
$F=\sim[\sim(\sim A$ and $\sim B)]$
given
$F=\sim A$ and $\sim B$
rule a9
$F=\sim(A$ or $B)$
rule c2
This is a NOR gate.
$\qquad$
$\qquad$
Fall 2001 Solution



Please show all work on all questions for full credit, some explanation of your answer is required.

1. Logic Gates ( $\mathbf{2 0}$ points) You should recognize the logic gates in the figure below as those used in part of experiment 10. The digital clock represents the function generator and the other outputs are DC values obtained by connecting to the ground and Vcc rails on the protoboard.

a. What kind of gate is U2A (2 points)?
NAND Gate



Revised: 12/4/2001
Troy, New York, USA
$\qquad$ Section $\qquad$
Fall 2001
ENGR-4300
Name $\qquad$
Pleage show all work on all questions for full credit, some explunatlon of your answer is required.
e. If you performed the same kind of experiment as you did when you tested the gates on the protaboard, which of the following three figures is conect for the inputs shown (12 psints)?



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Ploase show all trork on all questions for full credit, some explanatlon of your answer Is required.
2. NAND Gate Circuits (20 points) It is prossible to coningure all standard gates using just NAND gates. The figure below show one such combination of NANDS.

a. On the following ploh identify which signal goes with which location (6 pointis).

b. Draw a truth table for the circuit, showitg the inpuls, the output and as many steps in belween as you need to determithe hour it works ( 8 poincs).

c. Write the Boolean expression for the circuit. You do not have to simplify it. (4 points)

$$
Q=\overline{[\overrightarrow{(\vec{A}, \vec{B})}} \cdot \overrightarrow{\vec{B}]}
$$

K. A. Crmar
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$\qquad$
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| ENGR-4300 |
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Ptease show all work on all questions for full credit, some explanation of your answer is required.

3 Cambination Logle(20 puints)


N. A. Cominer

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Revited - $2 / 4 / 2001$ Troy, Mew Forl, USA
$\qquad$ Section $\qquad$
Fall 2000

1. Logic Gates You should recognize the logic gates in the figure below as those used in part of Experiment 10. If you performed the same kind of experiment as you did when you tested the gates on the protoboard, which of the following three figures is correct for the inputs shown? The digital clock represents the function generator and the other inputs are DC values obtained by connecting to the ground and $\mathrm{V}_{\mathrm{CC}}$ rails on the protoboard.

$\qquad$ Section $\qquad$



DSTM1:1
U1A: Y
U2A: Y
U3A:Y

$\qquad$
$\qquad$
Fall 200 Solution:

1. Logic Gates You should recognize the logic gates in the figure below as those used in part of Experiment 10. If you performed the same kind of experiment as you did when you tested the gates on the protoboard, which of the following three figures is correct for the inputs shown? The digital clock represents the function generator and the other inputs are DC values obtained by connecting to the ground and $\mathrm{V}_{\mathrm{CC}}$ rails on the protoboard.

work:

| DSTM1 | U2A: $\boldsymbol{Y}$ | $\boldsymbol{U} 3 A: Y$ | $\boldsymbol{U 1 A}: \boldsymbol{Y}$ |
| :---: | :---: | :---: | :---: |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 |

$\qquad$ Section $\qquad$


Answer: The one below is correct.


$\qquad$ Section $\qquad$
Fall 2000

## 3. Combinational Logic



Which of the following truth tables is correct for this circuit?

|  |  |  | A | B | Q |
| :--- | :--- | :--- | :--- | :--- | :--- |
| A | B | Q | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 |  |  |  |
|  |  |  | A | B | Q |
| A | B | Q | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 |  |  |  |
|  |  |  | 0 | B | Q |
| A | B | Q | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 |  | 1 | 1 |
| 1 | 1 | 1 | 0 | B | Q |
|  |  |  | 0 | 0 | 1 |
| A | B | Q | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 |  | 1 | 1 |
| 1 | 0 | 0 |  |  |  |

$\qquad$ Section $\qquad$
Fall 2000 solution
3. Combinational Logic


Which of the following truth tables is correct for this circuit?

| $\boldsymbol{A}$ | $\boldsymbol{B}$ | $\mathbf{U 1 A}: \mathbf{Y}$ | U2A: $\boldsymbol{Y}$ | $\mathbf{U 3 A}: \mathbf{Y}$ | U5A: $\boldsymbol{Y}$ | $\mathbf{U 4 A}: \boldsymbol{Y}$ | U6A: $\boldsymbol{Y}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

Answer: the one below is correct

| A | $\mathbf{B}$ | $\mathbf{Q}$ |
| :--- | :--- | :--- |
| $\mathbf{0}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| $\mathbf{0}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| $\mathbf{1}$ | $\mathbf{0}$ | $\mathbf{1}$ |
| $\mathbf{1}$ | $\mathbf{1}$ | $\mathbf{0}$ |


| A | B | Q |
| :--- | :--- | :--- |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |


| A | B | Q |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |


| A | B | Q |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

$\qquad$
$\qquad$
Fall 2000
4. NAND Gate Circuits

It is possible to configure all standard gates using just NAND gates. The figure below shows one such combination of NANDs. There are six voltages displayed on the transient voltage plot below. Identify which signal goes with which location. See if you can identify what the overall circuit is equivalent to. (You might want to construct the truth table for this purpose.) Remember that each standard gate comes in two forms, one that performs a particular logical function and one that performs the complement of (or NOT the) function.

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$\qquad$

## Fall 2000 Solution

## 4. NAND Gate Circuits

It is possible to configure all standard gates using just NAND gates. The figure below shows one such combination of NANDs. There are six voltages displayed on the transient voltage plot below. Identify which signal goes with which location. See if you can identify what the overall circuit is equivalent to. (You might want to construct the truth table for this purpose.) Remember that each standard gate comes in two forms, one that performs a particular logical function and one that performs the complement of (or NOT the) function.


Answer : Method 1-Truth Table

| DSTM1(A) | DSTM2(B) | $\mathbf{U 1 A}: \mathbf{Y}(\mathbf{C})$ | $\boldsymbol{U} 2 A: \mathbf{Y ( D )}$ | $\mathbf{U 3 A}: \mathbf{Y}(\mathbf{E})$ | $\mathbf{U 4 A} \mathbf{( Y ( Q )}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 0 | 0 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 |

This is a NOR GATE
Answer: Method 2 - Boolean Algebra

$$
\begin{aligned}
& \bar{A} \bullet \overline{\mathrm{~B}} \quad=\overline{\mathrm{A}} \bullet \overline{\mathrm{~B}}=\overline{\mathrm{A}+\mathrm{B}} \rightarrow \text { NOR GATE } \\
& \sim \sim(\sim \mathrm{A} \bullet \sim \mathrm{~B})=(\sim \mathrm{A} \bullet \sim \mathrm{~B})=\sim(\mathrm{A}+\mathrm{B}) \rightarrow \text { NOR GATE }
\end{aligned}
$$

