## LECTURE 5.        BINARY COUNTER

Before starting with counters there is some vital information that needs to be understood. The most important is the fact that since the outputs of a digital chip can only be in one of two states, it must use a different counting system than you are accustomed to. Normally we use a decimal counting system; meaning each digit in a number is represented by one of 10 characters (0-9). In a binary system, there can only be two characters, 0 and 1.

A computer does not recognize 0 or 1.  It only works on voltage changes.  What we call logic 0 to a computer is zero volts.  What we call logic 1 is +5 volts. When a logic state changes from a zero to a one the voltage at the pin in question goes from zero volts to +5 volts.  Likewise, when a logic state changes from a one to a zero the voltage is changing from +5 volts to zero volts.
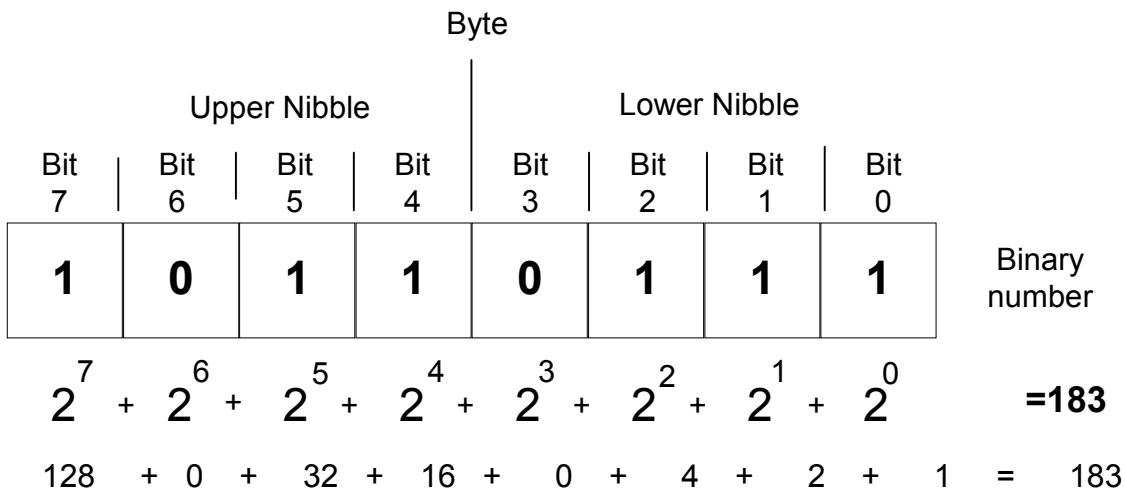
When counting up in a decimal system, we start with the first digit. When that digit 'overflows', i.e. gets above 9, we set it to 0 and add one to the next digit over. The same goes for a binary system. When the count goes above 1 we add one to the next digit over and set the first digit to 0. Here is an example.

DECIMAL TO BINARY CONVERSION

| Decimal Number (base 10) | Binary Number (base 2) |
|:---:|:---:|
| 0 | 0 |
| 1 | 1 |
| 2 | 10 |
| 3 | 11 |
| 4 | 100 |
| 5 | 101 |
| 6 | 110 |
| 7 | 111 |
| 8 | 1000 |
| 9 | 1001 |
| 10 | 1010 |

BINARY COUNTING

To convert a binary number to a decimal, we use a simple system. Each digit, or 'bit' of the binary number represents a power of two. All you need to do to convert from binary to decimal is add up the applicable powers of 2. In the example below, we find that the binary number 10110111 is equal to 183. The diagram also shows that eight bits make up what is called a byte. Nibbles are the upper or lower four bits of that byte. Referring to nibbles and bytes are useful when dealing with other number systems such as hexadecimal, which is base 16.

Byte

Upper Nibble | Lower Nibble

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|---|---|---|---|---|---|---|
| **1** | **0** | **1** | **1** | **0** | **1** | **1** | **1** | Binary number |

$$2^7 + 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^1 + 2^0 \qquad \mathbf{=183}$$

$$128 + 0 + 32 + 16 + 0 + 4 + 2 + 1 = 183$$

The counter you will use in lab is the 74XX161, the XX determines what technology was implemented when the chip was built. It may either not be there at all, i.e., 74161 or it could have been made with Lower Power Schottky characteristics and be designated 74LS161. The data sheet used is for an MC14161 counter from Motorola. The MC14161 is no longer made, however, the data specifications are identical.
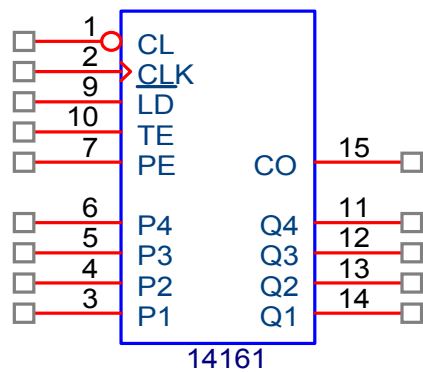


Some very important things should be noticed about this diagram. First, the pins on the chip diagram are not presented in their actual order. This is a common practice to keep the schematic as neat as possible. Be sure to hook up the pins correctly on the actual circuit.

<u>PIN OUT DETAILS</u>

| | |
|---|---|
| **QA-QD** | **= Outputs** |
| **P1-P4** | **= Program Input** |
| **CLK** | **= Clock** |
| **CO** | **= Carry out** |
| **TE, PE** | **= Counter and program enable** |
| **CL** | **= Clear (Master Reset)** |
| **LD** | **= Load P1-P4 value onto QA-QD** |

The binary outputs are located at pins Q1 through Q4.

Pins P1 through P4 are the program input pins. If your circuit needs to have a particular value at any time, these pins will be either connected to +5 volts or ground so that the correct number will be loaded at the output.

The clock input, CLK, is an active high input. This means that when the clock signal goes from zero volts to +5 volts, the counter increments by one.

The TE pin, counter enable, when high, + 5 volts, enables the counter to increment with every positive clock pulse.

The PE pin, program enable, allows the number programmed with P1-P4, to be sent to Q1-Q4.

The load pin, LD, is active low. The bar above the LD designation means active low. This means that when the signal on the LD pin goes from a low to a high, 0V to +5V, the data at P1-P4 is transferred to Q1-Q4.

The clear pin, CL, is also an active low pin. The circle before the connection indicated active low. When the signal at the clear pin goes from +5 volts to zero volts, all the outputs, Q1-Q4, will go low, zero volts, regardless of the count or data on pins P1-P4.
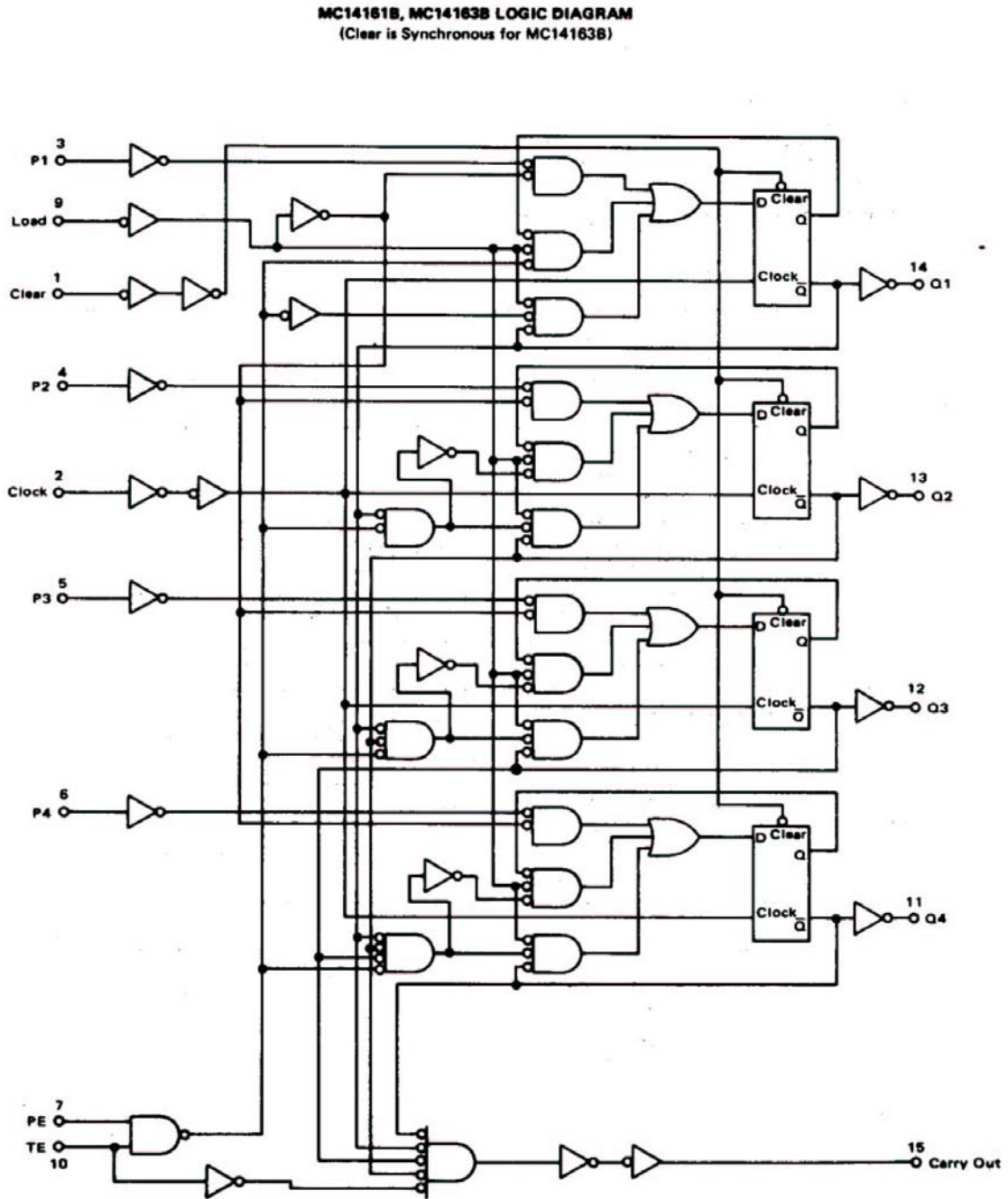
The carry over signal, CO, indicates that the counter has reached the maximum value it can count to and if higher numbers are still to be counted, this signal is connected to other counter chips to continue the process.
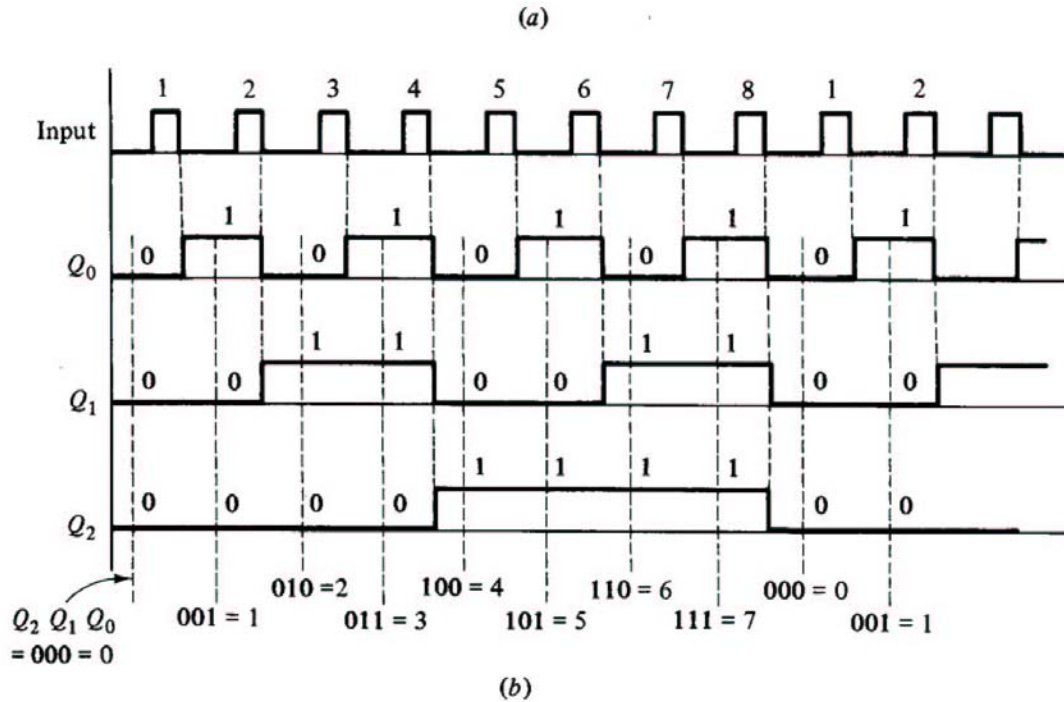
# CIRCUIT IN THE LAB
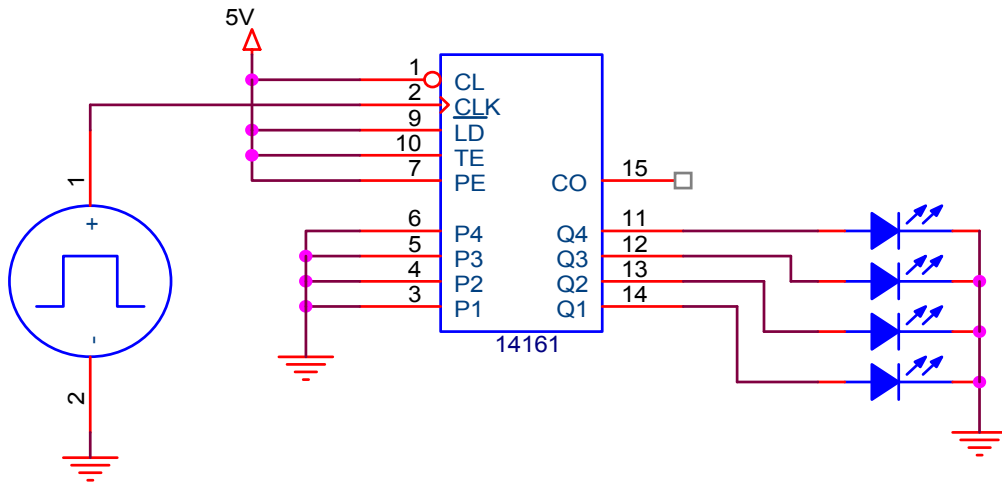
## COUNTER CIRCUIT

The counter is comprised primarily of inverters, NAND gates, and D flip-flops.

**MC14161B, MC14163B LOGIC DIAGRAM**
(Clear is Synchronous for MC14163B)

TIMING DIAGRAMS



(a)

(b)

This timing diagram is for a device that has only three outputs; the chip used in lab has four outputs. The diagram above shows that when the input signal goes low then the outputs change state as required. Each of the outputs is either dependent on the state of the input or the previous output. $Q_0$ is dependent on the input signal, $Q_1$ is dependent on $Q_0$, $Q_2$ is dependent on $Q_1$. Observing the input signal, the clock signal on the MC14161, when it goes low the $Q_0$ output changes state. This diagram shows that all outputs start at the zero state. When the first negative transition of the clock signal occurs, $Q_0$ goes from low to high. The remaining outputs stay at the same state. Note that $Q_0$ stays at its high state until the next negative transition of the clock signal. $Q_0$ will then go low. Since $Q_0$ was high and now has gone low, $Q_1$ senses this negative transition and then goes high.

It is also important to note that since the outputs change only after every two clock pulses, the outputs are successively one-half the frequency of the previous output. If the input frequency was 1,000 Hz, the frequency at $Q_0$ = 500 Hz, the frequency at $Q_1$ = 250 Hz, and the frequency at $Q_2$ = 125 Hz. This is because each output is held high or low for twice the amount of time as the previous output.
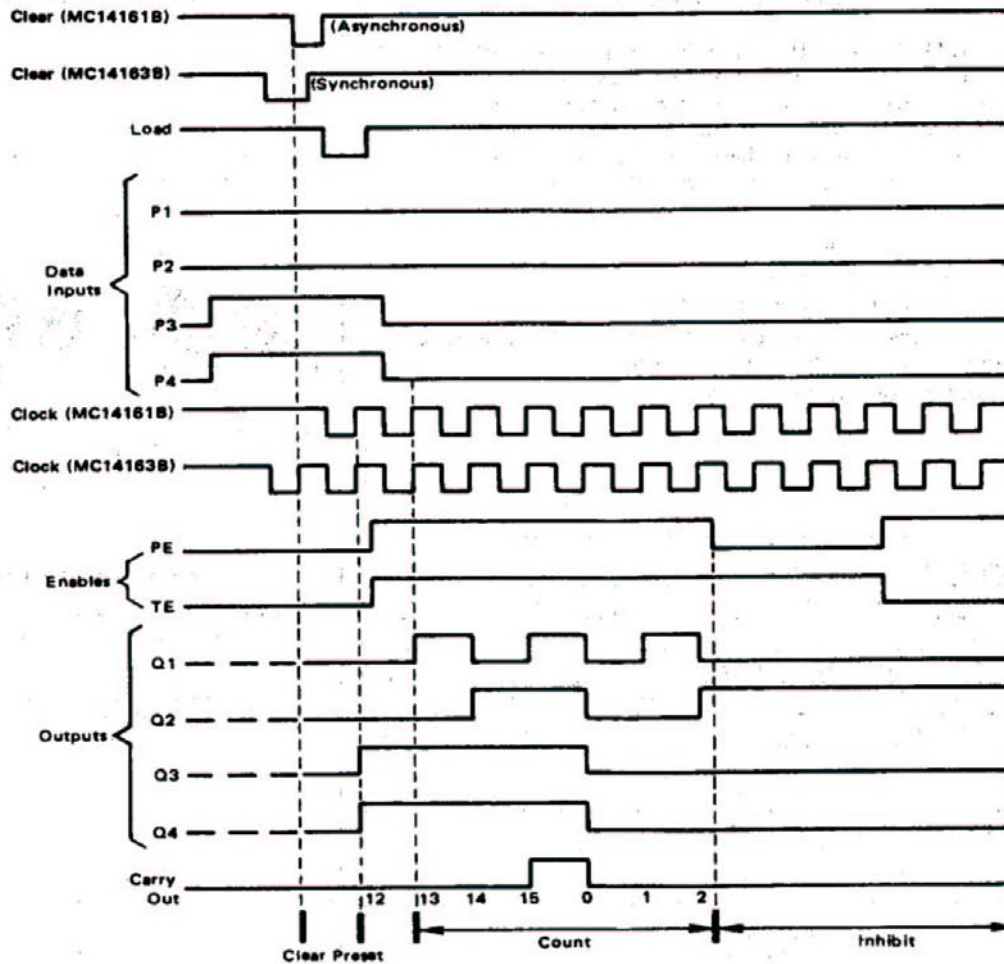
The diagram below is a typical output from the MC14161.



(a)

(b)
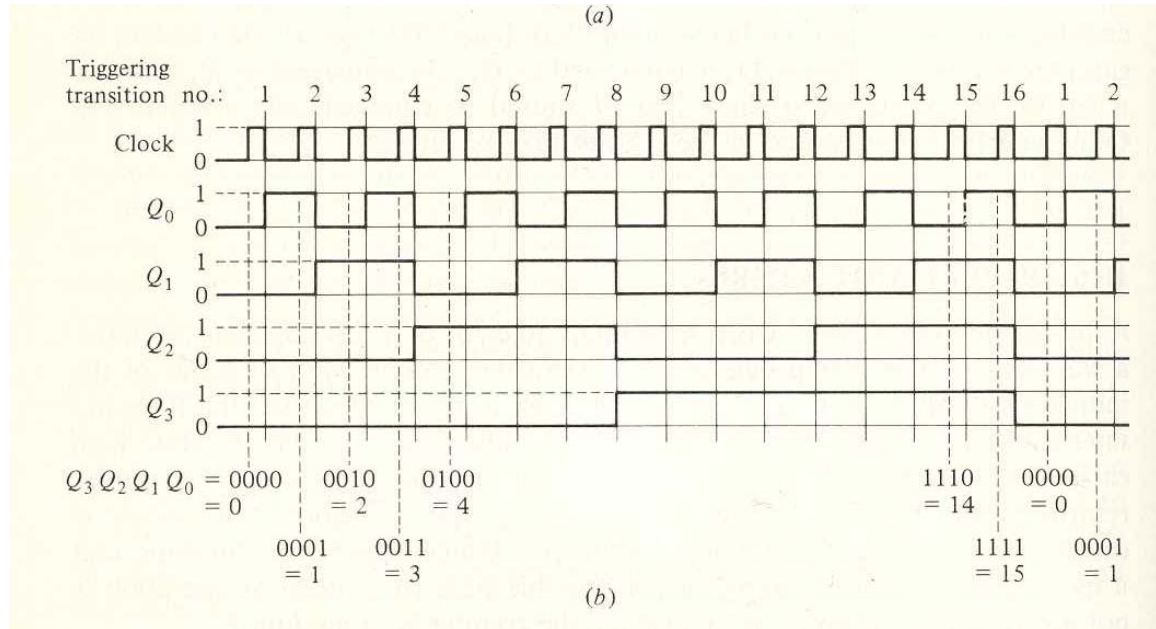
# COUNTING WITH PROGRAMMED INPUTS

**Sequence illustrated in waveforms:**

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit

Note in this timing diagram all inputs are cleared to zero, the decimal number 12 is loaded using the P1-P4 inputs, and the counter counts up to 15 and then returns to zero.