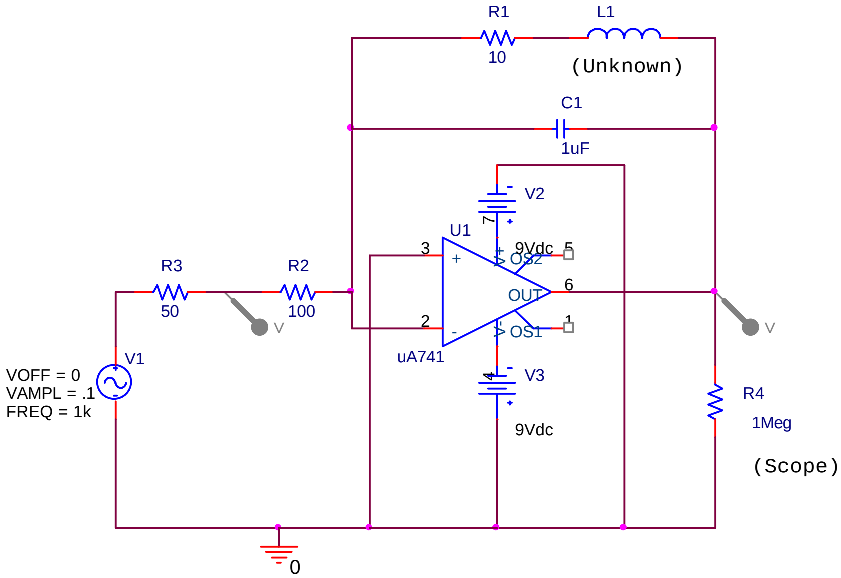
ENGR4300 | **Test 3A&B** | **Spring 2004**

Name ***solution*** | **Section ______**

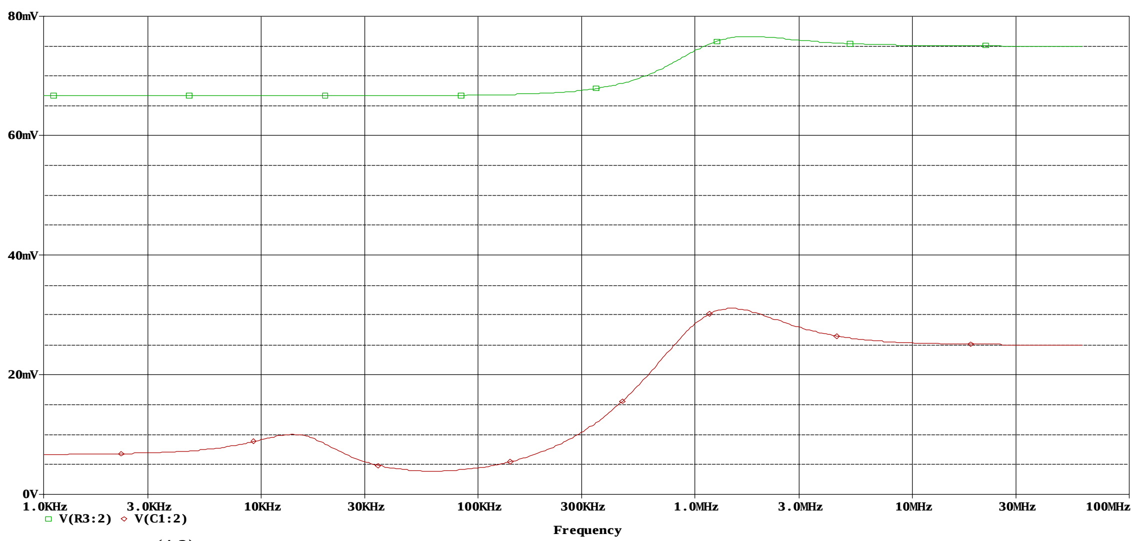
1. Inductance/Transformers (25 points)

In a variation of the inductance measurement experiment we did recently, a student decides to combine the configuration with an op-amp to see if things work better. The following circuit is built:



(Part a for Test A)

a. Capacitor C1 is varied until a distinctive response is obtained that can be used to find the unknown inductance. The four values of capacitance tried were 1uF, .1uF, .01uF, and .001uF, producing the four plots that follow. Identify the value of capacitance used for each plot. *(1 point each)* and find the unknown inductance for each plot. *(2 points each)* *[Total=12 points]*



$f_0=10^{(4.2)}=15849$ Hz $w_0=2pf_0=99582$ rad/sec

Capacitance: ***1uF*** *(lowest resonant frequency means highest capacitance)*

Inductance: *$L=1/[(w_0^2)(C)]=1/9916.5$* ***L=0.1 mH***

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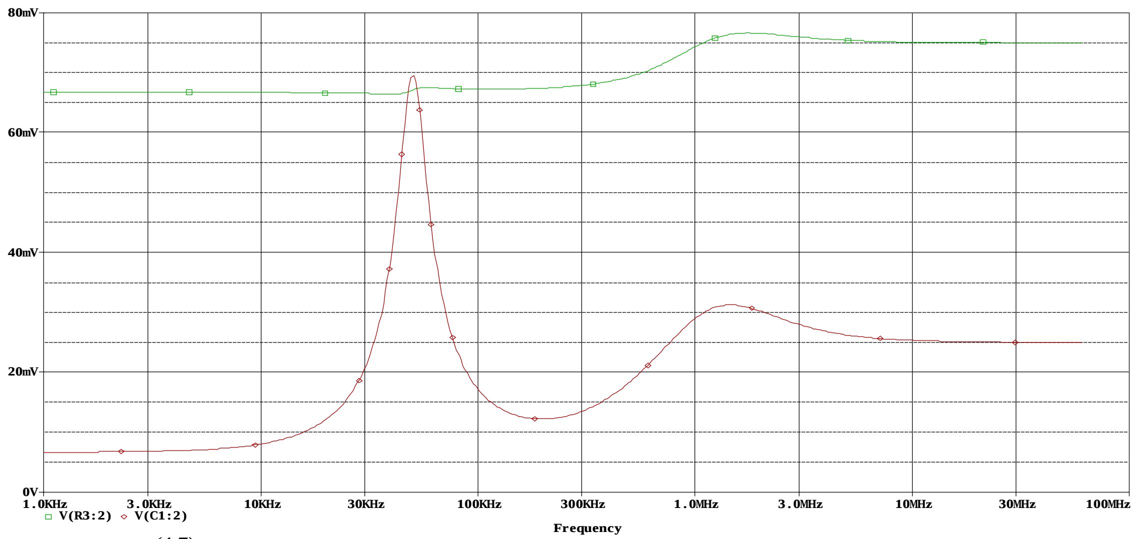
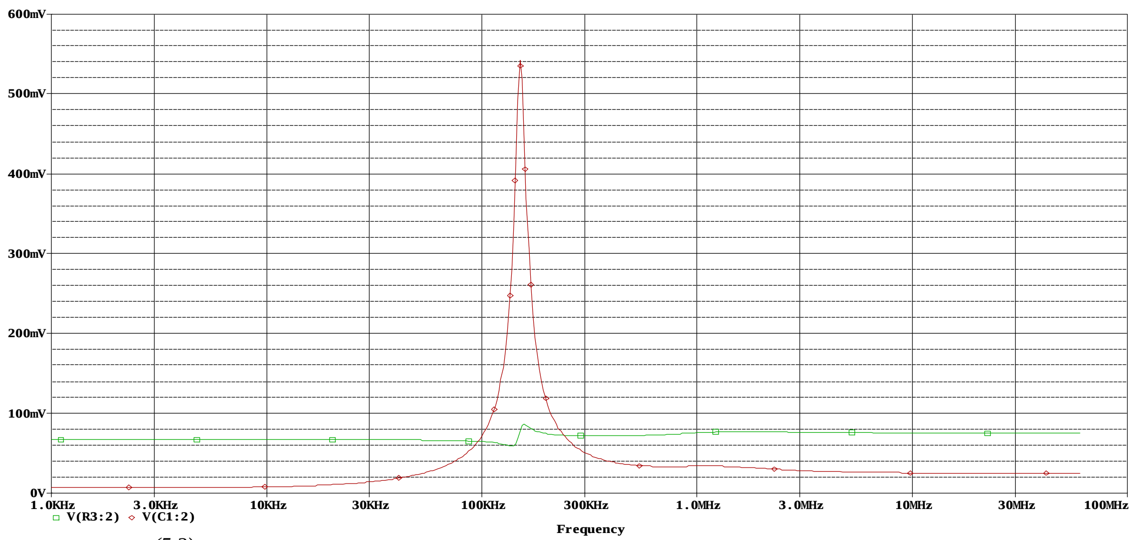


$f_0=10^{(4.7)}=50119$ Hz $w_0=2pf_0=314905$ rad/sec

Capacitance: ***0.1uF***

Inductance: *$L=1/[(w_0^2)(C)]=1/9916.5$* ***L=0.1 mH***



$f_0=10^{(5.2)}=158490$ Hz $w_0=2pf_0=995817$ rad/sec

Capacitance: ***0.01uF***

Inductance: *$L=1/[(w_0^2)(C)]=1/9916.5$* ***L=0.1 mH***

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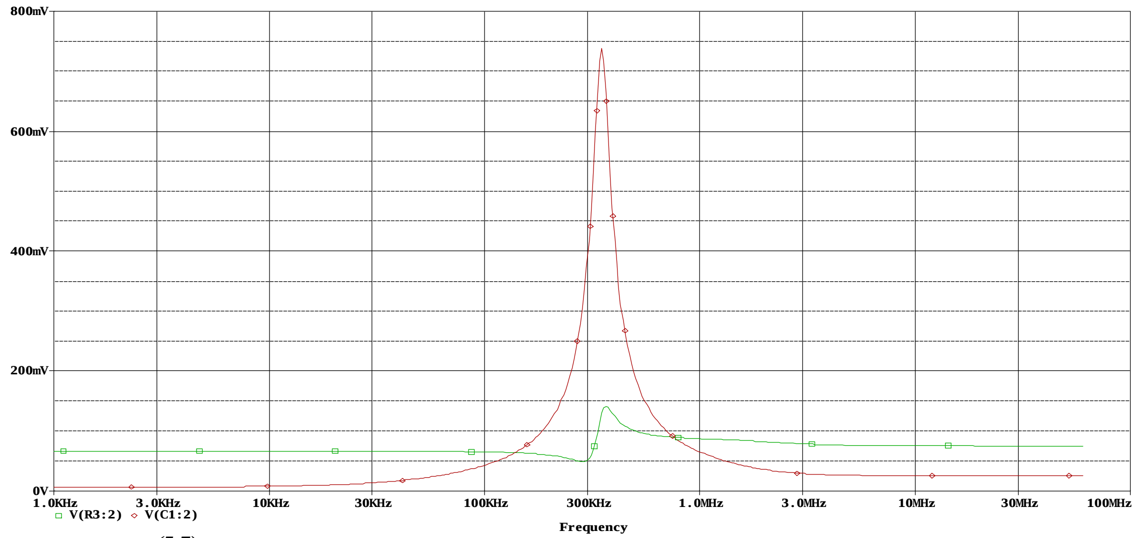

$f_0=10^{(5.7)}=501187$ *Hz* $w_0=2pf_0=3149052$ *rad/sec*

Capacitance: ***0.001uF*** *(highest resonant frequency means lowest capacitance)*

Inductance: $L=1/[(w_0^2)(C)]=1/9916.5$ ***L=0.1 mH***

I interpreted these a bit creatively to get them to come out perfectly. If yours are within an order of magnitude, the answers are good. Remember that the inductance changes at different frequencies (especially high frequencies).

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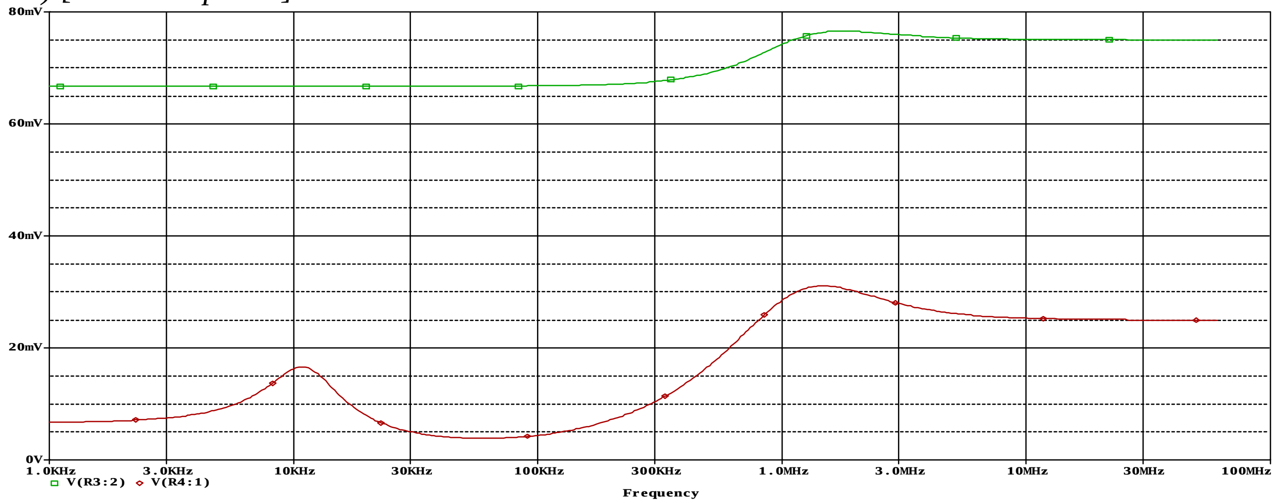
Name ***solution*** **Section ______**

(Part a for Test B)

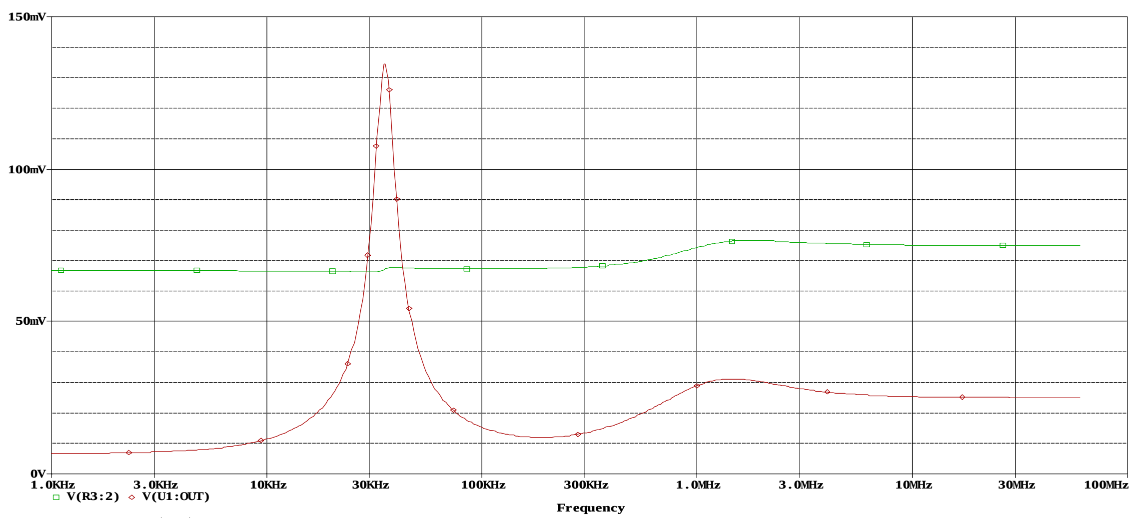
a. Capacitor C1 is varied until a distinctive response is obtained that can be used to find the unknown inductance. The four values of capacitance tried were .1uF, .01uF, .001uF, and 0.001uF producing the four plots that follow. Identify the value of capacitance used for each plot. *(1 point each)* and find the unknown inductance for each plot. *(2 points each) [Total=12 points]*



$f_0=10^{(4.1)}=12589$ *Hz* $w_0=2pf_0=79101$ *rad/sec*

Capacitance: ***0.1uF*** *(lowest resonant frequency means highest capacitance)*

Inductance: $L=1/[(w_0^2)(C)]=1/625.7$ $\boldsymbol{L=1.6}$ ***mH***



$f_0=10^{(4.6)}=39811$ *Hz* $w_0=2pf_0=250138$ *rad/sec*

Capacitance: ***0.01uF***

Inductance: $L=1/[(w_0^2)(C)]=1/625.7$ $\boldsymbol{L=1.6}$ ***mH***

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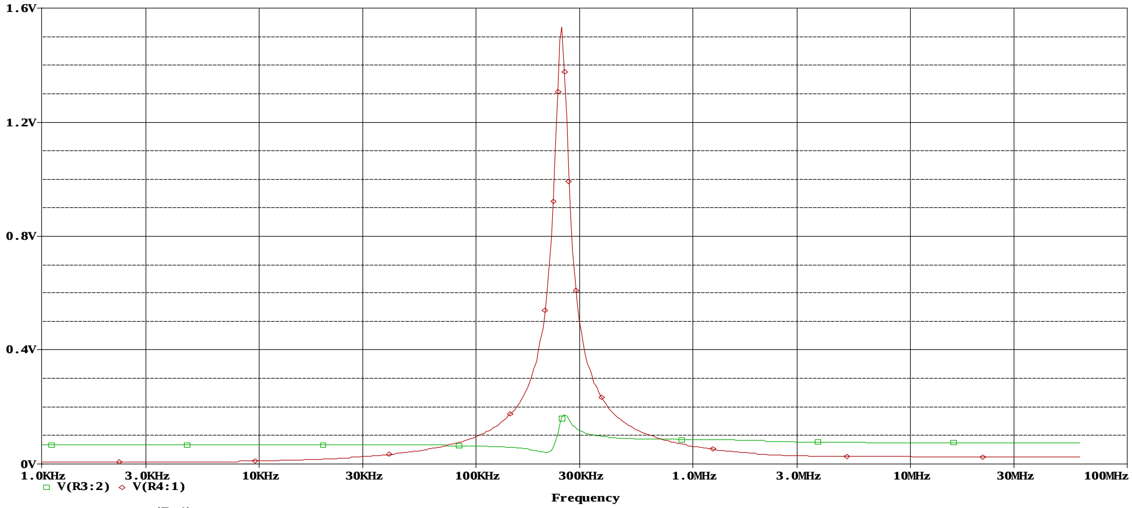
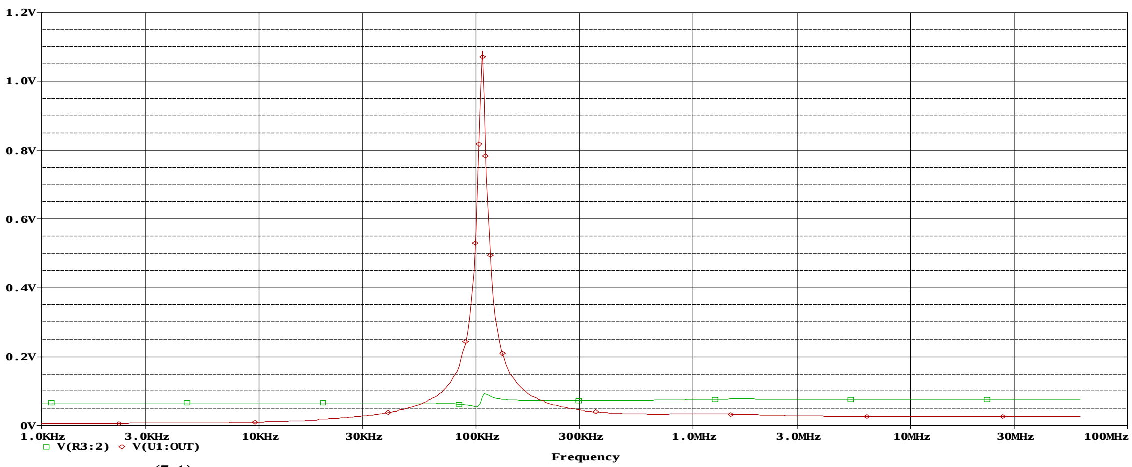


$f_0=10^{(5.4)}=251187\ Hz\ \ w_0=2pf_0=1578265\ rad/sec$

Capacitance: ***0.0001uF***

Inductance: $L=1/[(w_0^2)(C)]=1/249.1$ ***L=4.0 mH***



$f_0=10^{(5.1)}=125892.5\ Hz\ \ w_0=2pf_0=791006\ rad/sec$

Capacitance: ***0.001uF*** *(highest resonant frequency means lowest capacitance)*

Inductance: $L=1/[(w_0^2)(C)]=1/625.7$ ***L=1.6 mH***

These ones I interpreted more exactly. You can see how off it is at high frequencies. The inductance of the inductor is increasing.

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(Answer for both tests)

b. The resistance shown in series with the inductor is the resistance of the inductor coil. Assuming the student works in our classroom, how would he or she have measured this resistance? *(3 points)*

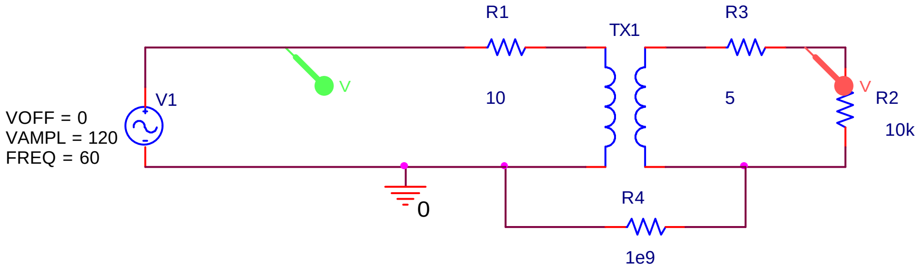
1) *Turn on the digital multimeter*
2) *Plug a dual banana connector between low and high for resistance*
3) *Connect a BNC cable to the dual banana connector*
4) *Connect a mini-grabber to the BNC cable*
5) *Connect the red and black leads of the mini-grabber cable together to measure the resistance of the wires. (Let this be R_w).*
6) *Disconnect the two leads and connect one lead to each end of the inductor.*
7) *Measure the resistance of the inductor and cable. (Let this be R_{w+L}.)*
8) *Subtract the wire resistance from the measured resistance to get the resistance of the inductor itself, R_L. ($R_L = R_{w+L} - R_w$)*

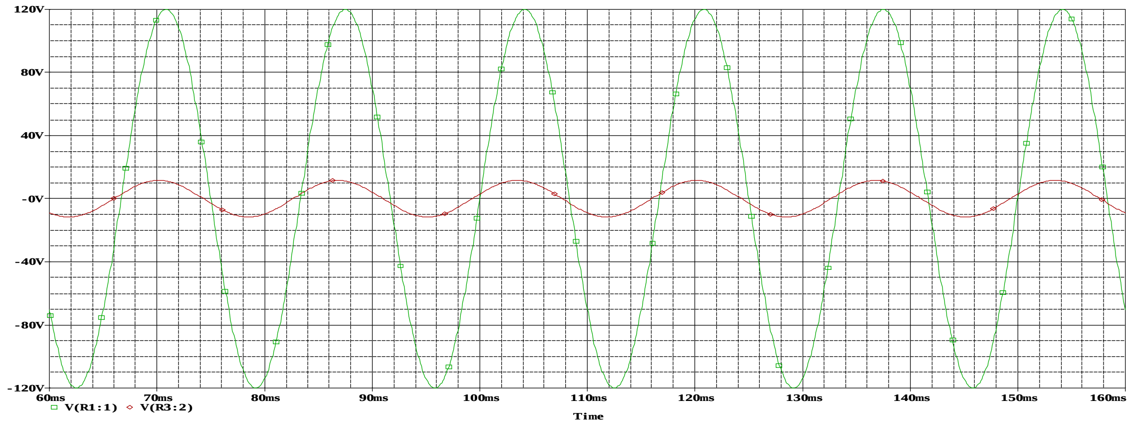
(Answers may vary)

c. If the particular application where the inductor is to be used requires a smaller resistance, a new inductor would have to be found or made. If you were to make an inductor with nearly identical inductance, but with much less resistance, how would you do it? Explain your reasoning. *(3 points)*

The equation for inductance is $L = \frac{mN^2 p r_c^2}{d}$*, where m is a constant, N is the number of turns, r_c is the coil radius and d is the coil diameter. My resistance equation tells me that* $R = \frac{l}{sA} = \frac{l}{s\,(p r_w^2)}$*, where s is a constant, and r_w is the radius of the wire. Since the inductance does not depend upon the radius of the wire itself and increasing this radius decreases the resistance, I could easily create another coil of similar inductance and less resistance by winding a thicker wire (with greater radius and lower resistance) of the same material around the same core with the same length and the same number of turns.*

d. The original inductor is now used as the primary of a transformer. The secondary is formed by wrapping an additional winding around the primary, as was done in a recent experiment. Note: the smaller resistances shown are for the inductors. Also, note that a very large resistor has been used to connect the primary to the secondary. This is because PSpice requires everything to be referenced to ground. This resistance is so large that it acts like an open circuit.





i) Assuming an ideal transformer, what inductance must the secondary have to produce the plot above (the AC line voltage is stepped down from 120Volts to 12Volts. *(3 points)*

The inductor we tested has an inductance of about 0.1mH. From the general transformer equations, we know that $a = \frac{V_2}{V_1} = \sqrt{\frac{L_2}{L_1}}$. *My voltage ratio, a, is 12/120 or 0.1. Therefore my inductance must be :*

Test A: $L2 = L1(a)^2 = (0.1m)(0.1)^2$. *Therefore* ***L2 = 0.001mH***

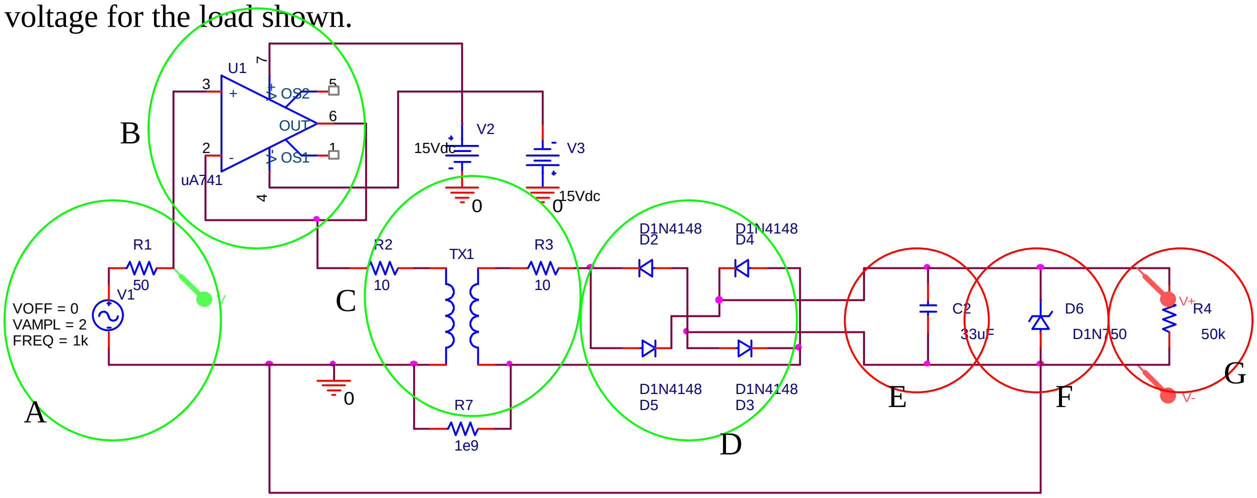
Test B: $L2 = L1(a)^2 = (1.6m)(0.1)^2$. *Therefore* ***L2 = 0.016mH***

ii) Again assuming an ideal transformer, what would the equation [in the form i(t)=Asin(ωt)] be for the current through the load resistor, R2? (Assume R4 is negligible) *(4 points)*

*The voltage through the load loop can be taken from the plot. It is v(t)=12Vsin(2p*60 t). Since v(t)=i(t)R and the load resistance is 10K ohms, we can simply divide v(t) by 10K to get an equation for the current.* ***i(t) = 1.2mA sin (120p t)=1.2mA sin(377 t)***

2. Zener Diodes/Circuit Functionality (25 points) *(Answer for A and B)*

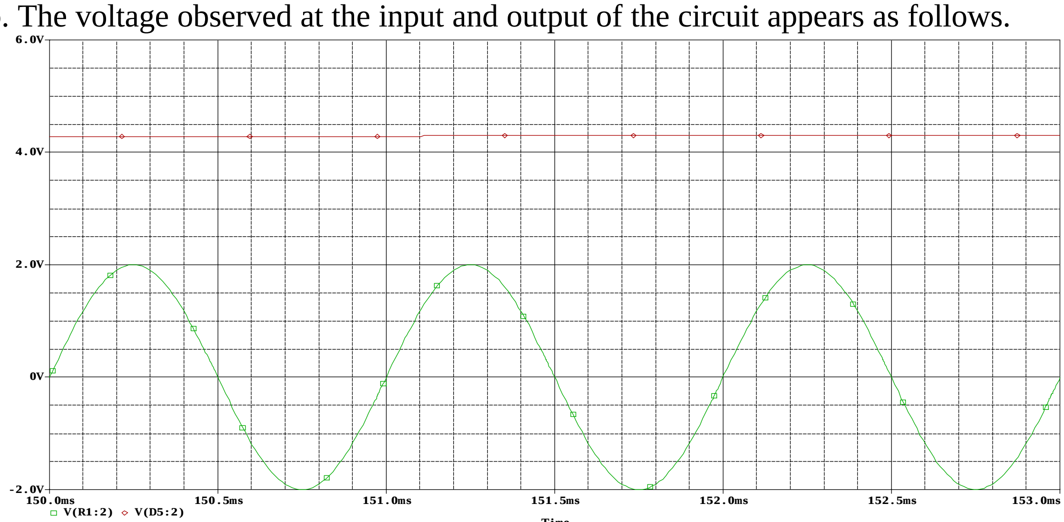
The relatively complex looking circuit below was designed to produce a constant DC voltage for the load shown.



a. Identify all of the functional blocks of this circuit by connecting the name with the letter for each circled section of the circuit. *(7 points)*

Circle		Name
A	***B***	Voltage Follower
B	***F***	Zener Diode
C	***G***	Load Resistor
D	***A***	Voltage Source
E	***D***	Full Wave Rectifier
F	***C***	Transformer
G	***E***	Smoothing Capacitor

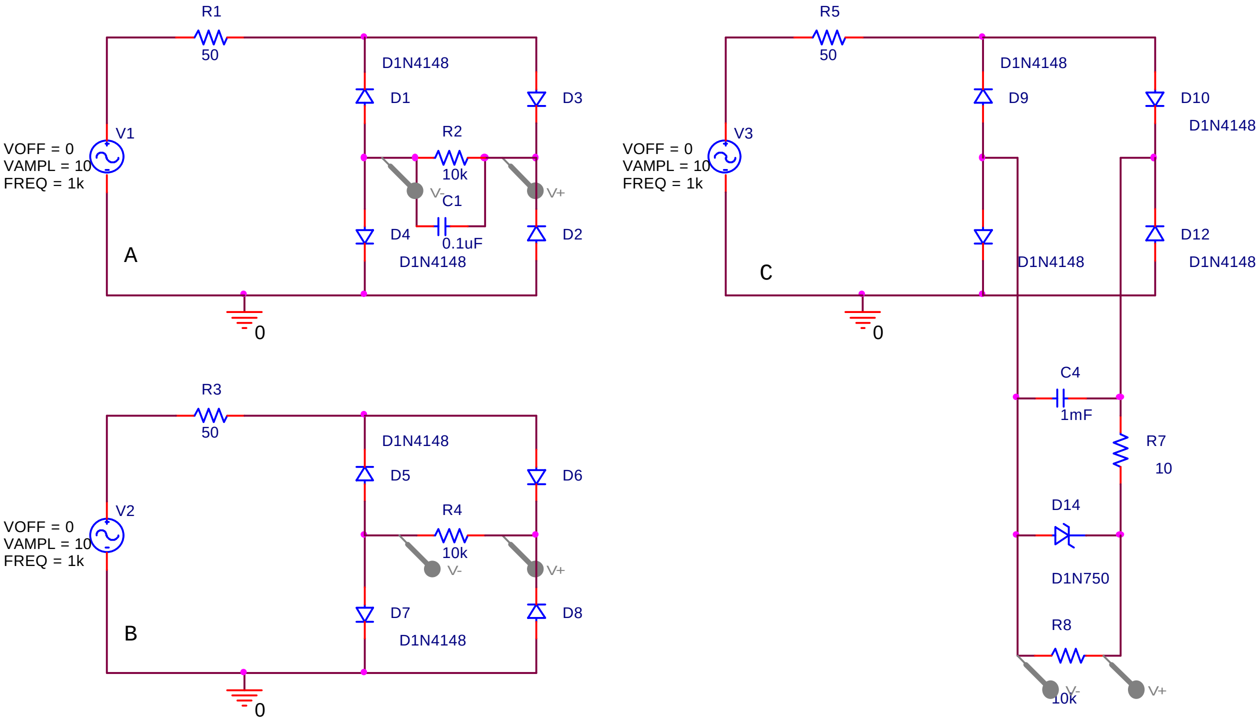
b. The voltage observed at the input and output of the circuit appears as follows.



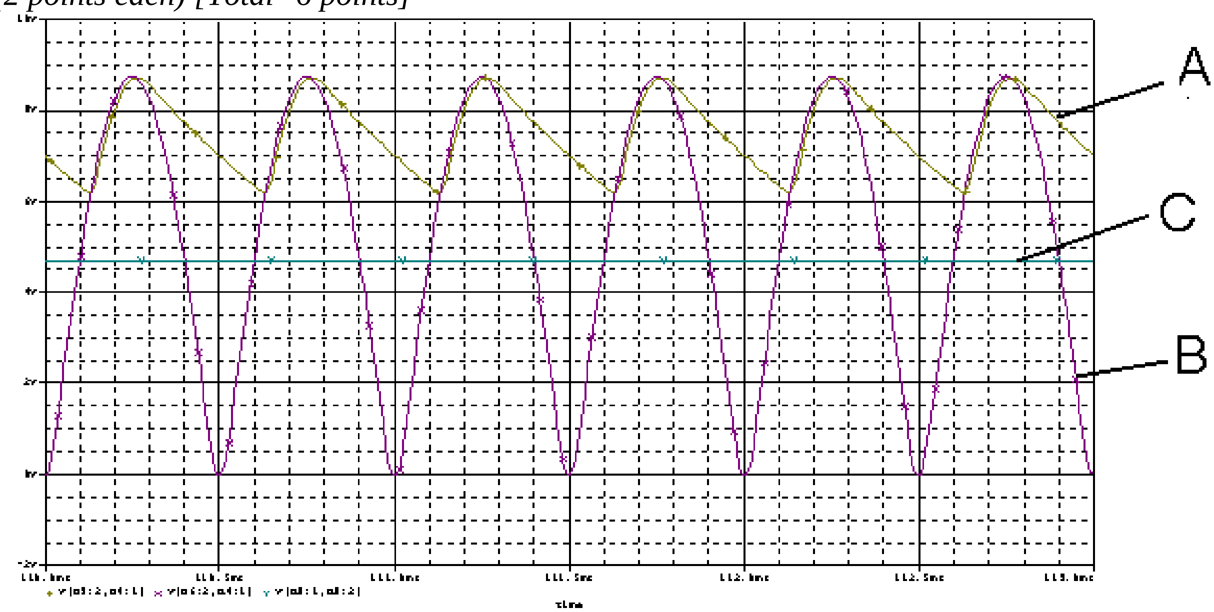
Is the transformer stepping up or stepping down the source voltage? How do you know? *(3 points)*

*It is **stepping up**. If it were stepping down, then the output would never reach the cutoff region of the zener diode and the output would not be regulated (a straight line). Stepping the voltage up brings it above Vz and then the diode holds it at exactly Vz.*

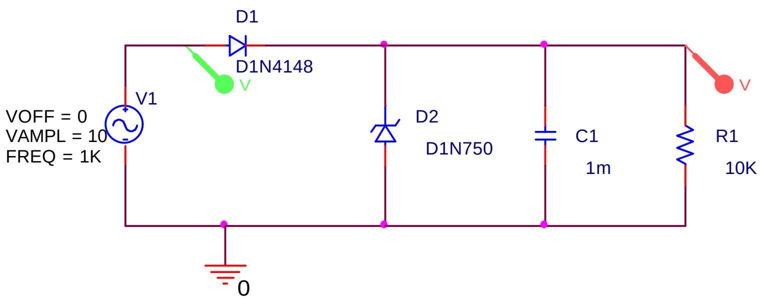
c. The following three circuits were built and analyzed.



Which of the following traces shows the output voltage for each of these circuits?
(2 points each) [Total=6 points]



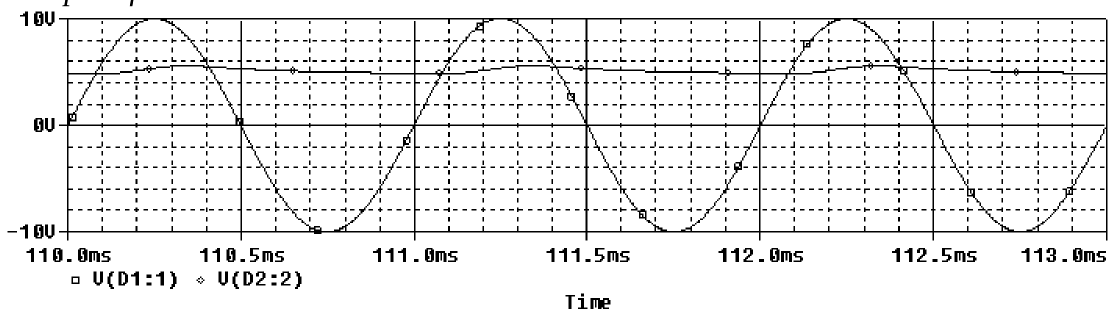
d. Using some of the components from the circuits in part c, design a circuit which uses a half wave rectifier to produce a constant DC voltage. *(6 points)*



You could also use the 0.1uF capacitor for smoothing.

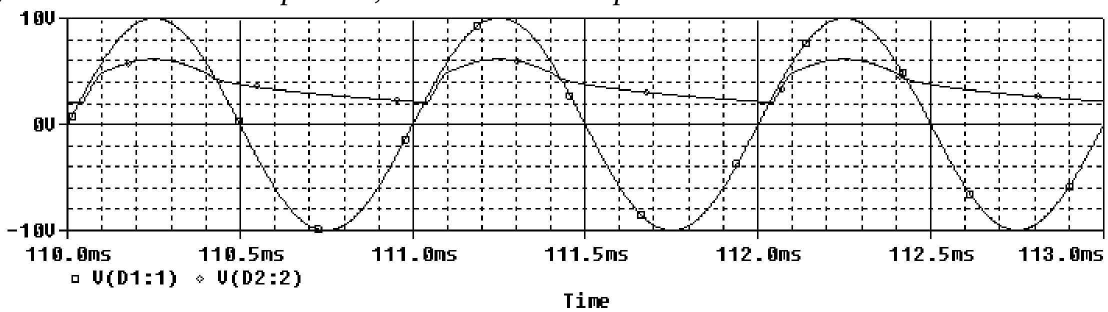
e. Would this circuit be as effective at keeping the voltage level at a constant voltage as the circuit in b? Why or why not. *(3 points)*

The output of the above circuit looks like:



You can see that it is not as smooth as the original signal. This is because the smoothing capacitor is not large enough to always keep the voltage above Vz.

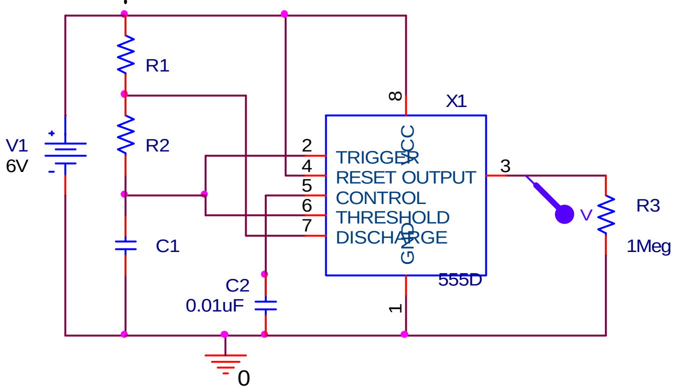
If you use the smaller capacitor, the result is even poorer:



Since the half wave rectifier only rectifies half the signal, the capacitor is discharging longer for each cycle. This gives the signal more time to drop below the zener voltage. If the signal drops below this voltage, the zener diode will be off and Vout will be equal to Vin (a voltage less than Vz). The smoothing is not complete.

3. 555 Timer Circuit (25 points)

(Answer to a for Test A)
a. Given the following 555 timer in Astable mode, where R1=50K, R2=10K and C1=0.001µF.



i) What is the value of

The on-time *(2 points)*

T1=0.693(R1+R2)C1=0.693(50E3+10E3)(1E-9)=41.58E-6

T1=41.6 ms

The frequency *(2 points)*

f=1.44/[(R1+2R2)(C1)]=1.44/[(50E3+20E3)(1E-9)]=0.020571E6

f=20571Hz

The duty cycle *(2 points)*

*D=(T1/T)x100 T=1/f=4.86E-5 D=(41.6E-6/4.86E-5)*100=.856x100*

D=86%

ii) List two ways you could change components in the above circuit to double the frequency of the output pulses. [No pots or variable resistors allowed.] Then, demonstrate mathematically that your component changes have had the desired effect.

f=20571Hz Double that is 41,143 Hz

Method 1 *(3 points):*

Half the size of C1 to 0.5 nF
f=1.44/[(R1+2R2)(C1)]=1.44/[(50E3+20E3)(5E-10)]=41,143 Hz

Method 2 *(3 points):*

Half the size of R1 and R2 R1=25K and R2=5K
f=1.44/[(R1+2R2)(C1)]=1.44/[(25E3+10E3)(1E-9)]=41,143 Hz

(Answers may vary)

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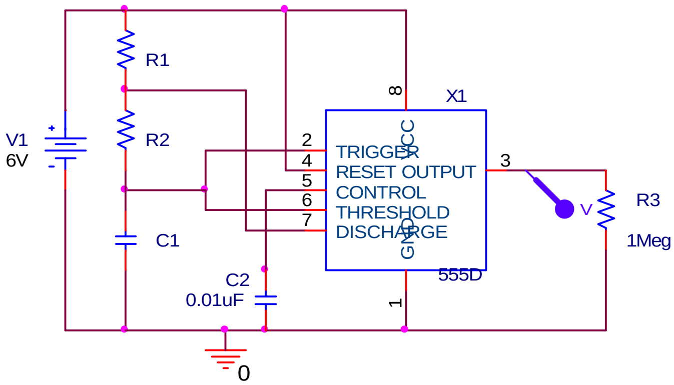
Name ***solution*** **Section ______**

(Answer to a for Test B)
a. Given the following 555 timer in Astable mode, where R1=30K, R2=5K and C1=0.001µF.



i) What is the value of

The on-time *(2 points)*

T1=0.693(R1+R2)C1=0.693(30E3+5E3)(1E-9)=41.58E-6

T1=24.255 ms

The frequency *(2 points)*

f=1.44/[(R1+2R2)(C1)]=1.44/[(30E3+10E3)(1E-9)]=36000

f=36,000Hz

The duty cycle *(2 points)*

*D=(T1/T)x100 T=1/f=2.778E-5 D=(24.255E-6/2.778E-5)*100=.873x100*

D=87.3%

ii) List two ways you could change components in the above circuit to double the frequency of the output pulses. [No pots or variable resistors allowed.] Then, demonstrate mathematically that your component changes have had the desired effect.

f=20571Hz Double that is 72,000 Hz

Method 1 *(3 points):*

Half the size of C1 to 0.5 nF
f=1.44/[(R1+2R2)(C1)]=1.44/[(30E3+10E3)(5E-10)]=72000 Hz

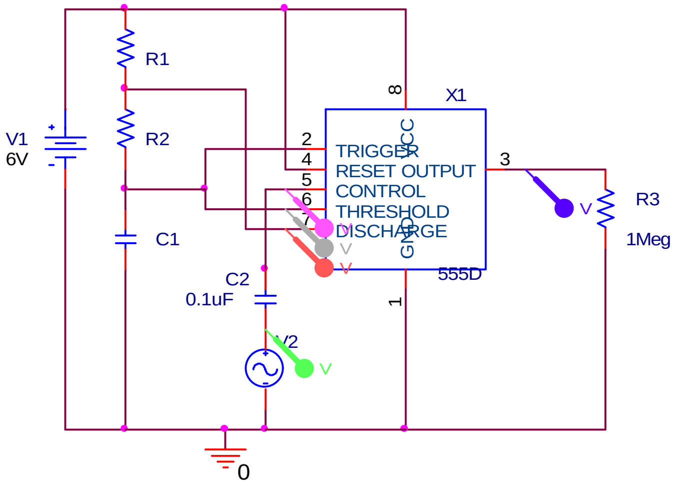
Method 2 *(3 points):*

Half the size of R1 and R2 R1=15K and R2=2.5K
f=1.44/[(R1+2R2)(C1)]=1.44/[(15E3+5E3)(1E-9)]=72000 Hz

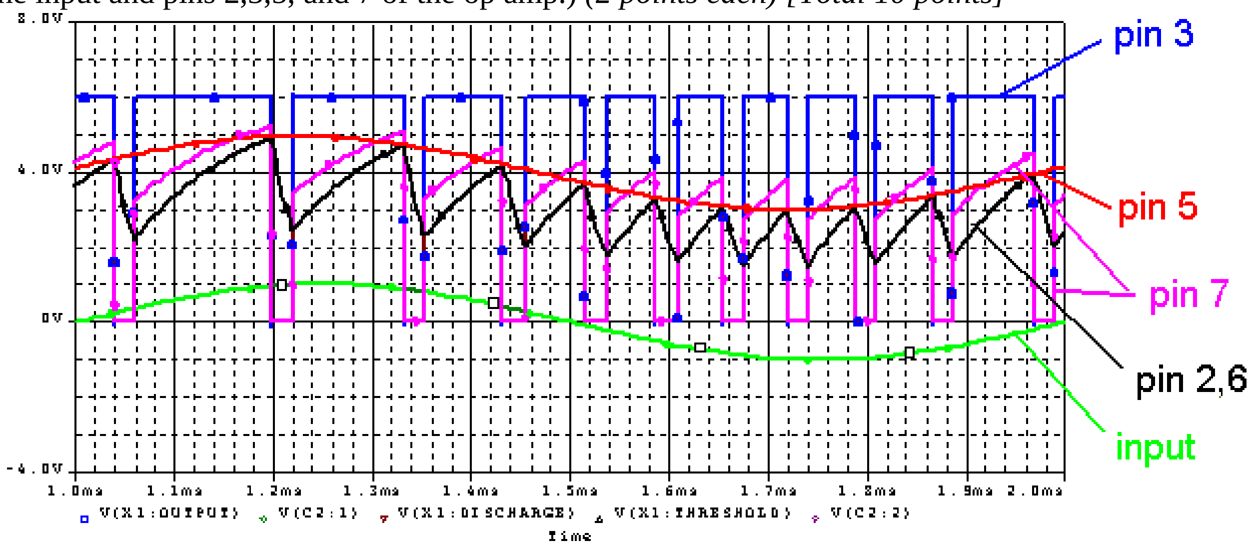
(Answers may vary)

(Answer b for both tests)

b. We have placed a sinusoidal signal on pin 5 of the above circuit.



i) Identify the traces on the following plot which go with the output locations shown. (The input and pins 2,3,5, and 7 of the op amp.) *(2 points each) [Total 10 points]*



ii) Does the frequency of the output pulses increase or decrease as the input voltage increases? Why? *(3 points)*

The frequency of the output pulses decreases as the voltage level of the input increases. This is because the capacitor has to charge for a longer time to reach the voltage level (and subsequently discharge for a longer time). Since the length of the output pulses depends upon the charge time of the capacitor, when the voltage level is high, the pulses get longer. This corresponds to a decrease in frequency.

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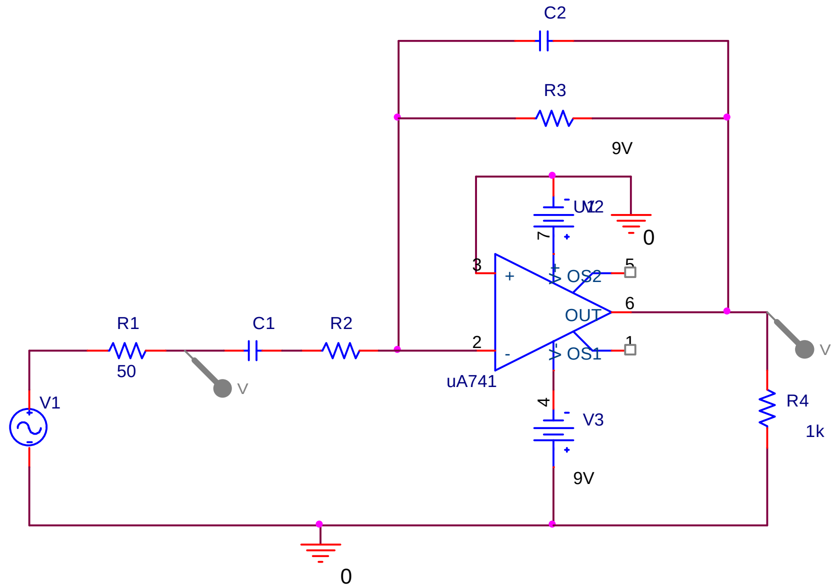
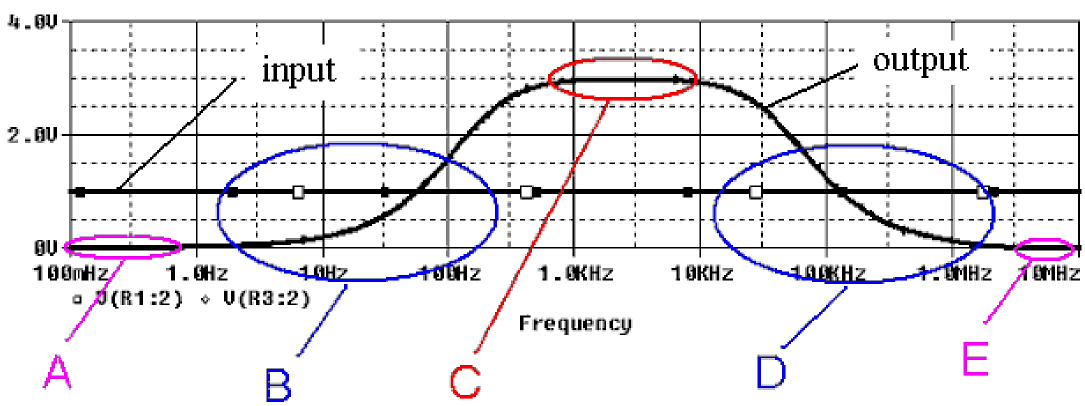
4. Op-Amps (25 points) ***(Test A Only)***

Here is a combined differentiator/integrator similar to the one you implemented in experiment 8. Let C1=0.01μF, R2=100K ohms, C2= 0.01 nF, and R3=300K ohms.



a. Below is an AC sweep for the above circuit



i) Identify the input and the output traces.*(2 points) (Test A)*

ii) If you built this circuit in the studio, in which of the circled regions would the output look like the following? *(2 points each) [Total=8 points]*

a reasonable integration of the input? ***D***

a reasonable differentiation of the input? ***B***

an amplified inversion of the input? ***C***

disappear into the noise? ***A,E***

b. What are the general equations for the following: (Give specific values based on the components in the circuit.)

i. The circuit when it is acting as an ideal integrator *(3 points)*

$$v_{out} = \frac{-1}{R_{in}C_f}\int v_{in}dt = \frac{-1}{(100K)(0.01n)}\int v_{in}dt = -1Meg\int v_{in}dt$$

(Note how the large gain compensates for 1/w in the integration. w is large, its inverse is small, so a large gain is needed to make the signal recognizable.)

ii. The circuit when it is acting as an ideal differentiator *(3 points)*

$$v_{out} = -R_f C_{in}\frac{dv_{in}}{dt} = -(300K)(0.01m)\frac{dv_{in}}{dt} = -3m\frac{dv_{in}}{dt}$$

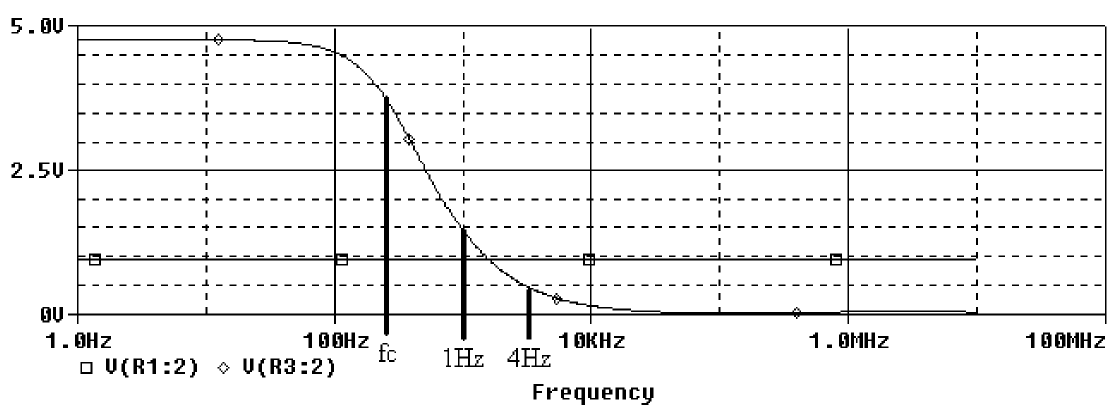
(Note how the small gain compensates for w in the differentiation. w is large, soothe gain must be small or the op-amp will saturate.)

iii. The circuit when it is acting as an inverting amplifier *(3 points)*

$$v_{out} = \frac{-R_f}{R_{in}}v_{in} = \frac{-300K}{100K}v_{in} = -3v_{in}$$

(Note that the input amplitude is 1V and at C, where the circuit is an inverting amplifier, the output amplitude is 3)

c. Sketch the AC sweep of an integrator that integrates between 1K and 4K hertz. Give a ballpark estimate of the corner frequency. Mark 1K, 4K and the corner frequency on the sketch. Justify your decisions. *(6 points)*

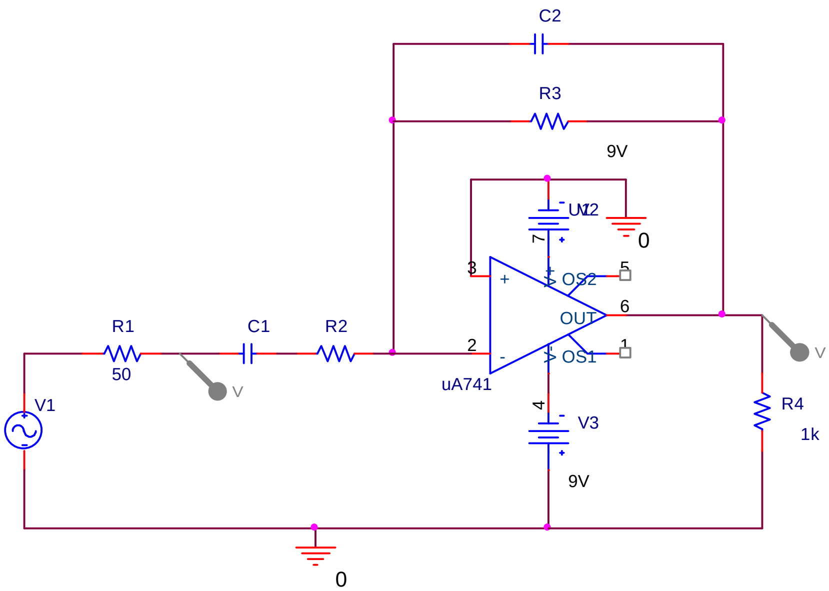


The corner frequency in this case is about 200 Hertz. Note that answers may vary. Corner frequencies should be at or below 500Hz.

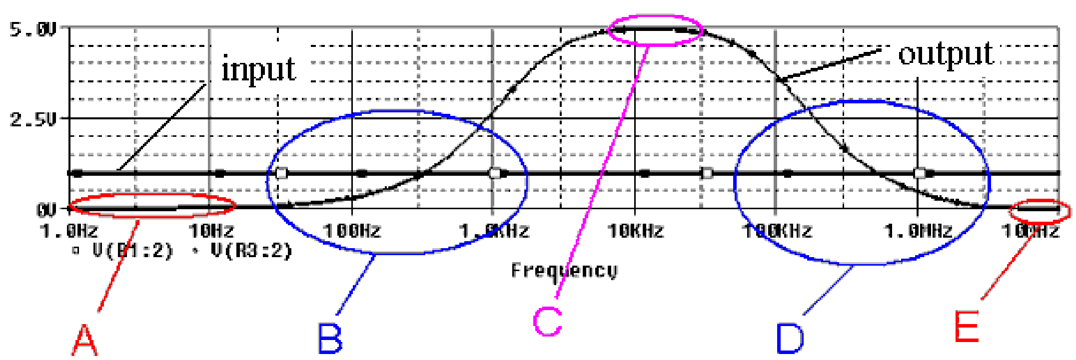
This page for Test B only

4. Op-Amps (25 points) ***(Test B Only)***

Here is a combined differentiator/integrator similar to the one you implemented in experiment 8. Let C1=0.001μF, R2=100K ohms, C2= 0.001 nF, and R3=500K ohms.



b. Below is an AC sweep for the above circuit



i) Identify the input and the output traces.*(2 points) (Test A)*

ii) If you built this circuit in the studio, in which of the circled regions would the output look like the following? *(2 points each) [Total=8 points]*

a reasonable integration of the input? ***D***

a reasonable differentiation of the input? ***B***

an amplified inversion of the input? ***C***

disappear into the noise? ***A,E***

b. What are the general equations for the following: (Give specific values based on the components in the circuit.)

i. The circuit when it is acting as an ideal integrator *(3 points)*

$$v_{out} = \frac{-1}{R_{in}C_f}\int v_{in}dt = \frac{-1}{(100K)(0.001n)}\int v_{in}dt = -10Meg\int v_{in}dt$$

(Note how the large gain compensates for 1/w in the integration. w is large, its inverse is small, so a large gain is needed to make the signal recognizable.)

ii. The circuit when it is acting as an ideal differentiator *(3 points)*

$$v_{out} = -R_f C_{in}\frac{dv_{in}}{dt} = -(500K)(0.001m)\frac{dv_{in}}{dt} = -0.5m\frac{dv_{in}}{dt}$$

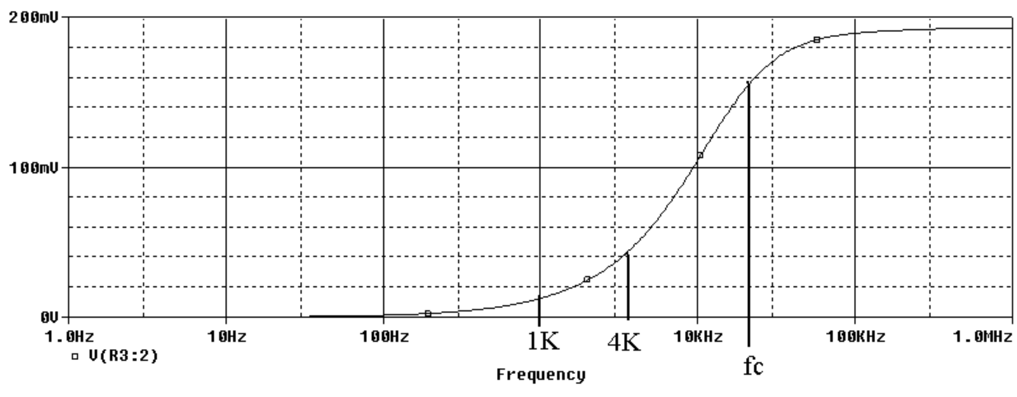
(Note how the small gain compensates for w in the differentiation. w is large, so the gain must be small or the op-amp will saturate.)

iii. The circuit when it is acting as an inverting amplifier *(3 points)*

$$v_{out} = \frac{-R_f}{R_{in}}v_{in} = \frac{-500K}{100K}v_{in} = -5v_{in}$$

(Note that the input amplitude is 1V and at C, where the circuit is an inverting amplifier, the output amplitude is 5)

c. Sketch the AC sweep of an integrator that integrates between 1K and 4K hertz. Give a ballpark estimate of the corner frequency. Mark 1K, 4K and the corner frequency on the sketch. Justify your decisions. *(6 points)*



The corner frequency in this case is about 20K Hertz. Note that answers may vary. Corner frequencies should be at or above 8K Hz