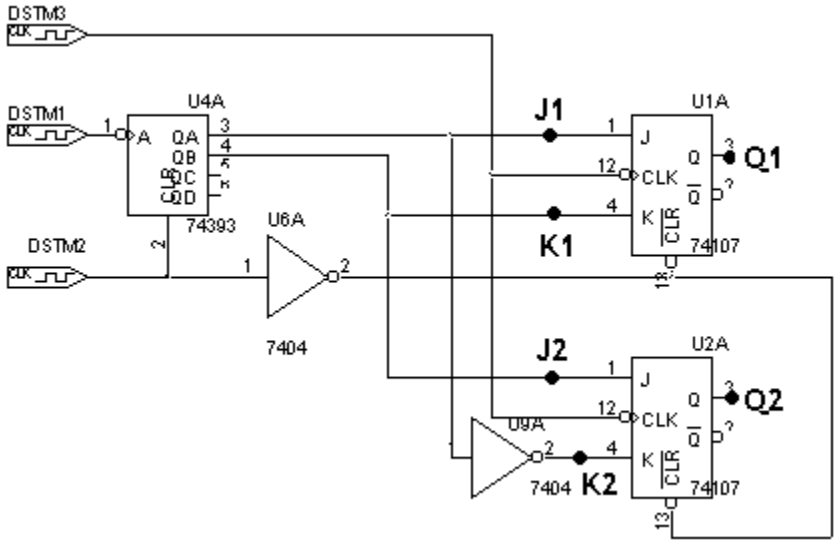
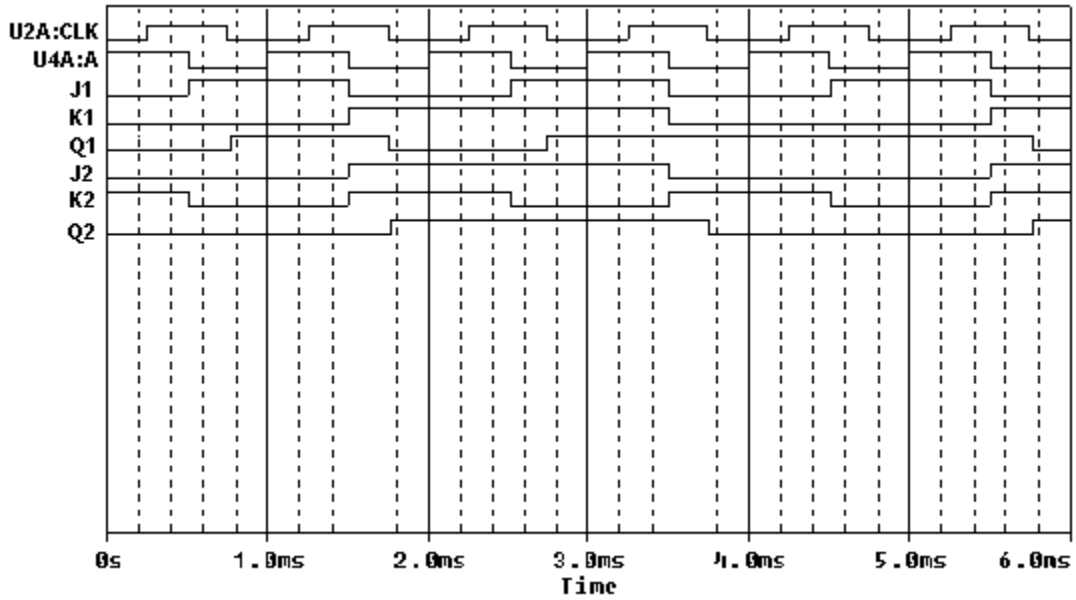
Question 1 -- Flip Flops and Counters (20 points)



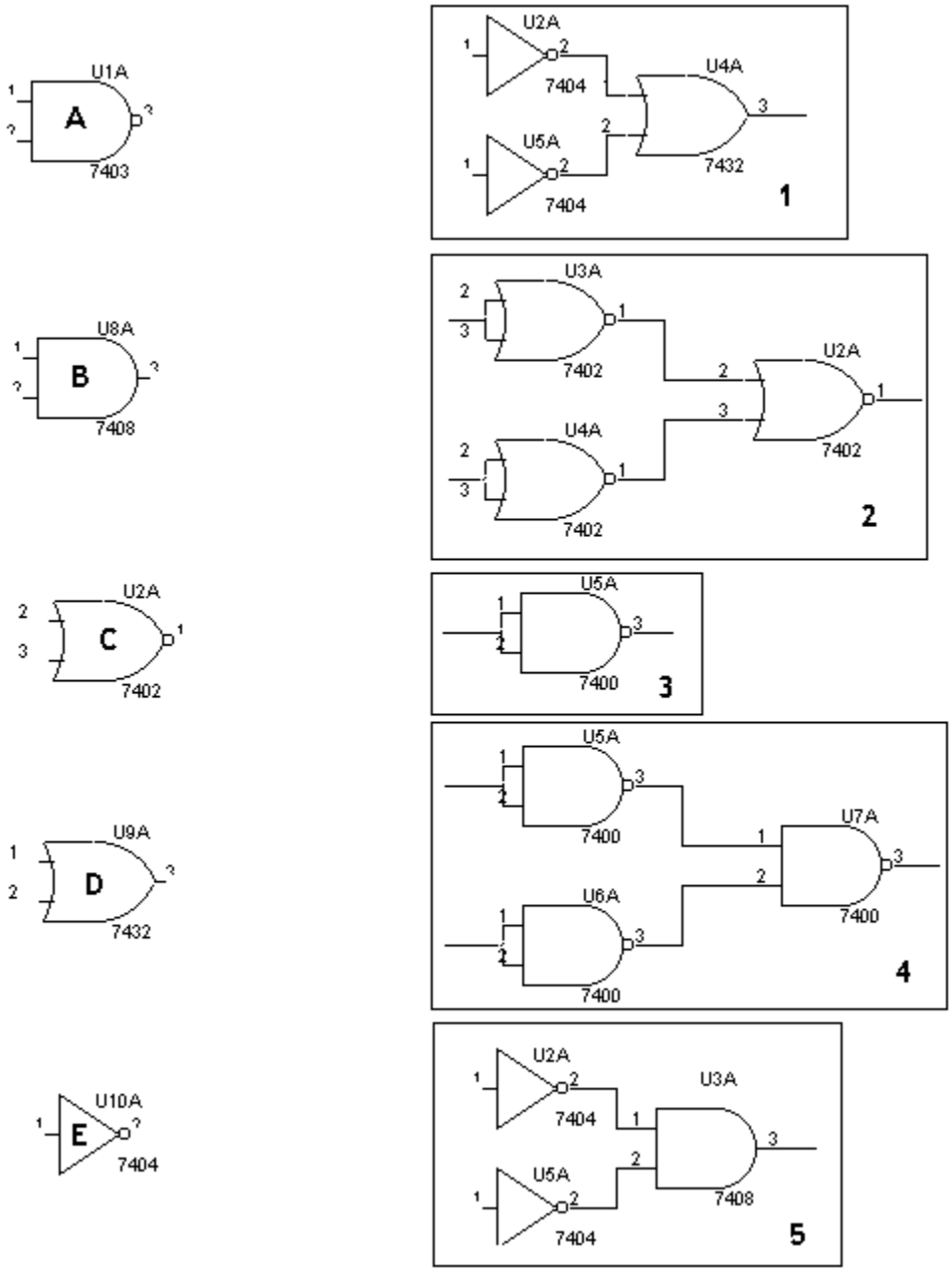
a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (counter clock), the second trace shown is DSTM3 (flip flop clock), and DSTM2 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2)
(3 points each = 18 points)



b) To what value does the counter count in the time frame indicated? *(2 points)*

*110 (binary) = **6** (decimal)*
(The highest order bit is not pictured.)

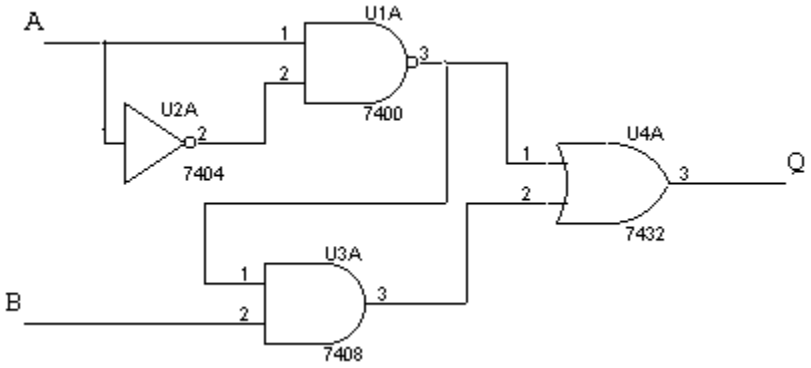
Question 2 – Logic Gates (20 points)



a) Match the gate on the left with an equivalent circuit on the right. *(10 points)*

A=1 B=2 C=5 D=4 E=3
1 and 5 are DeMorgan's Laws
3 is ~(A and A) = ~A ~(A or A) = ~A too
2 is ~(~A or ~B) = ~~(A and B) by DeMorgan's Law = (A and B)
4 is ~(~A and ~B) = ~~(A or B) by Demorgan's Law = (A or B)

b) Fill in the truth table for the circuit below. *(6 points)*



A	B	U2A:Y	U1A:Y	U3A:Y	Q
0	0	***1***	***1***	***0***	***1***
0	1	***1***	***1***	***1***	***1***
1	0	***0***	***1***	***0***	***1***
1	1	***0***	***1***	***1***	***1***

c) Write the Boolean expression for the circuit in b. Do not simplify. *(4 points)*

$$Q = \left\{\left(\overline{A \bullet \overline{A}}\right) + \left[(B \bullet \left(\overline{A \bullet \overline{A}}\right)\right]\right\}$$

Extra credit *(1 point):* Simplify the Boolean expression in c) using the rules of Boolean algebra on your crib sheet.

$$Q = \left\{\left(\overline{A \bullet \overline{A}}\right) + \left[(B \bullet \left(\overline{A \bullet \overline{A}}\right)\right]\right\} \quad \textit{From part c)}$$

$$Q = \left\{\left(\overline{A} + \overline{\overline{A}}\right) + \left[(B \bullet \left(\overline{A} + \overline{\overline{A}}\right)\right]\right\} \quad \textit{DeMorgan's Law}$$

$$Q = \left\{\left(\overline{A} + A\right) + \left[(B \bullet \left(\overline{A} + A\right)\right]\right\} \quad \overline{\overline{X}} = X$$

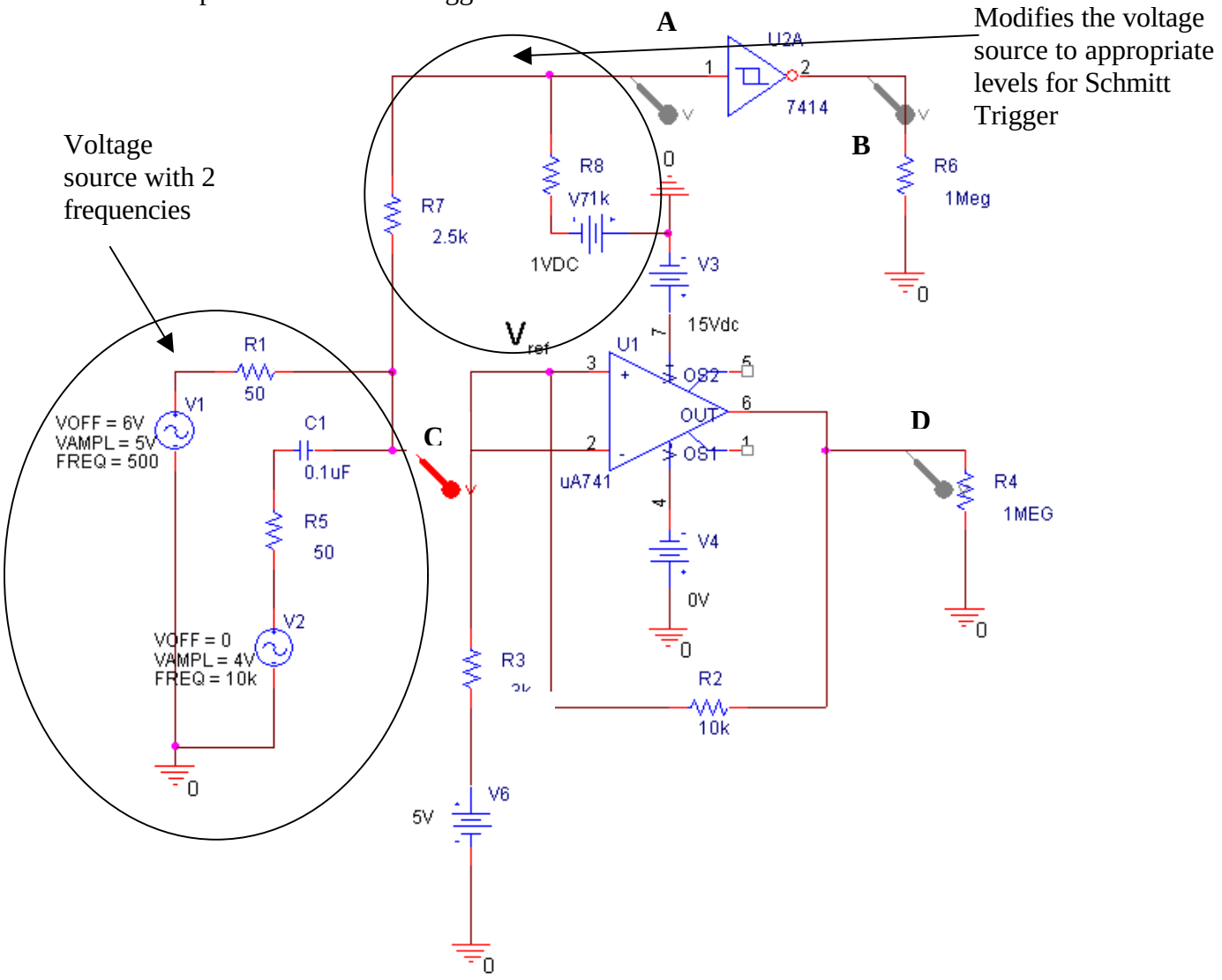
$$Q = \left\{1 + \left[(B \bullet 1)\right]\right\} \quad \overline{X} + X = 1$$

$$Q = \left\{1 + B\right\} \quad X \bullet 1 = X$$

$$Q = 1 \quad X + 1 = 1$$

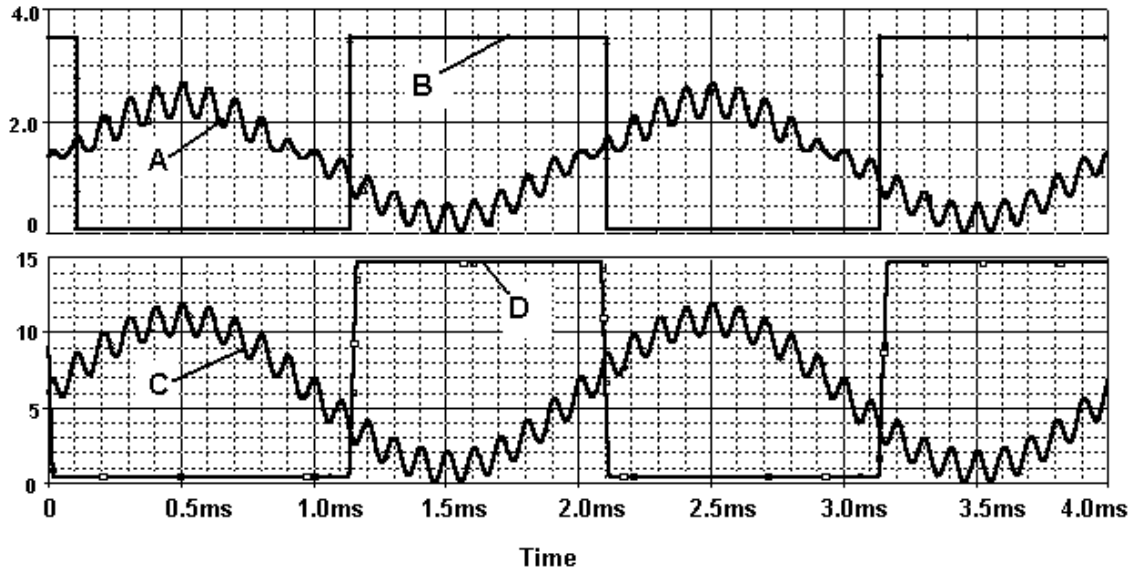
Question 3 -- Schmitt Trigger (20 points)

The following circuit was configured to study Schmitt Triggers. It includes the Schmitt trigger device (7414) we studied in Experiment 10 and the op-amp configuration assembled to produce a Schmitt Trigger circuit.



The voltage source is a combination of two sinusoidal sources at two different frequencies. The higher frequency source is coupled in through a capacitor, since this is what must be done in a real circuit. The voltage levels for the op-amp Schmitt Trigger circuit are higher than for the commercial Schmitt Trigger. Thus, two resistors and a voltage source are used to change the input voltages to levels appropriate for a logic circuit. Note that we are also operating the op-amp in an unbalanced mode with the negative voltage source set to zero.

The voltage signals measured at points **A, B, C,** & **D** in the circuit look like:



The voltage scale on the top plot ranges from 0 to 4 Volts, while the scale on the lower plot varies from 0 to 15 Volts.

a. Label each of the four signals with the letter **A, B, C,** or **D** indicating where it is measured. *(4 points)*

b. Based on the properties of the voltage sources, what range of times is shown in these plots? Assume time starts at zero (as is shown). Label the rest of the time scale. *(4 points)*

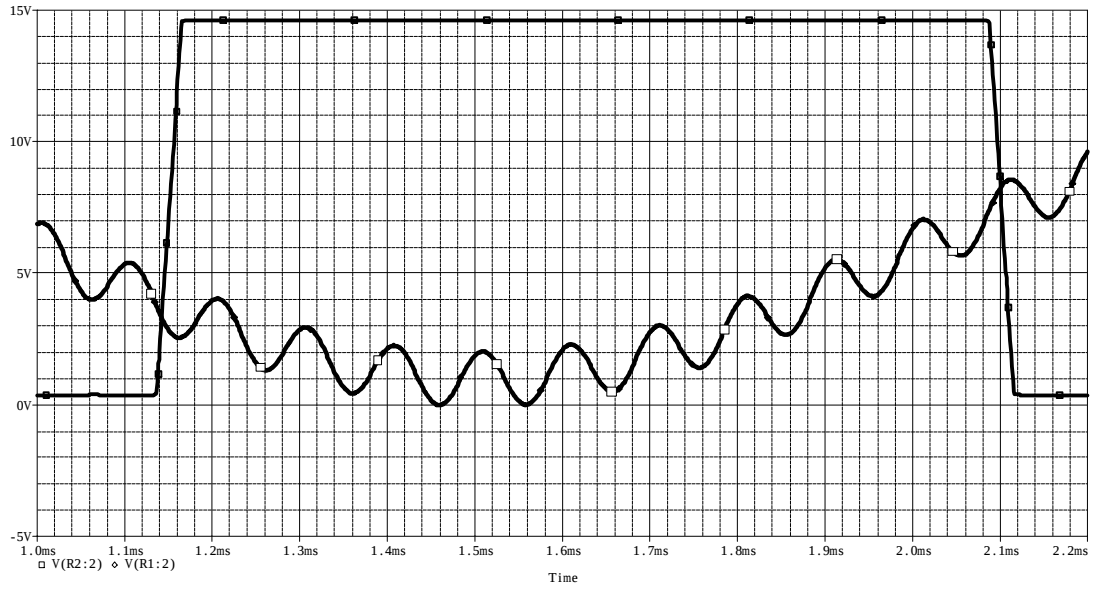
The time scale is given. The lower frequency signal is 500Hz, which has a period of 2ms. Two periods is 4ms, which is the maximum time.

c. At what voltages do the two circuits switch output states? Be as accurate as possible. *(2 points each – 8 points)*

Top plot (High to Low): ***1.7V*** Top plot (Low to High): ***0.9V***

Bottom plot (High to Low): ***7.3V*** Bottom plot (Low to High): **3.9V**

Note that acceptable voltages can be within 0.3V of these values for the bottom plot and .2V for the top plot. However, careful reading of the plots at the point where the voltage switches, should give these values. See an expanded version of the bottom plot on the next page.



d. Assuming, as is shown, that R2 = 10k Ohms, what must the value of R3 be to cause the output measured across R4 to switch at these voltages? *(4 points)*

The positive power voltage for the op amp is 15 volts. Therefore, it will saturate in the positive direction at about +15 volts. (If we look at the plot, the actual saturation voltage is 14.6 volts.) The negative threshold for the op-amp is 0 volts. Therefore, it will saturate in the negative direction at 0 volts. Note that this schmitt trigger has an offset of 5 volts. This means that we have a voltage divider, BUT it is dividing up a voltage that is not referenced from zero. We can use the following equation:

Vref – 5V = [R3/(R3+10k)] [Vcc - 5V]

For the positive threshold, Vcc=14.6V and from the graph, we can read that Vref=7.3 volts at the point where the trigger switches from high to low. Therefore, our first solution is:

7.3-5 = [R3/(R3+10k)](14.6-5) 2.3/9.6 = R3/(R3+10k) 2.4k=0.76R3 R3=3.1k

For the negative threshold, Vcc=0V and from the graph, we can read that Vref=3.9 volts at the point where the trigger switches from low to high. Therefore, our second solution is:

3.9-5 = [R3/(R3+10k)](0-5) 1.1/5 = R3/(R3+10k) 2.2k=.78R3 R3=2.8K

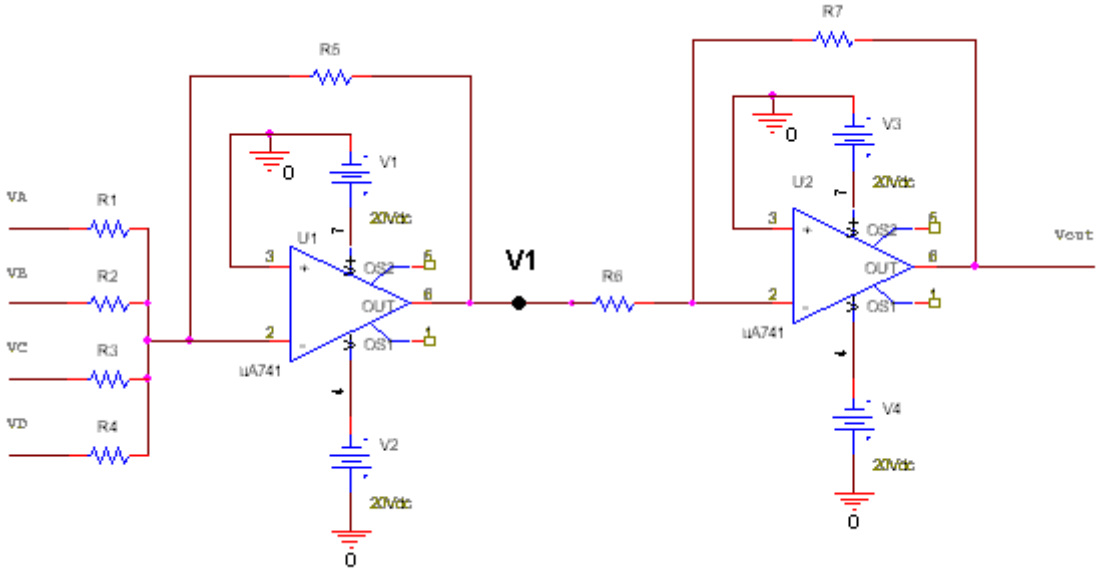
We want R3 to be the same, in both cases. Therefore, 3K is a good estimate for the value of R3.

3k is exactly the correct answer.

Given the range of voltages, any value from 2k to 4k is fine.

Question 4 -- Digital-to-Analog Converter (20 points)

The circuit below converts digital signals into analog signals. This circuit produces an analog output voltage equal to the binary word DCBA in terms of the four inputs. Please assume that the input voltage levels for this circuit is 5 Volts for a logic of "one" and 0 Volts for a logic "zero" and that R5 = 5KΩ, R6 = 2KΩ and R7 = 30KΩ.



a) Select values for R1, R2, R3, and R4 so that the output voltage will be the decimal equivalent of DCBA. For example, if DCBA=1010, or equivalently VD=VB=5 V, VA=VC=0 V, then Vout = 10 V. The circuit should work for **all** possible DCBA combinations. *(12 points)*

V1=(-R5)[(VA/R1)+(VB/R2)+(VC/R3)+(VD/R4)] *Vout = (-R7/R6)V1*

*Vout=(R5*R7/R6)[(VA/R1)+(VB/R2)+(VC/R3)+(VD/R4)]*

*(R5*R7/R6)=(5K*30K)/2K=75K*

Vout	*VA*	*VB*	*VC*	*VD*	*plug in*	*solve*
1	*5V*	*0*	*0*	*0*	*75K(5/R1)=1*	*R1=375K*
2	*0*	*5V*	*0*	*0*	*75K(5/R2)=2*	*R2=187.5K*
4	*0*	*0*	*5V*	*0*	*75K(5/R3)=4*	*R3=93.75K*
8	*0*	*0*	*0*	*5V*	*75K(5/R4)=8*	*R4=46.875K*

R1 = 375K ***R2 = 187.5K*** ***R3 = 93.75K*** ***R4 = 46.875K***

b) Show that the circuit correctly converts binary input 0111 to an AC voltage. What decimal number does 0111 represent? *(4 points)*

*Vout=(R5*R7/R6)[(VA/R1)+(VB/R2)+(VC/R3)+(VD/R4)]*
Vout=(75K)[(5/375K)+(5/187.5K)+(5/93.75K)+(0/46.875K)]
Vout = 1+2+4=7 volts

0111 = ***7 decimal***

c) Explain one way you could modify the values of the resistors in this circuit so that the output voltage gives 4*N (rather than N), when N is the digital number at the input . For example, when the input is DCBA=1010, then Vout = 4*10 V or 40V. You can modify any of the resistors R1-R7.*(4 points)*

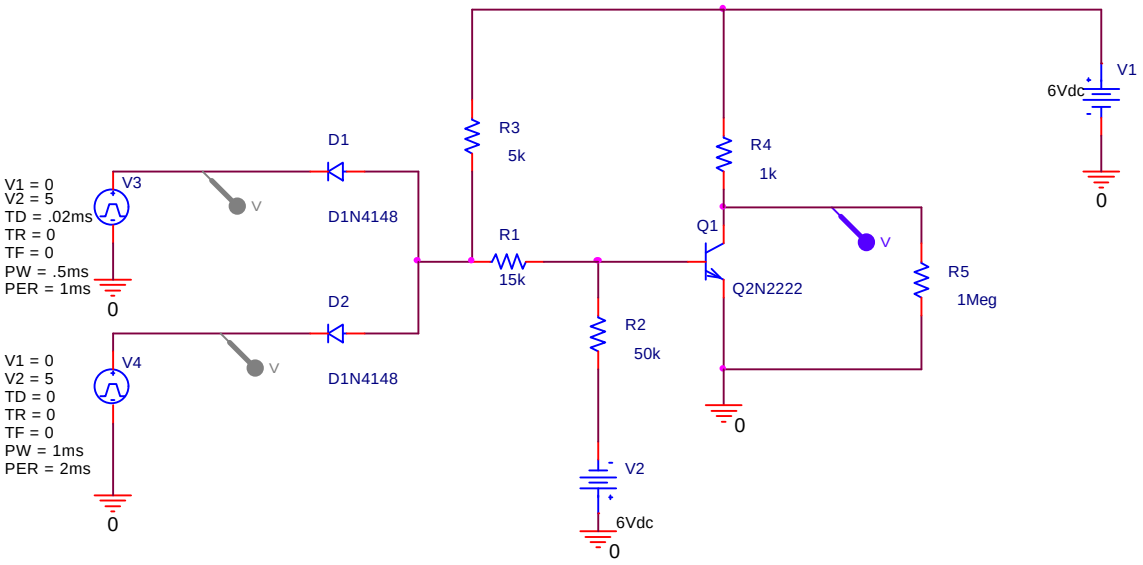
The easiest way to do this is to modify one of the gain resistors:
*R5 = 4*R5 = 20K*
or
*R7 = 4*R7=120K*
or
R6 = R6/4 = 1.25K

You could also modify the four input resistors:
R1 = R1/4 =93.75 and R2 = R2/4=46.875K and
R3 =R3/4= 23.47 and R4 = R4/4= 11.73K

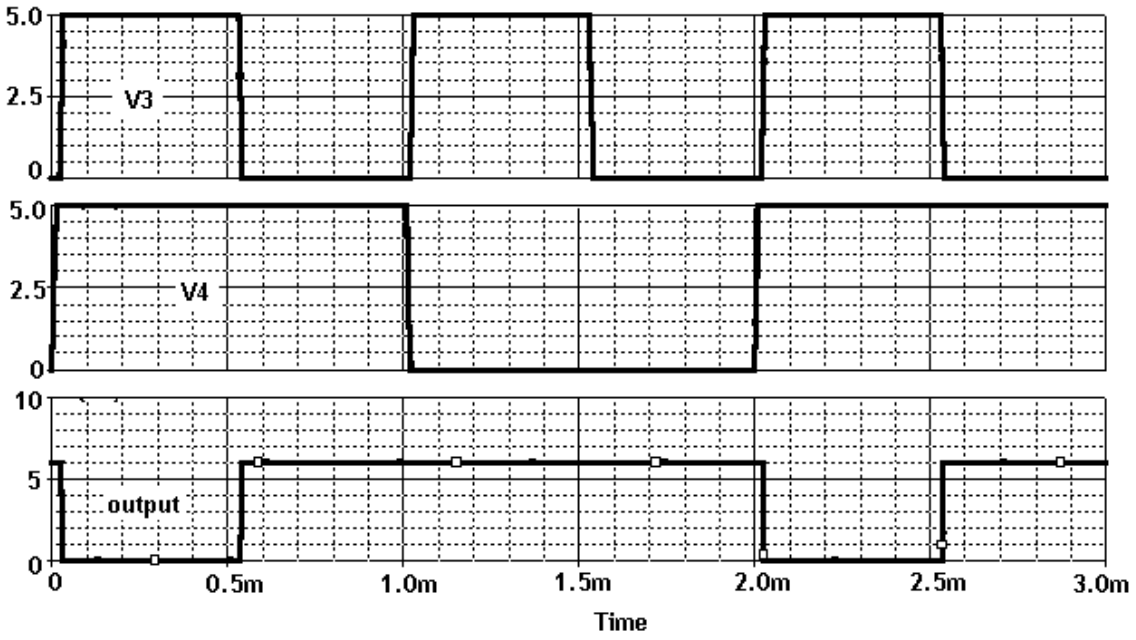
A combination which changes the gain would work also:
*R5 = R5*2=10K and R6 = R6/2 = 2.5K*

5. Transistor Switches

A simple logic circuit with two inputs and one output is configured as shown. The input voltages and the output voltages are plotted below.



a. Label which of these plots is the input V3 and the input V4. Also label which is the output measured across R5. *(2 points each – 6 points)*



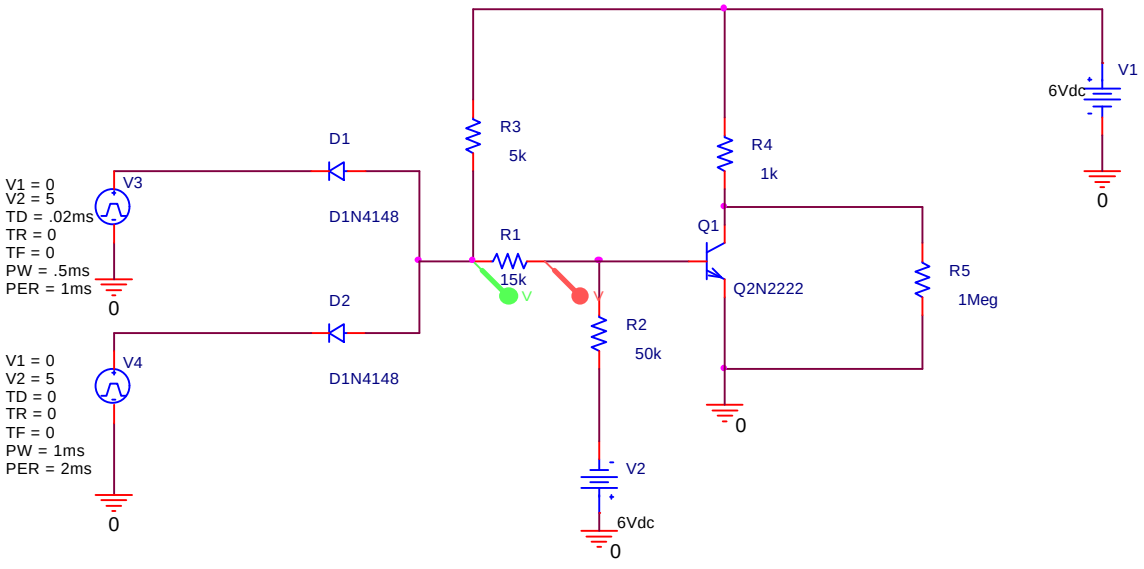
b. Based on the voltages displayed on the previous page, complete the following truth table for this configuration by putting a 0 or 1 in each of the output cells. *(4 points)*

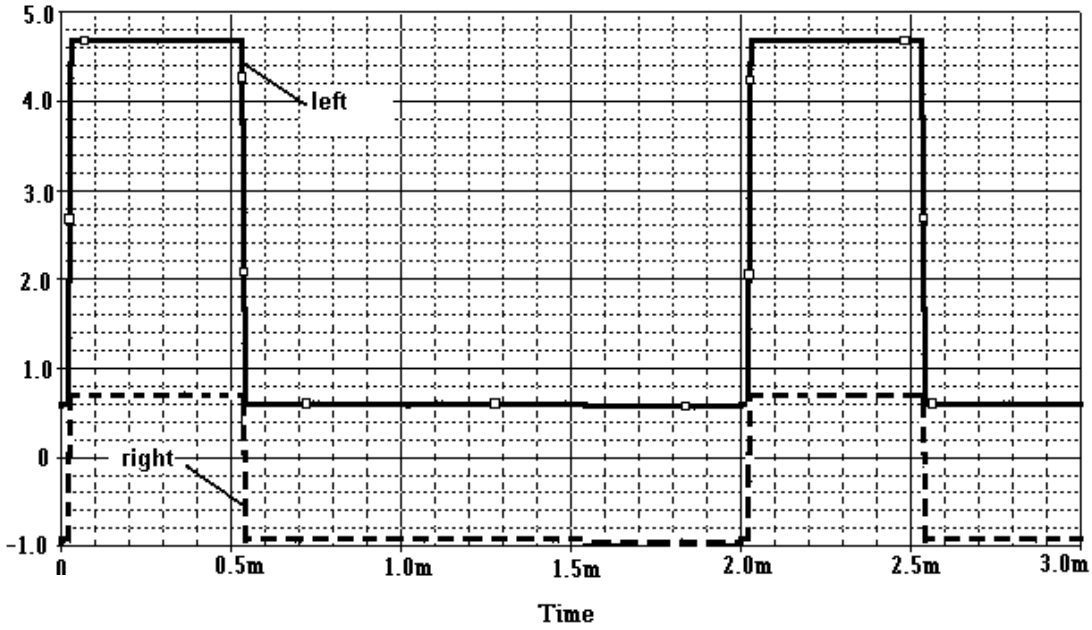
Input V3	Input V4	Output
0	0	1
0	1	1
1	0	1
1	1	0

c. What kind of device is this circuit? *(2 points)*

NAND GATE

d. Under exactly the same conditions shown above, the voltages on either side of resistor R1 are displayed below. Again, identify which of the voltages traces is which by labeling them 'left' and 'right,' respectively. The time scale is the same as for the plots above and the voltage ranges from 0 to 5 Volts. *(2 points each – 4 points)*





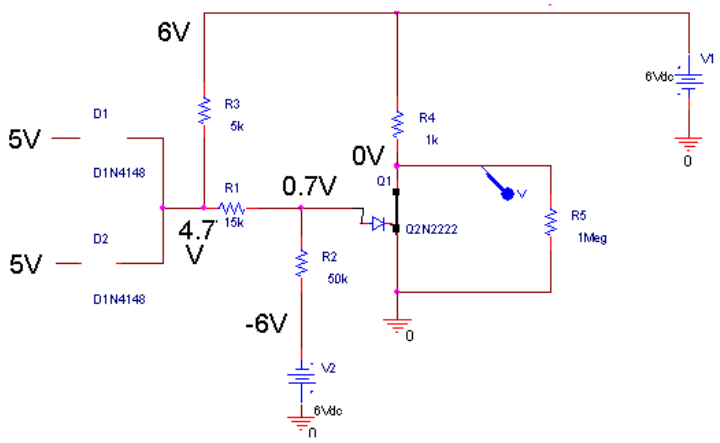
e. Explain your choice for d above*: (4 points)*

Case 1: left is 4.7V and right is .7V. For this case, both diodes are off and the transistor is on so that the base voltage must be .7V. Since the right point is connected to the base of the transistor, it must be the lower voltage.

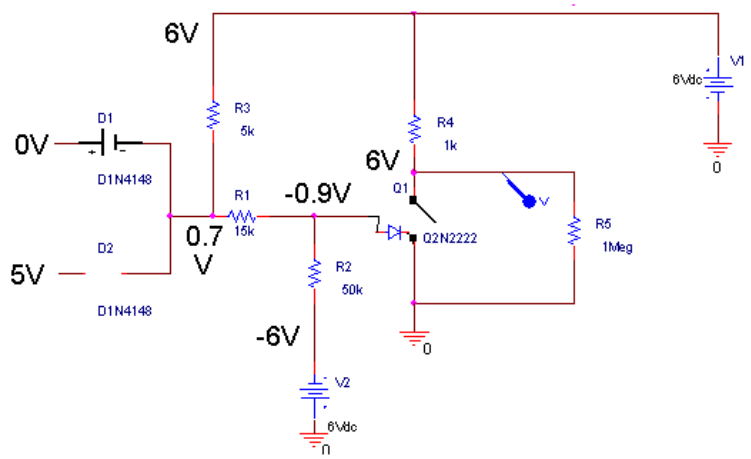
Case 2: left is .6V and right is -.9V. For this case, either diode is on, which connects the left voltage point to ground through the diode. Since it takes .6V to turn on the diode, the left must be at .6V

Extra Credit – Explain in detail how this circuit works for each of the four input combinations. *(1 point)*

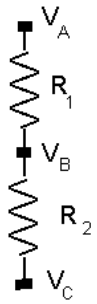
Case 1: Both inputs high. For this case, the diodes must be off. [In order for them to be on, the voltage across the diode must be less than –0.7]. Then we have the simple voltage divider circuit between 6V and .7V. The right voltage must be the voltage required to turn on the transistor (.7V) while the left voltage must be .7V+(15/20)(6-.7)=4.7V*



Case 2: Either input low or both low. For these cases, at least one of the diodes must be on. Then the diode will hold the voltage at the left point to 0.7V from the ground at the input. The right voltage is determined from the voltage divider relation (0.7-(-6))(15/65)=0.7-V → V=-0.9V



Note that there are two places on this test where a general voltage divider equation is used. Here is the general case:



The total voltage from V_A to V_C is V_A-V_C. This is the voltage we want to divide. This means that V_{R1}=[R1/(R1+R2)](V_A-V_C) and V_{R2}=[R2/(R1+R2)](V_A-V_C). It also means that the voltage at point B is given by
$V_B = V_C + V_{R2} = V_C + [R2/(R1+R2)](V_A - V_C)$.