ENGR4300
Fall 2005
Test 3C

Name_____

Section_____

Question 1 (25 points)_____

Question 2 (25 points) _____

Question 3 (25 points)_____

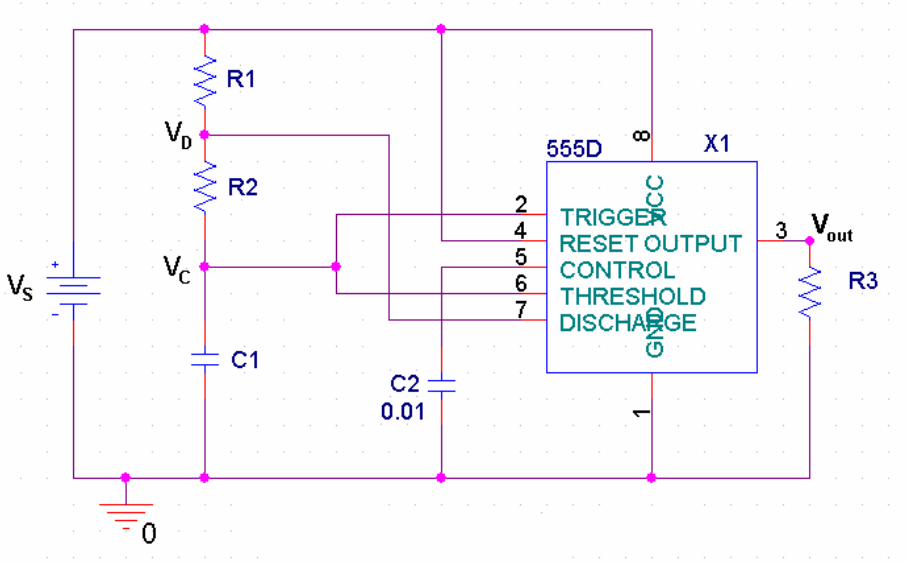
Question 4 (25 points)_____

Total (100 points): _____

Please do not write on the crib sheets.

On all questions: SHOW ALL WORK. BEGIN WITH FORMULAS, THEN SUBSTITUTE VALUES AND UNITS. No credit will be given for numbers that appear without justification.

Question 1 – Astable Multivibrator (25 points)



The multivibrator above was built with the 555 timer chip shown. In the diagram, Vs is the source voltage, Vc is the voltage across the capacitor C1, and V_D is the voltage at the discharge pin of the timer. You are given the following component values:
R1=6.8k ohms R2=8.6k ohms C1=0.47µF Vs=5V

1) Calculate the on time and off time of the multivibrator. (4 pt)

2) Calculate the frequency and period of the multivibrator. (4 pt)

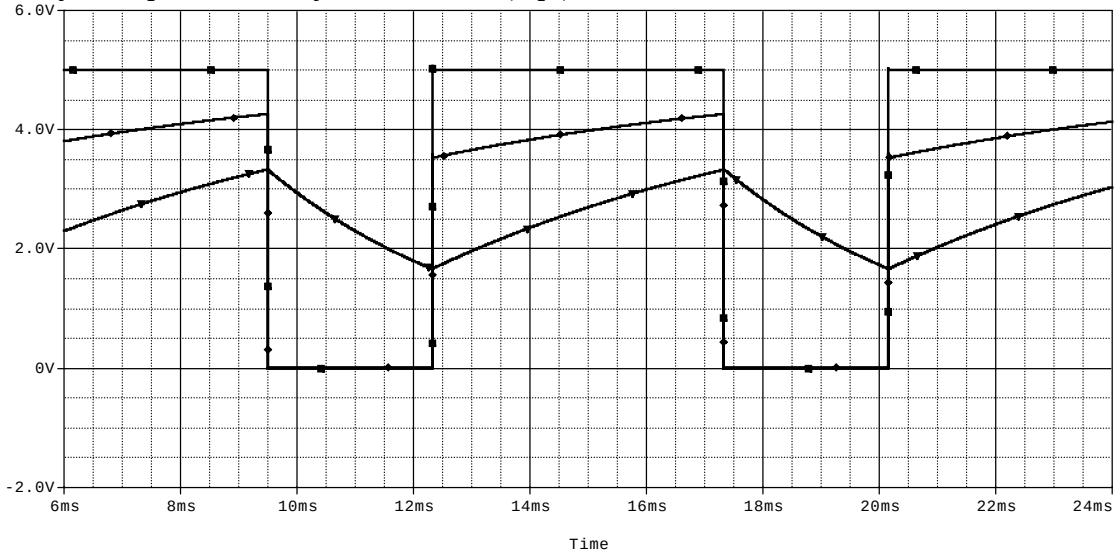
3) Calculate the duty cycle of the multivibrator. (2 pt)

4) In theory, what are the maximum and minimum voltage across the capacitor, Vc? (Please give numbers.) (2 pt)

5) When the transistor inside the 555 timer is closed, the output at pin 7 is grounded, and therefore, equal to zero. When the transistor is open, the output at pin 7 can be found using the voltage divider formed by R1 and R2. Find an expression for the voltage at pin 7 (when pin 7 is not grounded) in terms of the voltage across the capacitor, Vc, the source voltage, Vs, and the two resistors R1 and R2. [Hint: Recall how you calculate the voltage at the non-inverting input for a Schmitt trigger.] Do not substitute values. (3 pt)

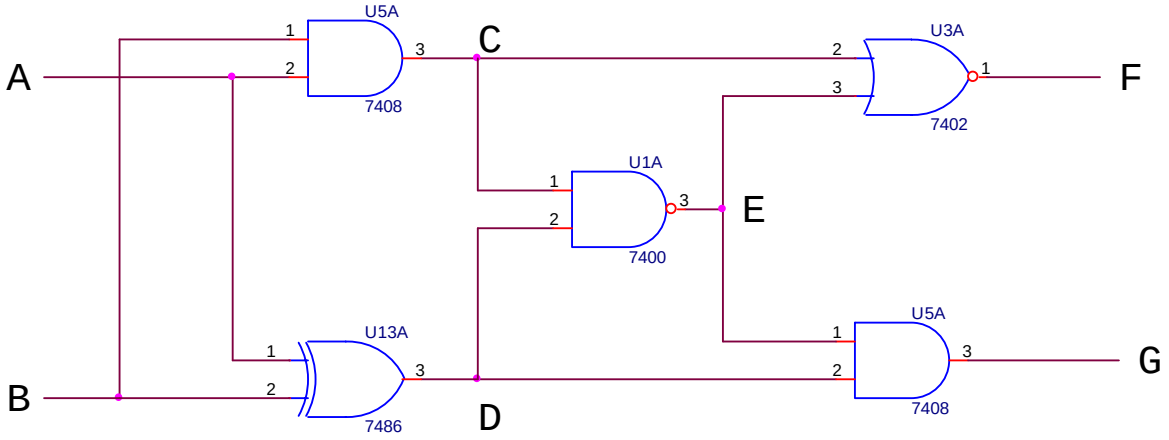
6) *Use the equation in 5)* to find the maximum and minimum voltage at pin 7 when the transistor is open. (2 pt)

7) On the graph below, identify the outputs at pin (2, 6), 7 and 3 of the multivibrator. Identify both parts of the cycle for each. (6 pt)



Question 2 – Combinational Logic Circuits (25 points)

1) You are given the following circuit



a) Fill out the truth table below (10 pt)

A	B	C	D	E	F	G
0	0					
0	1					
1	0					
1	1					

b) What gate is the output at G equivalent to (circle one)? (1 pt)

AND NAND OR NOR XOR XNOR NOT

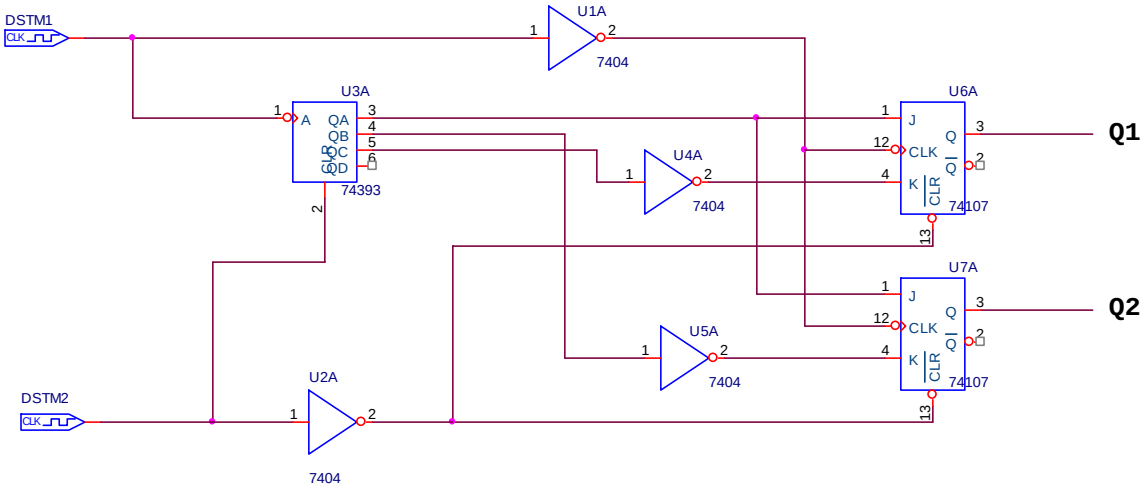
2) Fill out the truth table below to prove the following relationship: (14 pt)

if $Q = (\overline{A} + B) \bullet (A + \overline{B}) \bullet (A + B)$ *then* $Q = A \bullet B$

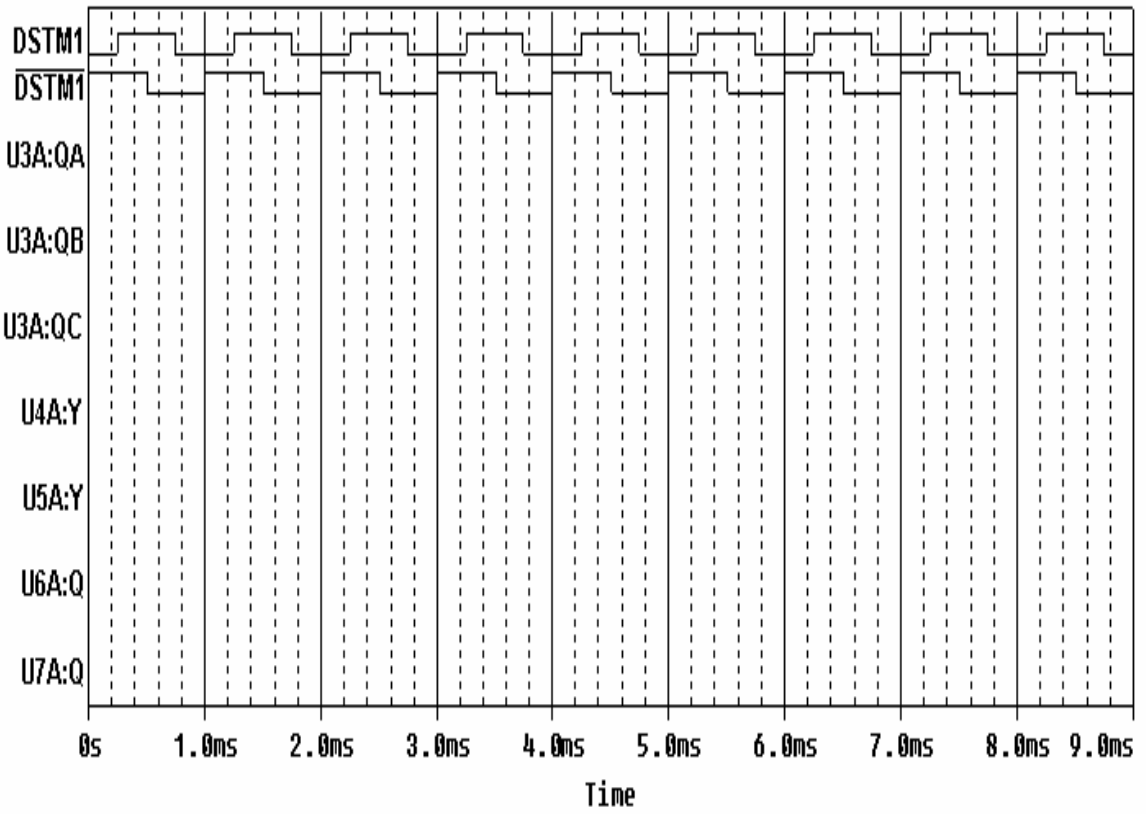
A	B	$\overline{A}$	$\overline{B}$	$\overline{A} + B$	$A + \overline{B}$	$A + B$	Q	$A \bullet B$
0	0							
0	1							
1	0							
1	1							

Question 3 – Sequential Logic Gates (25 points)

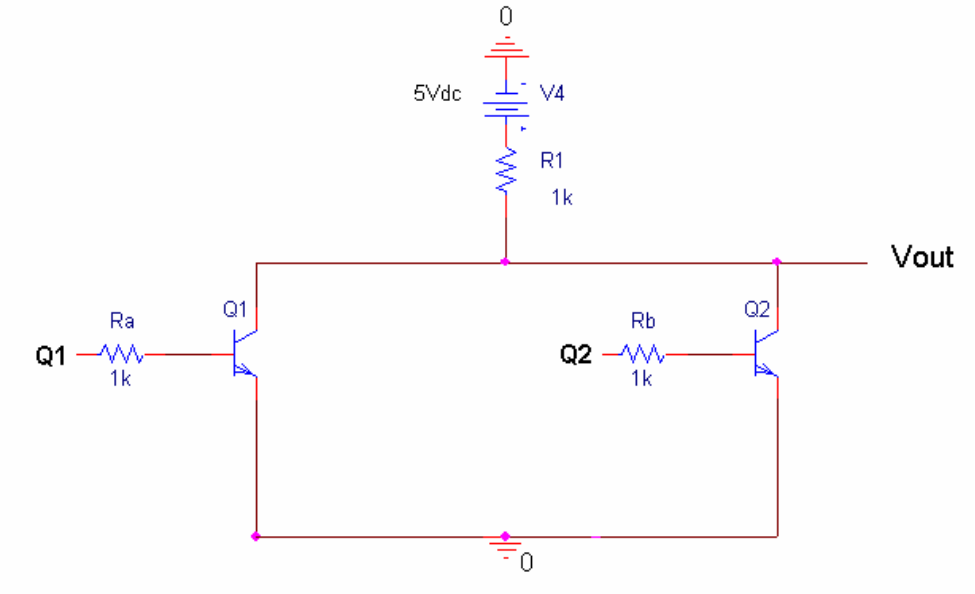
You are given the following circuit DSTM1 provides the clock for the counter. $\overline{DSTM1}$ provides the clock to the two flip flops. DSTM2 provides an initial reset pulse to all the sequential chips. Therefore, you can assume that QA, QB, QC, QD, Q1, and Q2 are all initially low.



1) Sketch the timing trace for each of the signals shown. (14 pt)



2) We take the output of this circuit and use it as the input to the transistor circuit shown below:



Fill in the following table for all possible values of Q1 and Q2. (4 pt)

Q1	Q2	Vout
0V	0V	
0V	5V	
5V	0V	
5V	5V	

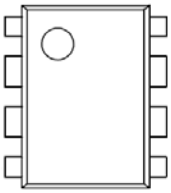
3) What are the values of the signals at Q1, Q2 and Vout after 8.9 milliseconds? (3 pt)

Q1:

Q2:

Vout:

4) IC chips have a standard numbering convention that you should now know. Label pins #1-8 on the IC below. (HINT: It doesn't matter what the chip's function is – just label #1, #2, …). (1 pt)



5) We've talked about the use of bypass capacitors when working with digital logic chips. Which answer below best describes where they should be located and why we use them? (1 pt)

a. Place one or more between digital logic inputs and ground to smooth the sharp transients of digital switching signals that could otherwise corrupt proper chip operation.
b. Place one or more in series with logic power (Vcc) where it enters the protoboard to filter noise coming from the power supply.
c. Place one or more in parallel with Vcc and ground at each chip to filter noise.
d. Place only one between Vcc and high speed logic chip outputs to suppress output oscillation (e.g. ringing).

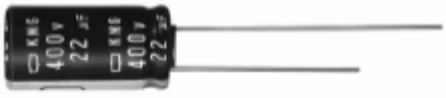
6) What was the recommended range of bypass capacitor values given for the TTL logic family used in the studio? (circle one) (1 pt)

a) 0.1pF – 0.5pF b) 0.01nF – 0.1nF c) 0.01uF – 0.1uF d) 0.1uF – 10uF

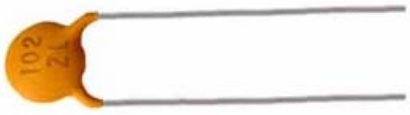
e) 10uF – 100uF f) I don't know because I slept through that lecture.

7) You've primarily used two types of capacitors in the studio: electrolytic and ceramic disc, each shown below:

Electrolytic:



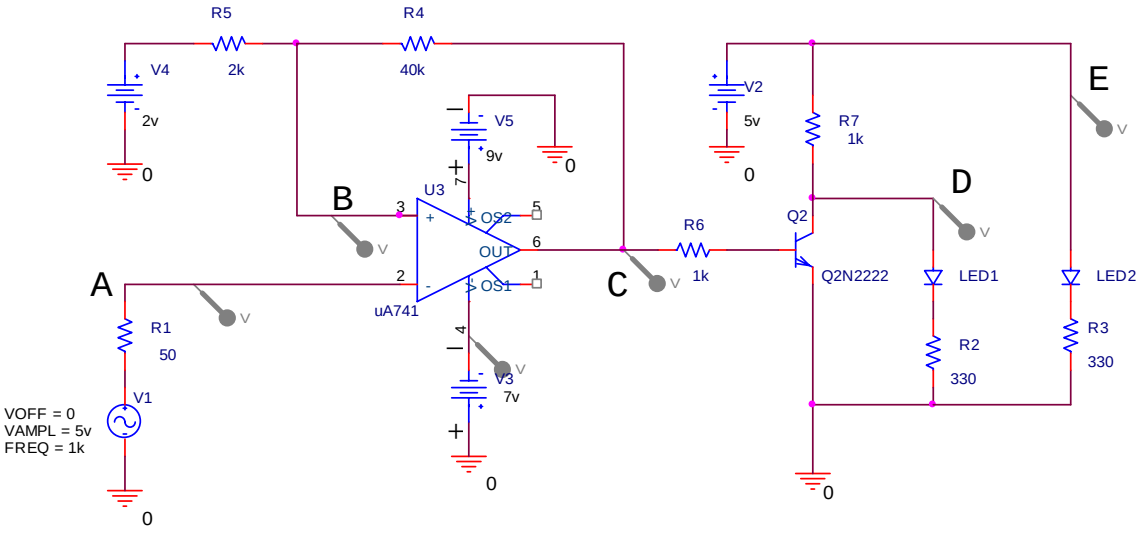
Ceramic Disc:



Which one is polarized (e.g. has a + and – lead) (circle one)? (1 pt)

neither electrolytic ceramic disc both

Question 4 – Switching Circuits (25 points)



1) In the circuit shown, circle the model of a Schmitt trigger. (1 pt)

2) What is the reference voltage of the Schmitt trigger model? (1 pt)

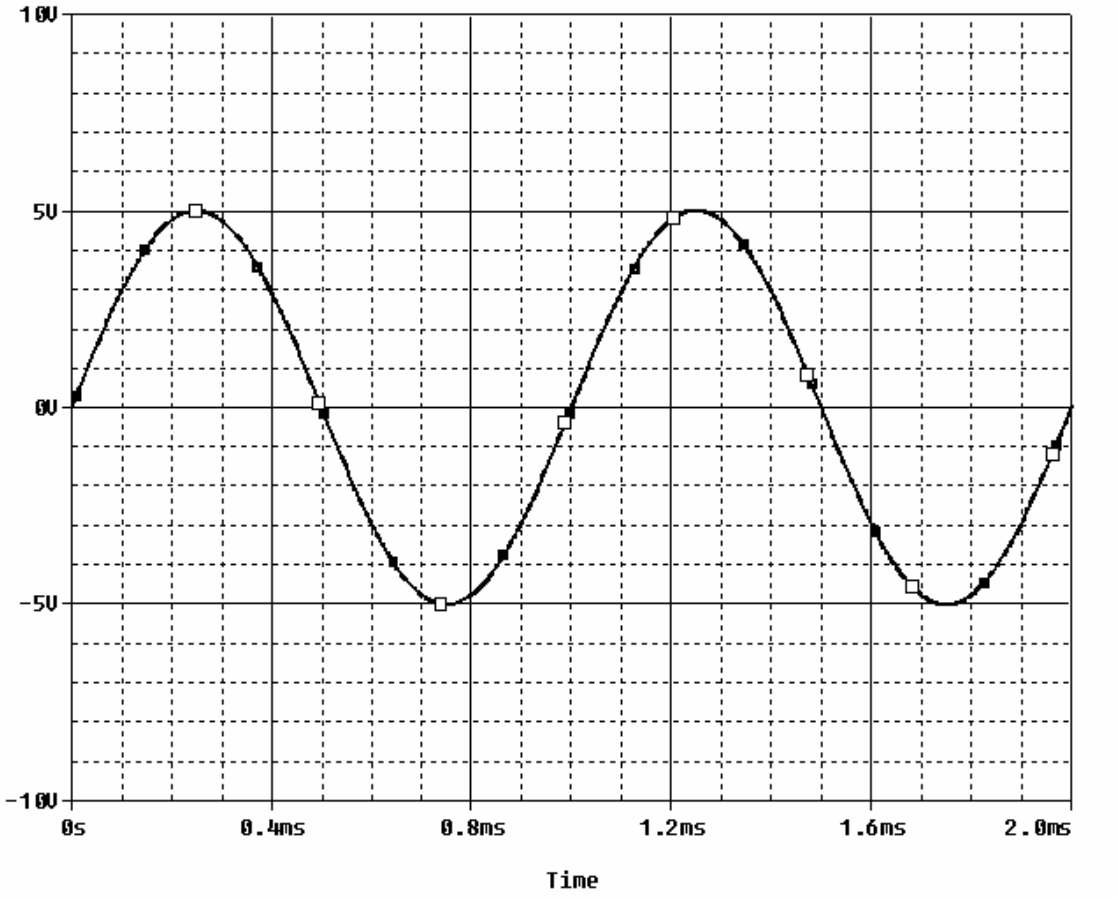
3) If the op-amp is putting out its maximum voltage at C, what is the voltage at point B, the non-inverting input to the op-amp? (3 pt)

4) If the op-amp is putting out is minimum voltage at point C, what is the voltage at point B, the non-inverting input to the op-amp? (3 pt)

5) On the following plot, the input at point A is shown.

a) Mark the upper and lower thresholds of the hysteresis (2 pt), and
b) sketch and label the output at points B, C, D and E for the input shown. (12 pt)

Many of the signals will overlap. Use the PSpice labeling convention to identify the signals by drawing unique symbols on *important parts* of each trace. Note that the input has a little box. Use the following: B = + C = × D = O and E = ◊.



8) Are the LEDs on or off at the following times? (3 pt)

time	LED1	LED2
0.3ms		
0.8ms		
1.2ms		