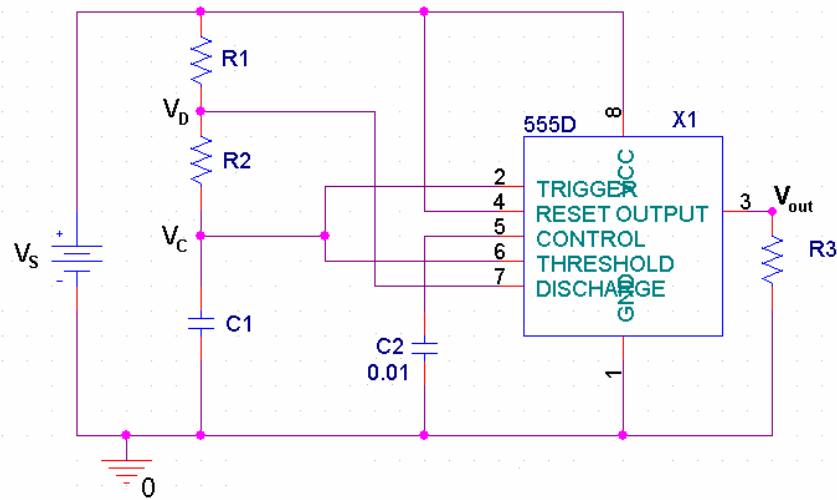


Question 1 – Astable Multivibrator (25 points)



The multivibrator above was built with the 555 timer chip shown. In the diagram, V_s is the source voltage, V_c is the voltage across the capacitor C_1 , and V_D is the voltage at the discharge pin of the timer. You are given the following component values:

Test A: $R_1 = 4.7\text{k ohms}$ $R_2 = 6.8\text{k ohms}$ $C_1 = 0.68\mu\text{F}$ $V_s = 6\text{V}$

Test B: $R_1 = 2.2\text{k ohms}$ $R_2 = 4.7\text{k ohms}$ $C_1 = 1.5\mu\text{F}$ $V_s = 12\text{V}$

Test C: $R_1 = 6.8\text{k ohms}$ $R_2 = 8.6\text{k ohms}$ $C_1 = 0.47\mu\text{F}$ $V_s = 5\text{V}$

1) Calculate the on time and off time of the multivibrator. (4 pt)

$$T_1 = 0.693(R_1 + R_2)C_1 \quad T_1 = 0.693(4.7\text{K} + 6.8\text{K})(0.68\mu) = 5.42\text{ms}$$

$$T_2 = 0.693(R_2)C_1 \quad T_2 = 0.693(6.8\text{k})(0.68\mu) = 3.20\text{ms}$$

Test A: $T_{on} = 5.42\text{ms}$ $T_{off} = 3.20\text{ms}$

Test B: $T_{on} = 7.17\text{ms}$ $T_{off} = 4.89\text{ms}$

Test C: $T_{on} = 5.02\text{ms}$ $T_{off} = 2.80\text{ms}$

2) Calculate the frequency and period of the multivibrator. (4 pt)

$$T = T_{on} + T_{off} \quad f = 1/T \quad T = 5.42\text{m} + 3.20\text{m} = 8.62\text{ms} \quad f = 1/8.62\text{m} = 116\text{Hz}$$

Test A: $T = 8.62\text{ms}$ $f = 116\text{ Hz}$

Test B: $T = 12.06\text{ms}$ $f = 82.9\text{ Hz}$

Test C: $T = 7.82\text{ms}$ $f = 128\text{ Hz}$

3) Calculate the duty cycle of the multivibrator. (2 pt)

$$DC = 100 * T_{on} / T \quad DC = 100 * 5.42\text{m} / 8.62\text{m} = 62.9\%$$

Test A: $DC = 62.9\%$

Test B: $DC = 59.5\%$

Test C: $DC = 64.2\%$

4) In theory, what are the maximum and minimum voltage across the capacitor, V_c ? (2 pt)

$$V_{min} = V_s/3 \quad V_{max} = 2*V_s/3 \quad V_{min}=6/3=2V \quad V_{max} = 2*6/3 = 4V$$

Test A: $V_{min} = 2V \quad V_{max} = 4V$

Test B: $V_{min} = 4V \quad V_{max} = 8V$

Test C: $V_{min} = 1.67V \quad V_{max} = 3.33V$

5) When the transistor inside the 555 timer is closed, the output at pin 7 is grounded, and therefore, equal to zero. When the transistor is open, the output at pin 7 can be found using the voltage divider formed by R_1 and R_2 . Find an expression for the voltage at pin 7 (when pin 7 is not grounded) in terms of the voltage across the capacitor, V_c , the source voltage, V_s , and the two resistors R_1 and R_2 . [Hint: Recall how you calculate the voltage at the non-inverting input for a Schmitt trigger.] Do not substitute values. (3 pt)

$$V_D = \left(\frac{R_2}{R_1 + R_2} \right) (V_s - V_C) + V_C$$

This can be simplified further, but it is not necessary.

6) Use the equation in 5) to find the maximum and minimum voltage at pin 7 when the transistor is open. (2 pt)

$$V_{Dlow} = [6.8k/(6.8k+4.7k)](6-2) + 2 = 4.36V$$

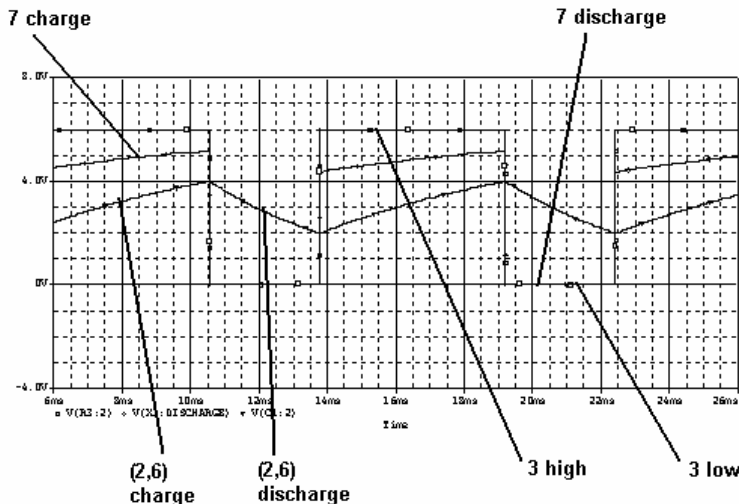
$$V_{Dhigh} = [6.8k/(6.8k+4.7k)](6-4) + 4 = 5.18V$$

Test A: $V_{Dlow} = 4.36V \quad V_{Dhigh} = 5.18V$

Test B: $V_{Dlow} = 9.44V \quad V_{Dhigh} = 10.72V$

Test C: $V_{Dlow} = 3.53V \quad V_{Dhigh} = 4.27V$

7) On the graph below, identify the outputs at pin (2, 6), 7 and 3 of the multivibrator. Identify both parts of the cycle for each. (6 pt)

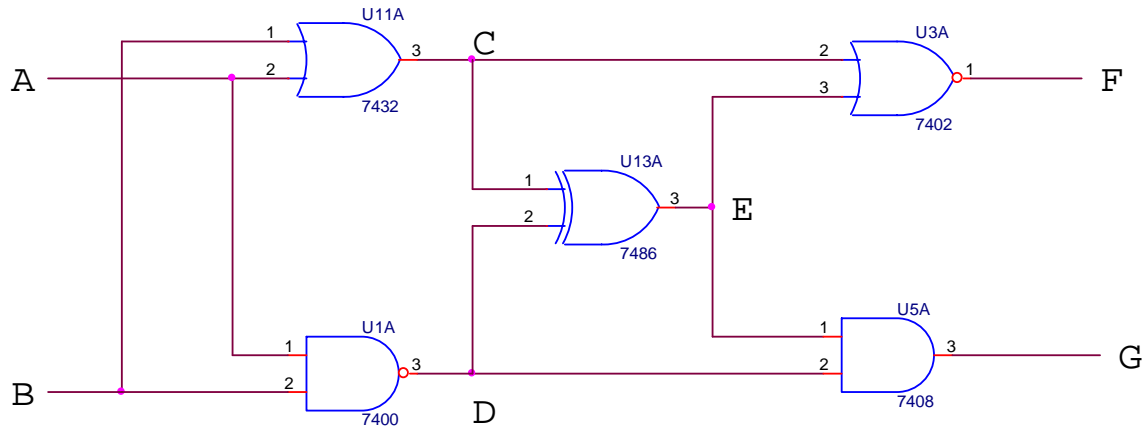


This shows the basic shape of the signals. The image on each test was different.

Question 2 – Combinational Logic Circuits (25 points)

Test A and B:

1) You are given the following circuit



a) Fill out the truth table below (10 pt)

A	B	C	D	E	F	G
0	0	0	1	1	0	1
0	1	1	1	0	0	0
1	0	1	1	0	0	0
1	1	1	0	1	0	0

b) What gate is the output at G equivalent to (circle one)? (1 pt)

AND NAND OR **NOR** XOR XNOR NOT

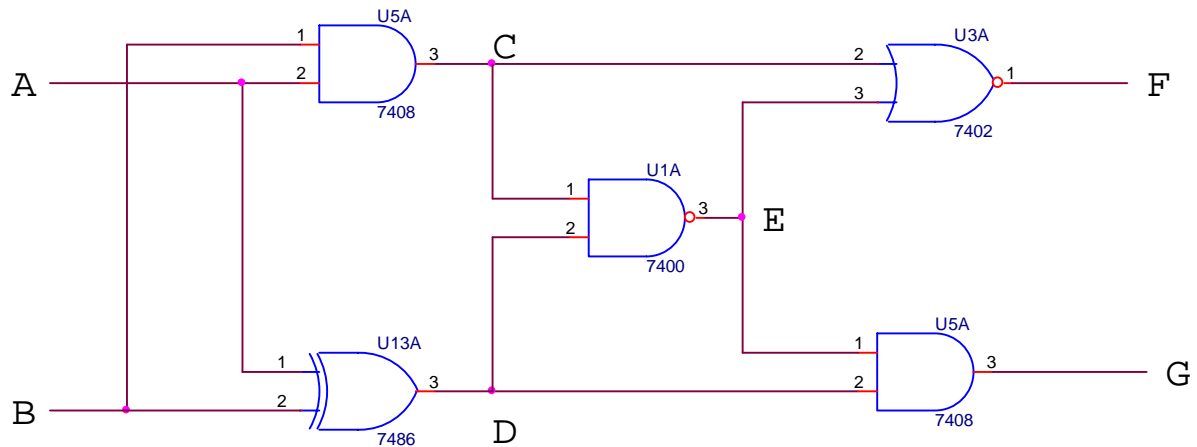
2) Fill out the truth table below to prove the following relationship: (14 pt)

if $Q = (\bar{A} \bullet B) + (A \bullet \bar{B}) + (A \bullet B)$ then $Q = A + B$

A	B	\bar{A}	\bar{B}	$\bar{A} \bullet B$	$A \bullet \bar{B}$	$A \bullet B$	Q	A+B
0	0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	1	1
1	0	0	1	0	1	0	1	1
1	1	0	0	0	0	1	1	1

Test C:

1) You are given the following circuit



a) Fill out the truth table below (10 pt)

A	B	C	D	E	F	G
0	0	0	0	1	0	0
0	1	0	1	1	0	1
1	0	0	1	1	0	1
1	1	1	0	1	0	0

b) What gate is the output at G equivalent to (circle one)? (1 pt)

AND NAND OR NOR **XOR** XNOR NOT

2) Fill out the truth table below to prove the following relationship: (14 pt)

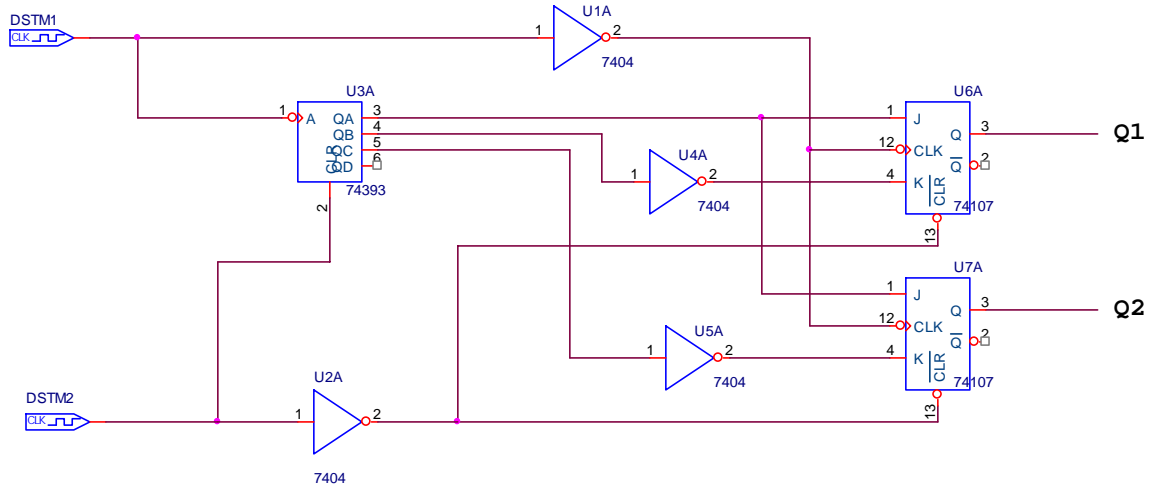
if $Q = (\bar{A} + B) \cdot (A + \bar{B}) \cdot (A + B)$ then $Q = A \cdot B$

A	B	\bar{A}	\bar{B}	$\bar{A} + B$	$A + \bar{B}$	$A + B$	Q	$A \cdot B$
0	0	1	1	1	1	0	0	0
0	1	1	0	1	0	1	0	0
1	0	0	1	0	1	1	0	0
1	1	0	0	1	1	1	1	1

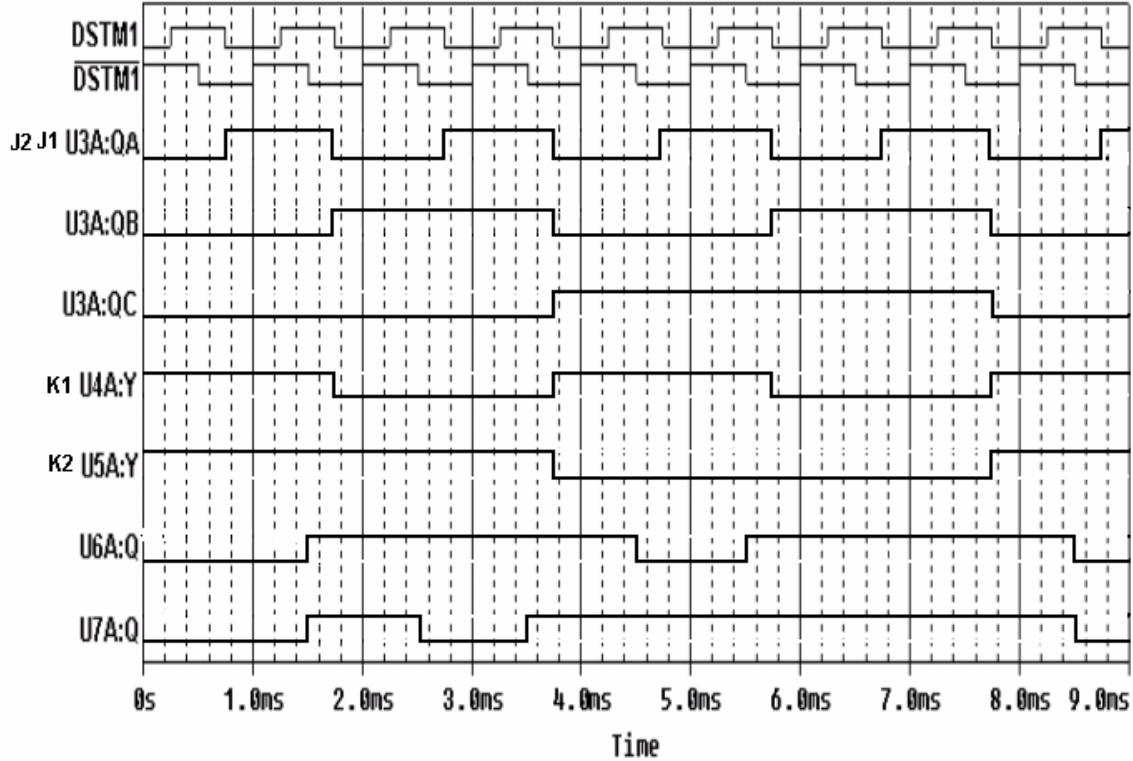
Question 3 – Sequential Logic Gates (25 points)

Quiz A and B:

You are given the following circuit. *DSTM1* provides the clock for the counter. *DSTM1* provides the clock to the two flip flops. *DSTM2* provides an initial reset pulse to all the sequential chips. Therefore, you can assume that QA, QB, QC, QD, Q1, and Q2 are all initially low.

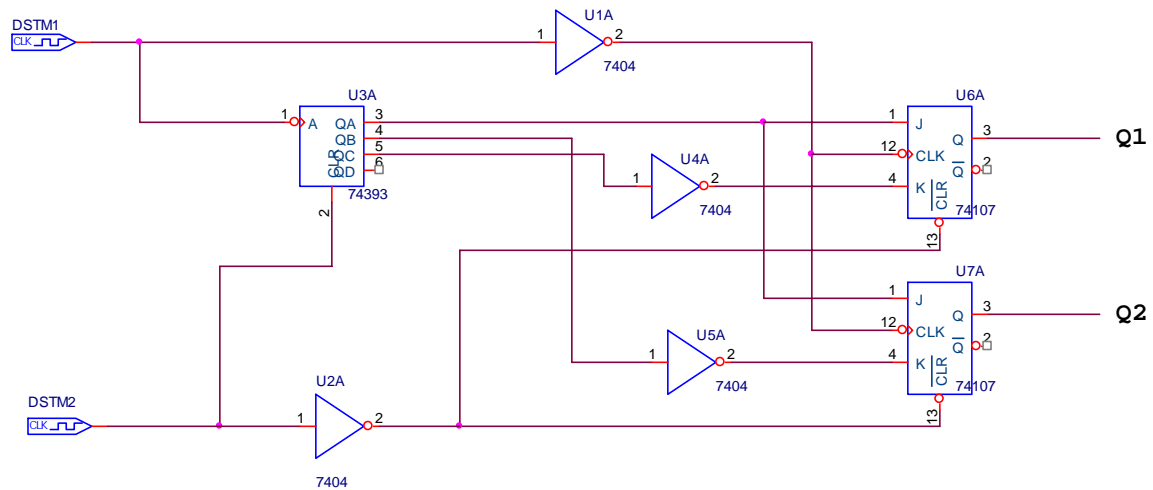


1) Sketch the timing trace for each of the signals shown. (14 pt)

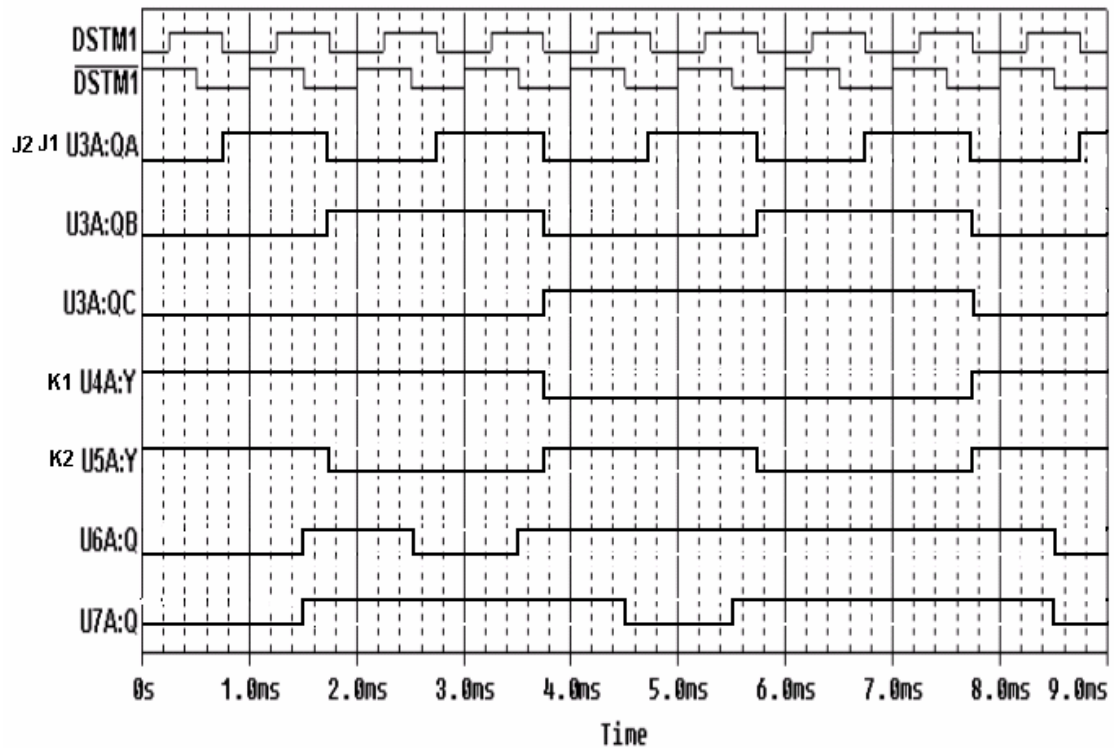


Quiz C:

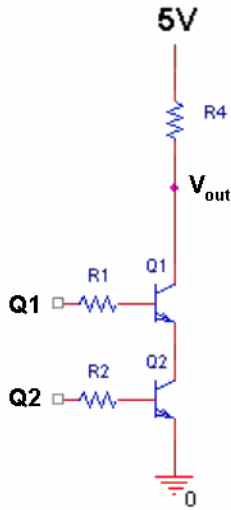
You are given the following circuit. $\overline{DSTM1}$ provides the clock for the counter. $\overline{DSTM1}$ provides the clock to the two flip flops. $\overline{DSTM2}$ provides an initial reset pulse to all the sequential chips. Therefore, you can assume that QA, QB, QC, QD, Q1, and Q2 are all initially low.



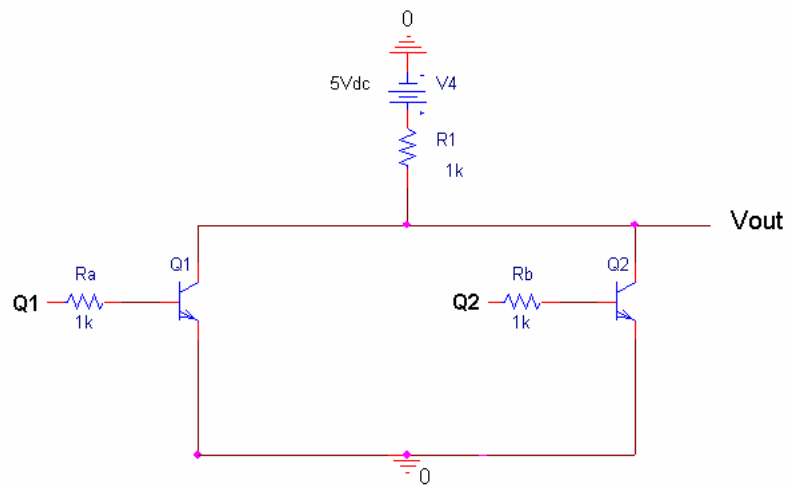
1) Sketch the timing trace for each of the signals shown. (14 pt)



2) We take the output of this circuit and use it as the input to the transistor circuit shown below:



Quiz A



Quiz B and C

Fill in the following table for all possible values of Q1 and Q2. (4 pt)

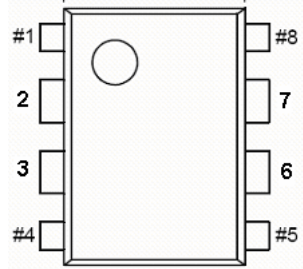
Quiz A			Quiz B and C		
Q1	Q2	Vout	Q1	Q2	Vout
0V	0V	5V	0V	0V	5V
0V	5V	5V	0V	5V	0V
5V	0V	5V	5V	0V	0V
5V	5V	0V	5V	5V	0V

3) What are the values of the signals at Q1, Q2 and Vout after 8.9 milliseconds? (3 pt)

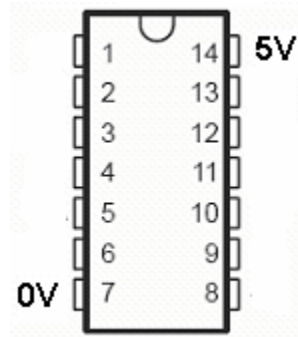
All Tests: Q1: 0V Q2: 0V Vout: 5V

Quiz A and B

4) IC chips have a standard numbering convention that you should now know. Label pins #1-8 on the IC below. (HINT: It doesn't matter what the chip's function is – just label #1, #2, ...). (1 pt)



5) Like op-amps, IC chips need two power connections in order to function. Label the power (V_{cc}) and ground pins on the 7404 IC chip pictured below with the appropriate *voltage values*. (1 pt)



6) The 7404 chip contains more than one inverter. How many does it contain? (1 pt)

6

7) You've primarily used two types of capacitors in the studio: electrolytic and ceramic disc, each shown below:

Electrolytic:



Ceramic Disc:

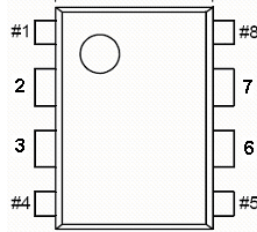


Which one is polarized (e.g. has a + and – lead) (circle one)? (1 pt)

- neither *electrolytic* ceramic disc both

Quiz C

4) IC chips have a standard numbering convention that you should now know. Label pins #1-8 on the IC below. (HINT: It doesn't matter what the chip's function is – just label #1, #2, ...). (1 pt)



5) We've talked about the use of bypass capacitors when working with digital logic chips. Which answer below best describes where they should be located and why we use them? (1 pt)

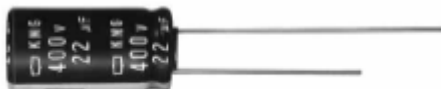
- Place one or more between digital logic inputs and ground to smooth the sharp transients of digital switching signals that could otherwise corrupt proper chip operation.
- Place one or more in series with logic power (V_{cc}) where it enters the protoboard to filter noise coming from the power supply.
- Place one or more in parallel with V_{cc} and ground at each chip to filter noise.**
- Place only one between V_{cc} and high speed logic chip outputs to suppress output oscillation (e.g. ringing).

6) What was the recommended range of bypass capacitor values given for the TTL logic family used in the studio? (circle one) (1 pt)

- a) 0.1pF – 0.5pF b) 0.01nF – 0.1nF **c) 0.01 μ F – 0.1 μ F** d) 0.1 μ F – 10 μ F
 e) 10 μ F – 100 μ F f) I don't know because I slept through that lecture.

7) You've primarily used two types of capacitors in the studio: electrolytic and ceramic disc, each shown below:

Electrolytic:



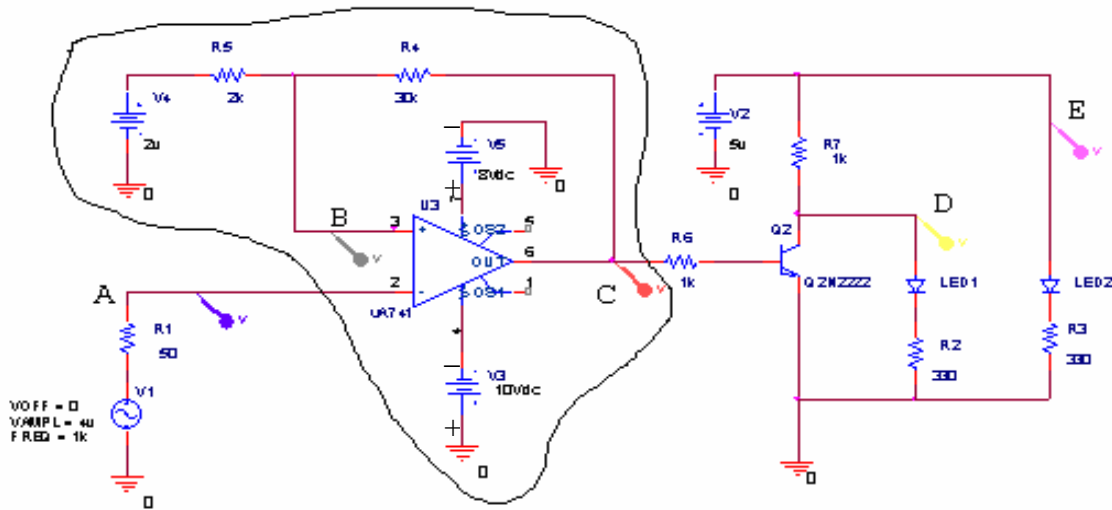
Ceramic Disc:



Which one is polarized (e.g. has a + and – lead) (circle one)? (1 pt)

- neither **electrolytic** ceramic disc both

Question 4 – Switching Circuits (25 points)



Quiz A: V1=4V V3= -10V V4=2V V5=8V R4=30k R5=2k
 Quiz B: V1=6V V3= -8V V4=3V V5=10V R4=20k R5=1k
 Quiz C: V1=5V V3= -7V V4=2V V5=9V R4=40k R5=2k

- 1) In the circuit shown, circle the model of a Schmitt trigger. (1 pt)
- 2) What is the reference voltage of the Schmitt trigger model? (1 pt)

Test A: $V_{ref} = 2V$ Test B: $V_{ref} = 3V$ Test C: $V_{ref} = 2V$

- 3) If the op-amp is putting out its maximum voltage at C, what is the voltage at point B, the non-inverting input to the op-amp? (3 pt)

$$v_+ = \left(\frac{R_2}{R_1 + R_2} \right) (v_{out} - V_{ref}) + V_{ref} \quad v_+ = [2k/(2k+30k)](8-2) + 2 = 2.375V$$

Test A: $v_+ = 2.38V$ Test B: $v_+ = 3.33V$ Test C: $v_+ = 2.33V$

- 4) If the op-amp is putting out its minimum voltage at point C, what is the voltage at point B, the non-inverting input to the op-amp? (3 pt)

$$v_+ = \left(\frac{R_2}{R_1 + R_2} \right) (v_{out} - V_{ref}) + V_{ref} \quad v_+ = [2k/(2k+30k)](-10 - 2) + 2 = 1.25V$$

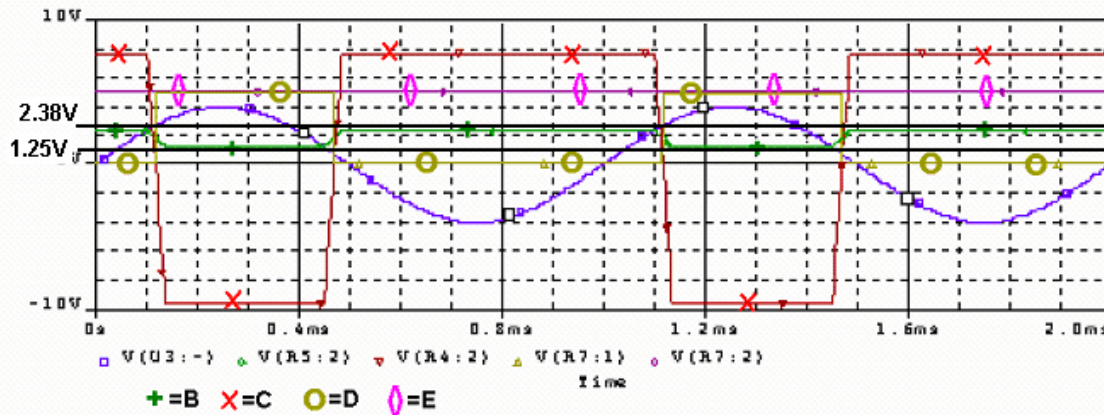
Test A: $v_+ = 1.25V$ Test B: $v_+ = 2.48V$ Test C: $v_+ = 1.57V$

5) On the following plot, the input at point A is shown.

- a) Mark the upper and lower thresholds of the hysteresis (2 pt), and
- b) sketch and label the output at points B, C, D and E for the input shown. (12 pt)

Many of the signals will overlap. Use the PSpice labeling convention to identify the signals by drawing unique symbols on *important parts* of each trace. Note that the input has a little box. Use the following: B = + C = × D = O and E = ◇.

This plot shows the basic shape of the signals for all three tests. Specific high and low values are given below.



*Test A: Signals change when input rises above 2.38V or falls below 1.25V
 Signal B toggles between 1.25 and 2.38 volts. (H-L-H-L-H)
 Signal C toggles between +8V and -10V (H-L-H-L-H)*

*Test B: Signals change when input rises above 3.33V or falls below 2.48V
 Signal B toggles between 2.48 and 3.33 volts. (H-L-H-L-H)
 Signal C toggles between +10V and -8V (H-L-H-L-H)*

*Test C: Signals change when input rises above 2.33V or falls below 1.57V
 Signal B toggles between 1.57 and 2.33 volts. (H-L-H-L-H)
 Signal C toggles between +9V and -7V (H-L-H-L-H)*

*All Tests: Signal D toggles between 0V and some voltage less than 5V (L-H-L-H-L)
 (You do not know enough about diodes to know the exact voltage, so we accepted anything in this range that was recognizable as not zero.)
 Signal E is constant at 5V*

8) Are the LEDs on or off at the following times (3 points)?

time	LED1	LED2
0.3ms	ON	ON
0.8ms	OFF	ON
1.2ms	ON	ON