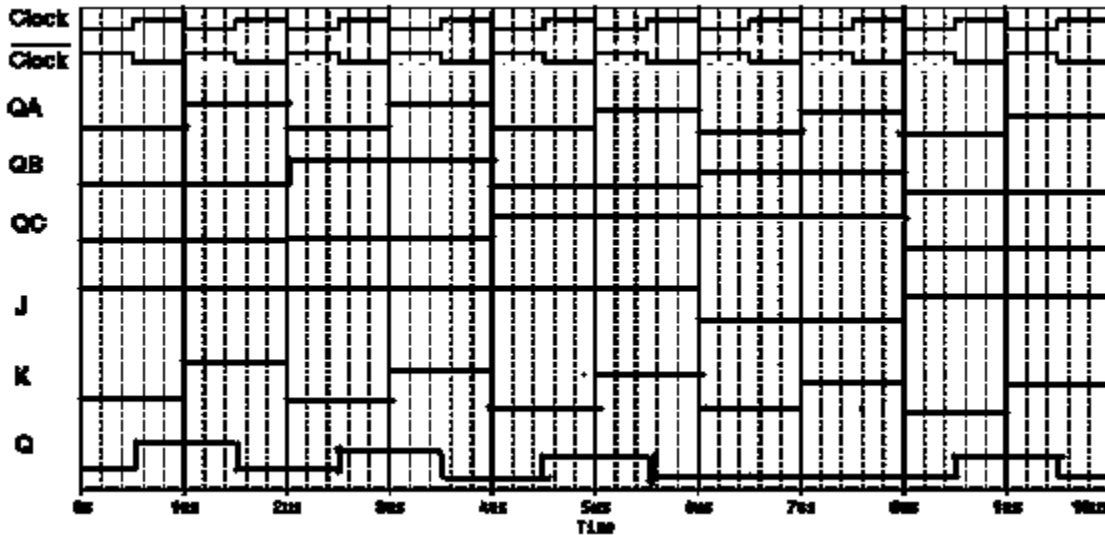
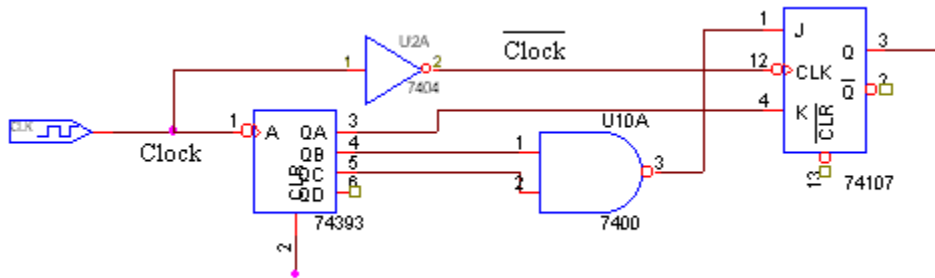


**Question 1) Flip Flops and Counters (15 points)**

- a) Fill in the truth table for a JK flip flop. Use  $Q_0$  or  $\overline{Q}_0$  to denote the previous value of Q and  $\overline{Q}$ . (6 pts)

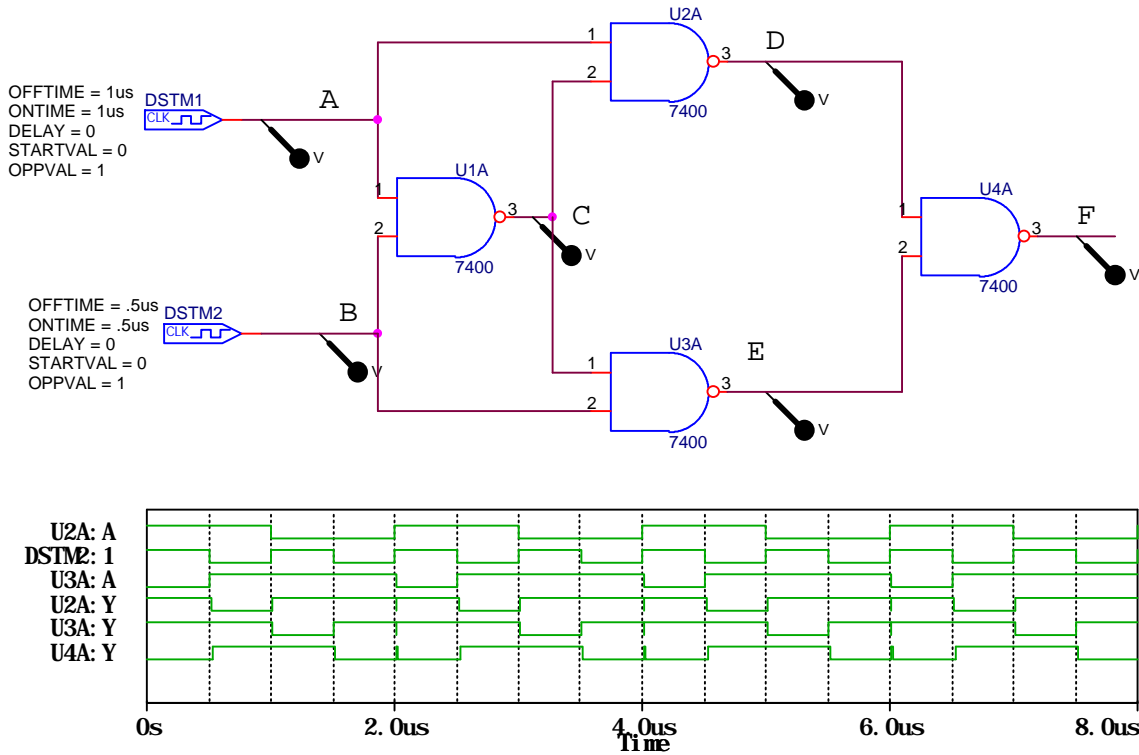
J	K	CLK	Q	$\overline{Q}$
0	0	$\lrcorner$	Q	$\overline{Q}$
0	1	$\lrcorner$	0	1
1	0	$\lrcorner$	1	0
1	1	$\lrcorner$	$\overline{Q}$	Q

- b) In Figure 1a we show a counter connected to the inputs of a JK flip flop. Draw the output versus time at each of the points specified in the diagram below. Assume that initially both the counter and the JK flip flop are cleared (i.e., at time 0:  $Q_A=0$ ,  $Q_B=0$ ,  $Q_C=0$ ,  $Q_D=0$ ,  $Q_0=0$ , and  $\overline{Q}_0=1$ ). Note that since both the counter and the flip flop trigger on the falling edge of the clock, we have added an inverter to one of them to prevent race conditions. (9 pts)



**Question 2) NAND Gate Circuit (15 points)**

Below is a picture of a series of NAND gates hooked together to form one of the basic gates we have studied and the PSpice output for the circuit.



a) Fill in the truth table for the circuit (9 pts).

A	B	C	D	E	F
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

b) What gate does this represent (2 pts)?

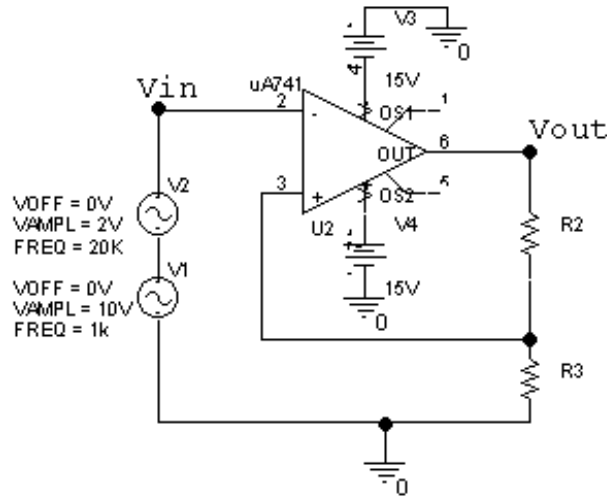
**XOR**

c) Write a boolean expression for this circuit. Do not simplify. (4 pts).

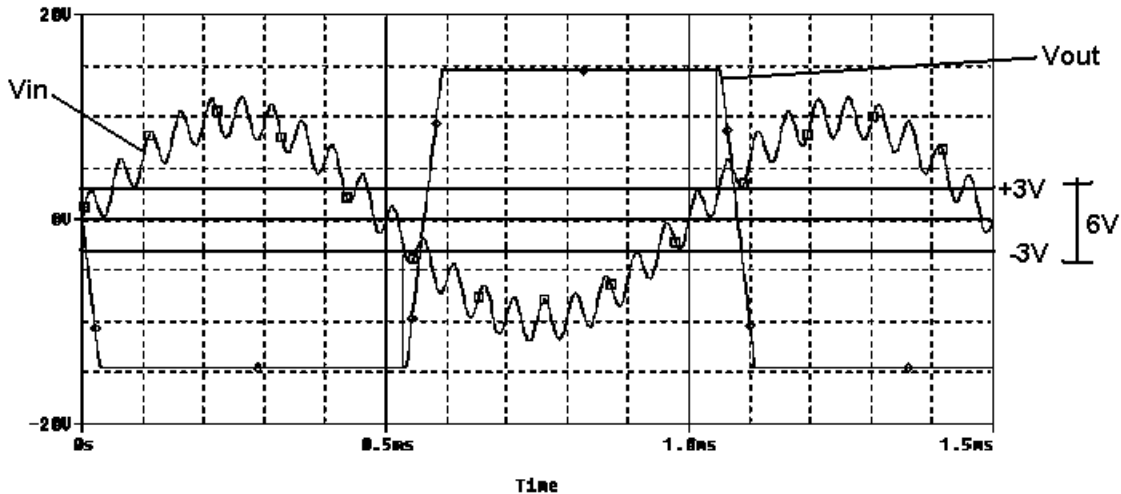
$$\overline{[(A \bullet B) \bullet A]} \bullet \overline{[(A \bullet B) \bullet B]}$$

**Question 3) Schmitt Trigger Model (25 Points)**

Below is a model of a Schmitt trigger, which uses an op amp and two voltage sources. The first source, V1, represents the source voltage and the second source, V2, represents noise on the signal. The plot below the circuit is the PSpice output from this circuit.



a) Indicate  $V_{in}$  and  $V_{out}$  for the model of a Schmitt trigger above on the output plot below (4 pts).



b) Estimate the value of the hysteresis for the Schmitt trigger model AND indicate the hysteresis range on the output plot. (8 pts).

*The point of transition seems to be at +3 volts and -3 volts. This makes the hysteresis 6 volts. (Answers may vary from about +/-2 to +/-4 depending on your interpretation.)*

c) What is the saturation voltage range of the op-amp in the model? (4 pts)

*The amp saturates at +14.6 is the positive and -14.6 in the negative. (Answers may vary, they should be consistent with the plot.) If there is no plot given, a saturation range from +/-14 (book) to +/-15(class) is acceptable.*

d) If R2 is 120K ohms, then what does R3 have to be to give results similar to the output plot pictured.? (9 pts)

$$[R3/(R2+R3)] V_{out} = V_{ref} \quad V_{ref} = \pm 3V \quad V_{out} = \pm 14.6V$$

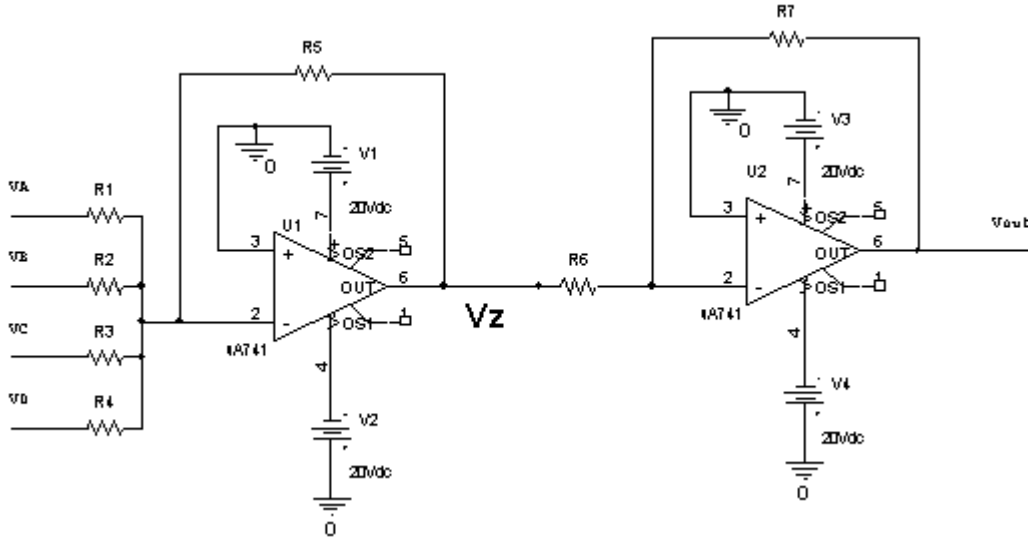
$$[R3/(120+R3)](14.6) = 3 \quad 14.6R3 = 3(120K+R3) \quad 11.6R3 = 360K \quad R3 = 31K \text{ ohms}$$

$$R3 = 31K \text{ ohms}$$

*(This answer depends on part b and part c, so answers will vary.)*

**Question 4) Digital-to-Analog Converter (20 points)**

The circuit below is a “Voltage Adder” followed by an “Inverting Op-Amp”, that converts digital signals into analog signals. This circuit produces an analog output voltage equal to the binary word ABCD in terms of the four inputs. Please assume that the input voltage levels for this circuit is 5 Volts for a logic of “one” and 0 Volts for a logic “zero” and that  $R5 = 15K\Omega$ ,  $R6 = 2K\Omega$  and  $R7 = 10K\Omega$ .



a) Select values for  $R1$ ,  $R2$ ,  $R3$ , and  $R4$  so that the output voltage will be the decimal equivalent of ABCD. For example, if  $ABCD=1010$ , or equivalently  $V_A=V_C=5\text{ V}$ ,  $V_B=V_D=0\text{ V}$ , then  $V_{out} = 10\text{ V}$ . The circuit should work for **all** possible ABCD combinations. (12 points)

$$V_{out} = -(R7/R6)V_z \quad V_z = -(R5/R1)V_A - (R5/R2)V_B - (R5/R3)V_C - (R5/R4)V_D$$

$$V_{out} = (R7 \times R5 / R6) [(V_A/R1) + (V_B/R2) + (V_C/R3) + (V_D/R4)]$$

$$(R7 \times R5 / R6) = 10K \times 15K / 2K = 75K$$

$V_{out}$	$V_A$	$V_B$	$V_C$	$V_D$	Equation	Result
1V	0	0	0	5V	$1V = 75K(5V/R4)$	$R4 = 375K\text{ ohms}$
2V	0	0	5V	0	$2V = 75K(5V/R3)$	$R3 = 187.5K\text{ ohms}$
4V	0	5V	0	0	$4V = 75K(5V/R2)$	$R2 = 93.75K\text{ ohms}$
8V	5V	0	0	0	$8V = 75K(5V/R1)$	$R1 = 46.875K\text{ ohms}$

$$R1 = 46.875K\text{ ohms} \quad R2 = 93.75K\text{ ohms} \quad R3 = 187.5K\text{ ohms} \quad R4 = 375K\text{ ohms}$$

b) What is the maximum binary input (ABCD=?) to this circuit (4 points)?

$$ABCD = 1111 \text{ (15 in decimal)}$$

c) Show that your selection of resistors above is correct by comparing the calculated  $V_{out}$  with the maximum digital input (4 points)

$$V_{out} = (R7 \times R5 / R6) [(VA/R1) + (VB/R2) + (VC/R3) + (VD/R4)]$$

$$V_{out} = 15V = 75K [(5V/46.875K) + (5V/93.75K) + (5V/187.5K) + (5V/375K)] ?$$

$$15V = 75 [0.107 + 0.053 + 0.027 + 0.013] = 75K \times 0.2m = 15 ?$$

*15=15 It checks.*

Question 5) Transistors (25 points)

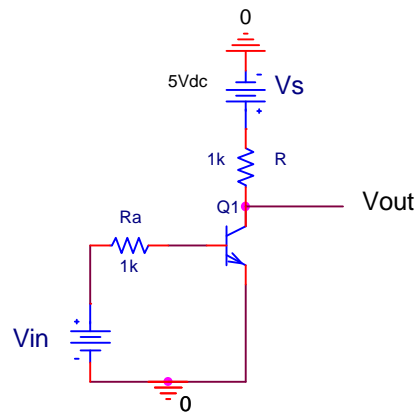
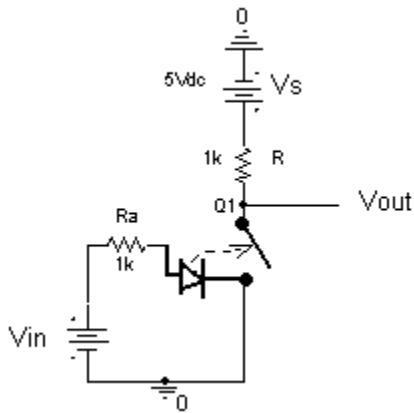
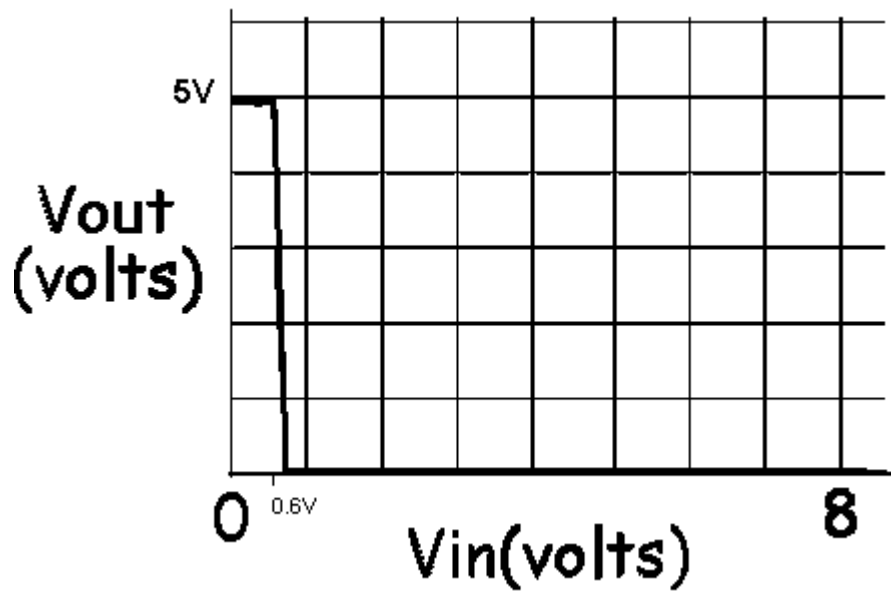


Figure 5a: Transistor as a Switch

a) Redraw Figure 5a with the transistor modeled as switch and a diode. (4 points)



b) Draw the  $V_{out}$  as a function of  $V_{in}$  assuming the transistor behaves as it appears in your model in part (a). (4 points)



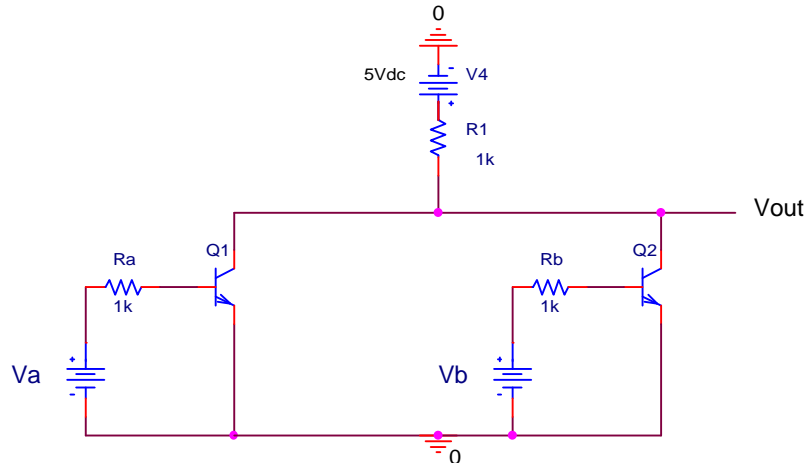
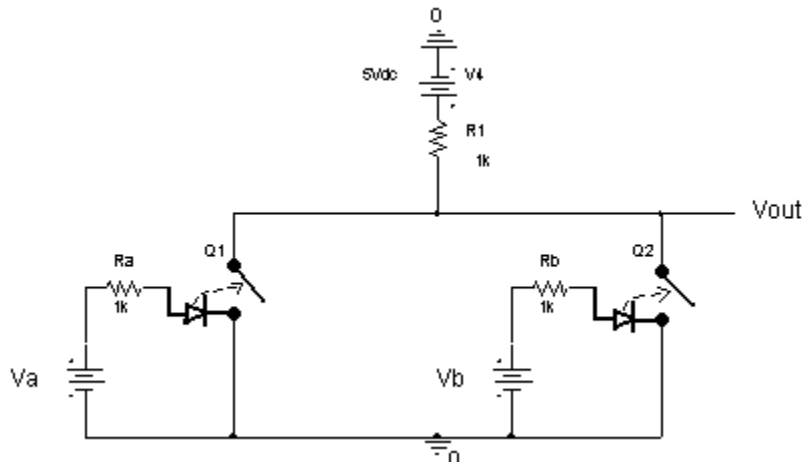


Figure 5b

- c) Redraw the circuit in Figure 5b with the transistors modeled as switches and diodes. (6 points)



- d) Fill in the following table of  $V_{out}$  as a function of  $V_a$  and  $V_b$  based on the model you gave in part c. (6 points)

$V_a$	$V_b$	$V_{out}$
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

- e) What kind of gate is this? (5 points)

- AND
- NAND
- OR
- NOR**
- XOR
- None of the above