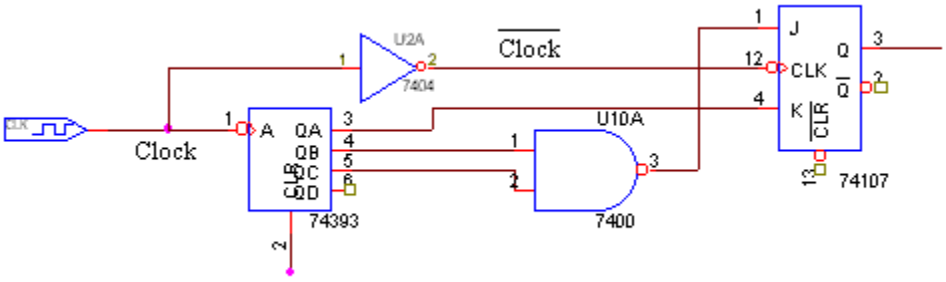
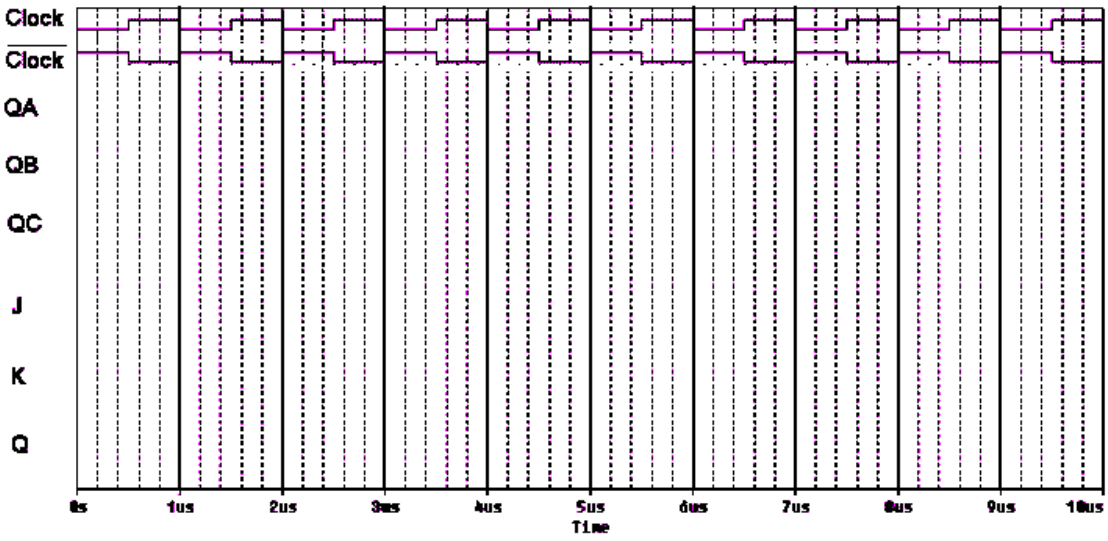
Question 1) Flip Flops and Counters (15 points)

a) Fill in the truth table for a JK flip flop. Use Q_0 or $\overline{Q}_0$ to denote the previous value of Q and $\overline{Q}$. (6 pts)

J	K	CLK	Q	$\overline{Q}$
		⌐		
		⌐		
		⌐		
		⌐		

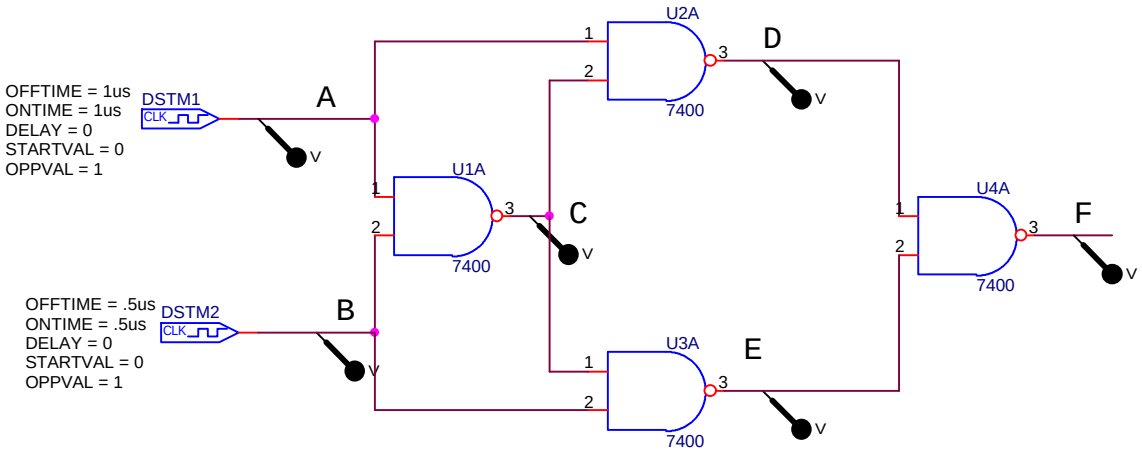
b) In Figure 1a we show a counter connected to the inputs of a JK flip flop. Draw the output versus time at each of the points specified in the diagram below. Assume that initially both the counter and the JK flip flop are cleared (i.e., at time 0: QA=0, QB=0, QC=0, QD=0, Q_0=0, and $\overline{Q}_0$ =1) . Note that since both the counter and the flip flop trigger on the falling edge of the clock, we have added an inverter to one of them to prevent race conditions. (9 pts)

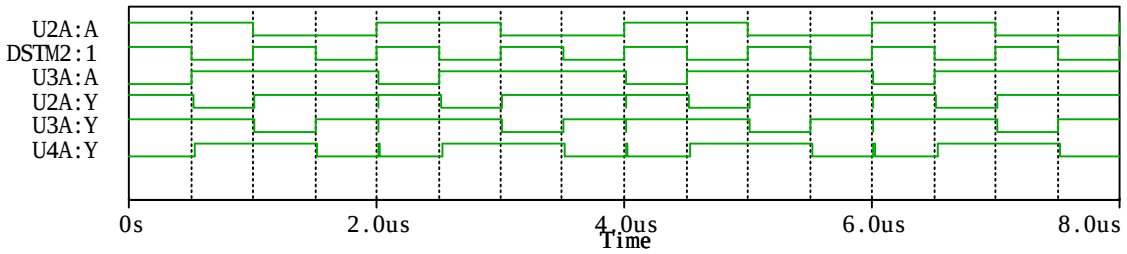




Question 2) NAND Gate Circuit (15 points)

Below is a picture of a series of NAND gates hooked together to form one of the basic gates we have studied and the PSpice output for the circuit.





a) Fill in the truth table for the circuit (9 pts).

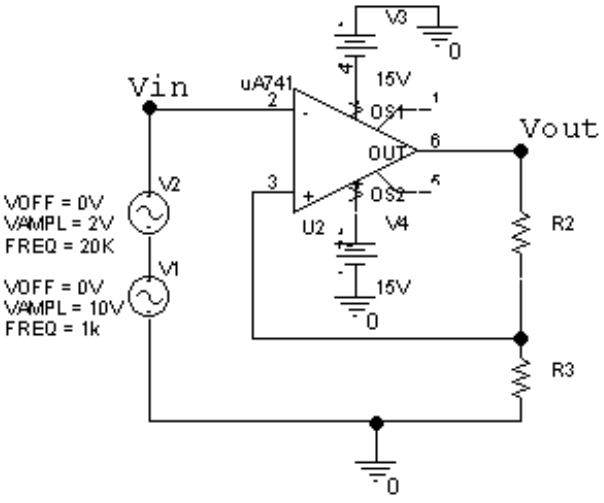
A	B	C	D	E	F

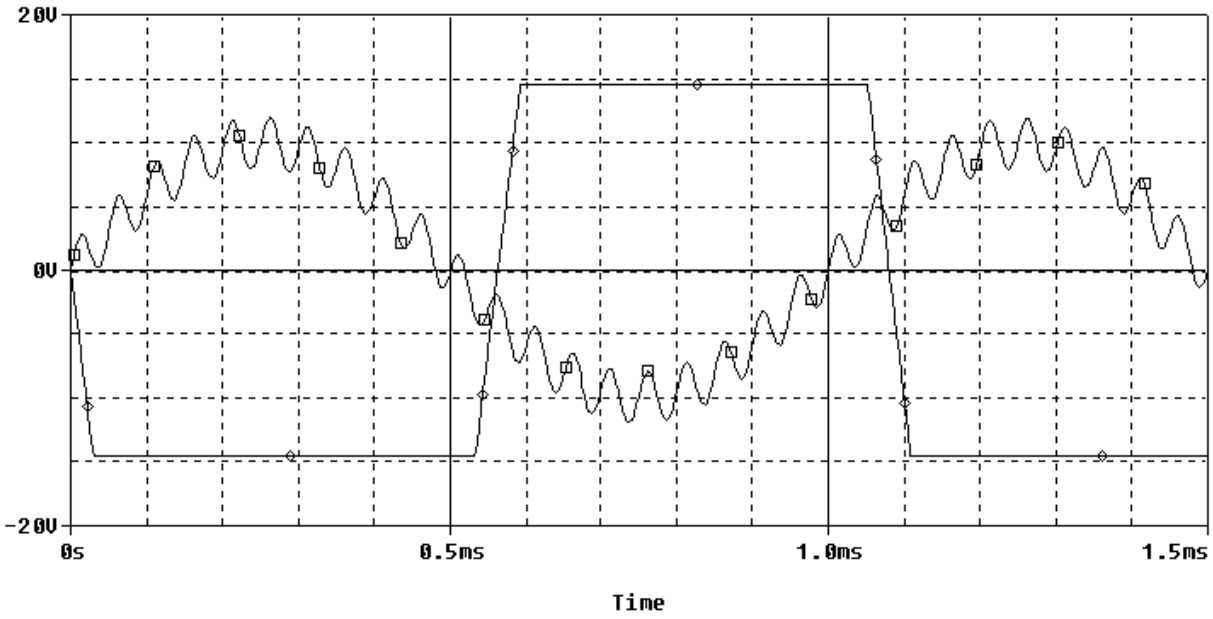
b) What gate does this represent (2 pts)?

c) Write a boolean expression for this circuit. Do not simplify. (4 pts).

Question 3) Schmitt Trigger Model (25 Points)

Below is a model of a Schmitt trigger, which uses an op amp and two voltage sources. The first source, V1, represents the source voltage and the second source, V2, represents noise on the signal. The plot below the circuit is the PSpice output from this circuit.





a) Indicate Vin and Vout for the model of a Schmitt trigger above on the output plot below (4 pts).

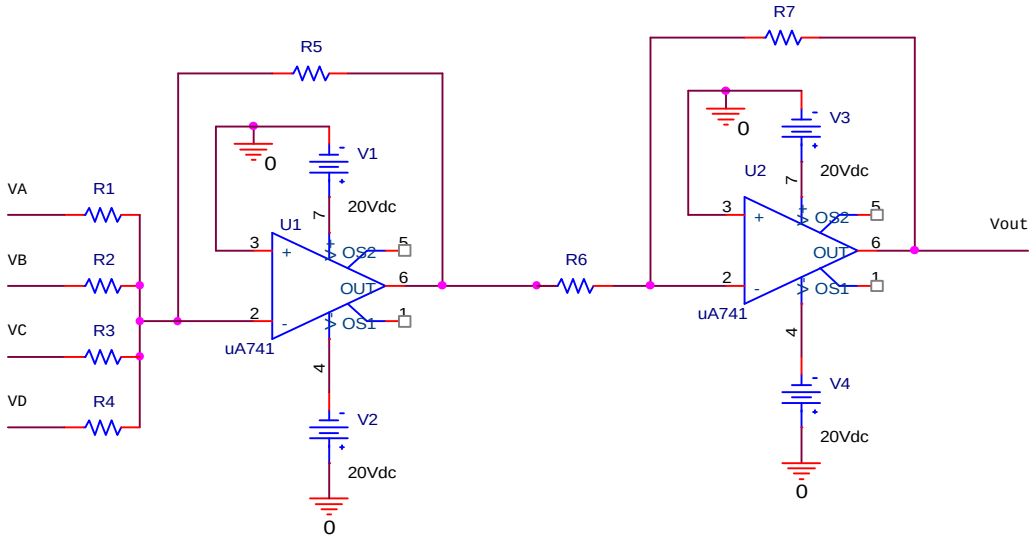
b) Estimate the value of the hysteresis for the Schmitt trigger model AND indicate the hysteresis range on the output plot. (8 pts).

c) What is the saturation voltage range of the op-amp in the model? (4 pts)

e) If R2 is 120K ohms, then what does R3 have to be to give results similar to the output plot pictured.? (9 pts)

Question 4) Digital-to-Analog Converter (20 points)

The circuit below is a "Voltage Adder" followed by an "Inverting Op-Amp", that converts digital signals into analog signals. This circuit produces an analog output voltage equal to the binary word ABCD in terms of the four inputs. Please assume that the input voltage levels for this circuit is 5 Volts for a logic of "one" and 0 Volts for a logic "zero" and that R5 = 15KΩ, R6 = 2KΩ and R7 = 10KΩ.



a) Select values for R1, R2, R3, and R4 so that the output voltage will be the decimal equivalent of ABCD. For example, if ABCD=1010, or equivalently VA=VC=5 V, VB=VD=0 V, then Vout = 10 V. The circuit should work for **all** possible ABCD combinations. (12 points)

R1 = R2 = R3 = R4 =

b) What is the maximum binary input (ABCD=?) to this circuit (4 points)?

c) Show that your selection of resistors above is correct by comparing the calculated Vout with the maximum digital input (4 points)

Question 5) Transistors (25 points)

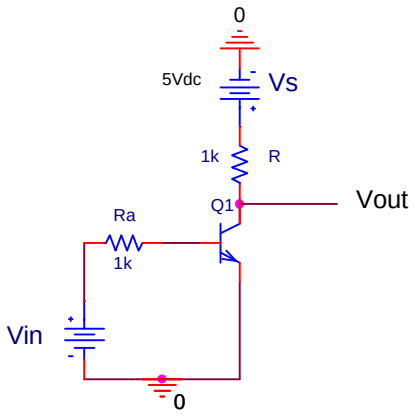
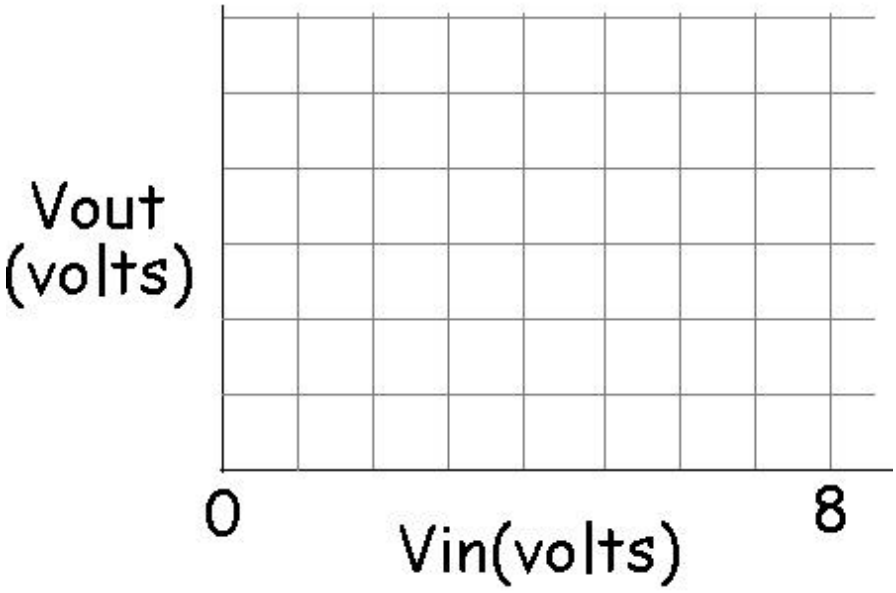


Figure 5a: Transistor as a Switch

a) Redraw Figure 5a with the transistor modeled as switch and a diode. (4 points)

b) Draw the Vout as a function of Vin assuming the transistor behaves as it appears in your model in part (a). (4 points)



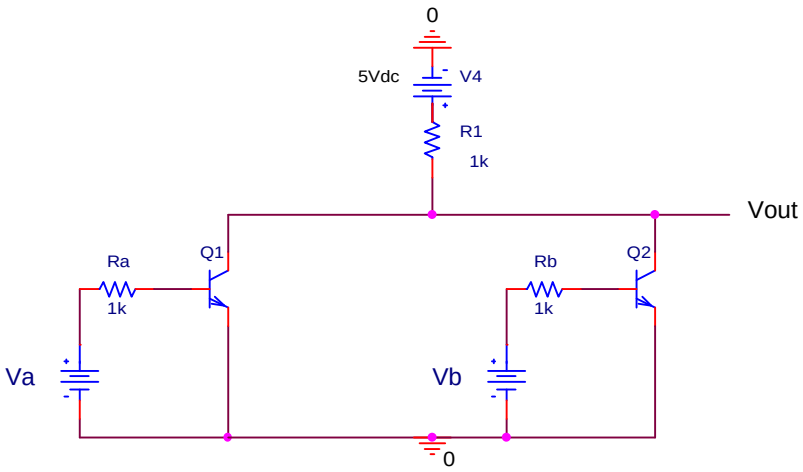


Figure 5b

c) Redraw the circuit in Figure 5b with the transistors modeled as switches and diodes. (6 points)

d) Fill in the following table of Vout as a function of Va and Vb based on the model you gave in part c. (6 points)

Va	Vb	Vout
0V	0V	
0V	5V	
5V	0V	
5V	5V	

e) What kind of gate is this? (5 points)

a. AND
b. NAND
c. OR
d. NOR
e. XOR
f. None of the above