Electronics and Instrumentation

ENGR-4300 Fall 2004 Section _____

Experiment 10: Digital Logic and Transistor Switches

Purpose: In this experiment we address the concepts of digital electronics, which is discussed rather well in Chapter 7 of Gingrich. Before looking at some of the basic building blocks of digital circuitry, we will first consider some of the advantages of this branch of electronics.

Equipment Required:

- HP 34401A Digital Multimeter
- HP 33120A 15 MHz Function / Arbitrary Waveform Generator
- HP E3631A Power Supply
- HP 54603B 2 Channel 60 MHz Oscilloscope
- Protoboard
- Some Resistors
- Logic Chips: 7402, 7404, 7410, 7414, 74107, 74393
- Phototransistor
- Relay

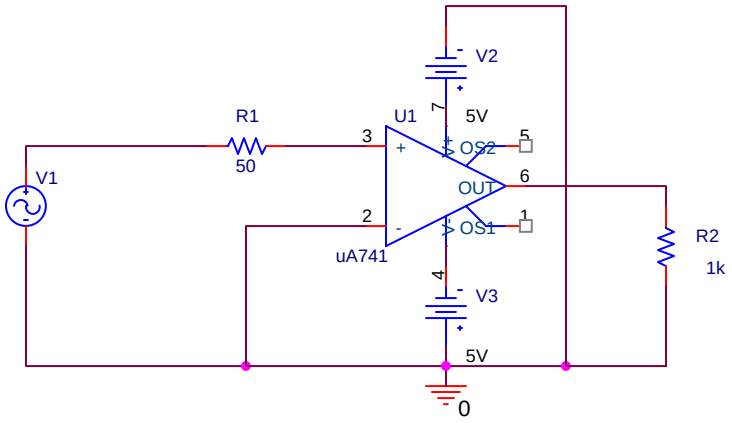
Background

Please skim pg 132-143, 202-209 in Essence, and also the handout packet of Gingrich before proceeding. The key issues to look over in each section are:

- Comparators and Schmitt Triggers
- BJT Transistors acting as a switch
- Number Systems: Decimal vs. Binary. Do not worry about Octal or Hex
- Boolean Algebra: Be sure that you understand the three basic boolean algebraic operations – AND, OR and NOT. You will not have to do a lot of this algebra in this course.
- Logic Gates: You should be able to recognize the symbols for the basic input-output gates along with their corresponding algebraic expressions and truth tables. (Truth tables are important.)
- Combinational Logic: It is possible to perform many different logical functions by combining the basic gates seen in section 7.3. The classic example is the exclusive-OR gate, which follows the logic of the three-way switches we use to control room lights from two different locations. Timing diagrams, another very useful concept, are also discussed.
- The remainder of the chapter can be read as needed.

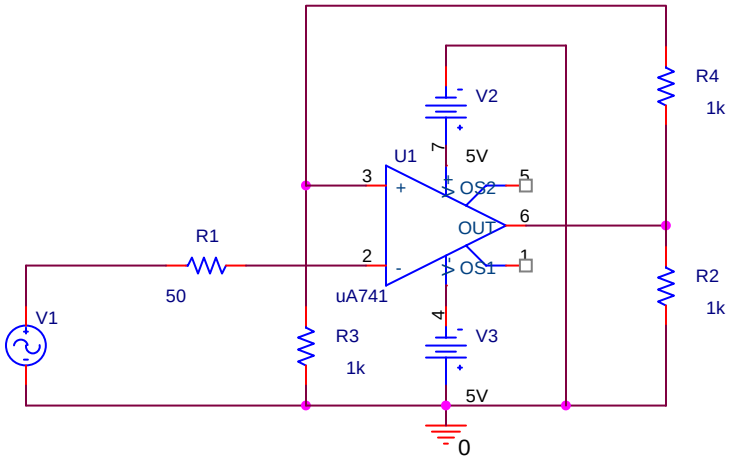
Part A1 Comparators and Schmitt Triggers

In circuit A-1, you will see that we have no feedback for the op amp so this configuration will not obey the rules for op-amps we addressed in a previous experiment. Since the intrinsic gain of the op-amp is very large, any positive voltage across the inputs will cause the output to go as positive as it can and any negative voltage across the inputs will cause the output to go as negative as it can. The range of outputs is limited by V_{CC}. Thus, the output should go to about $+V_{CC}$ whenever the input is positive and to $-V_{CC}$ whenever the input is negative. This is an example of a comparator. The voltage at the positive (+) terminal is compared to the voltage at the negative (-) terminal. When $V^+ > V^-$ then $V_{out} = V_{CC}$ and when $V^+ < V^-$ then $V_{out} = -V_{CC}$. Simulate (transient analysis with a time step of 1us from zero to 3ms) the circuit above to demonstrate that this indeed does happen. You can choose just about any amplitude voltage and see this effect. Once you see the output switch between voltages near $\pm V_{CC}$, print one plot of your output, showing the source voltage V1 and the load voltage (pin 6 of the op-amp). Include this plot in your report.



Circuit A-1

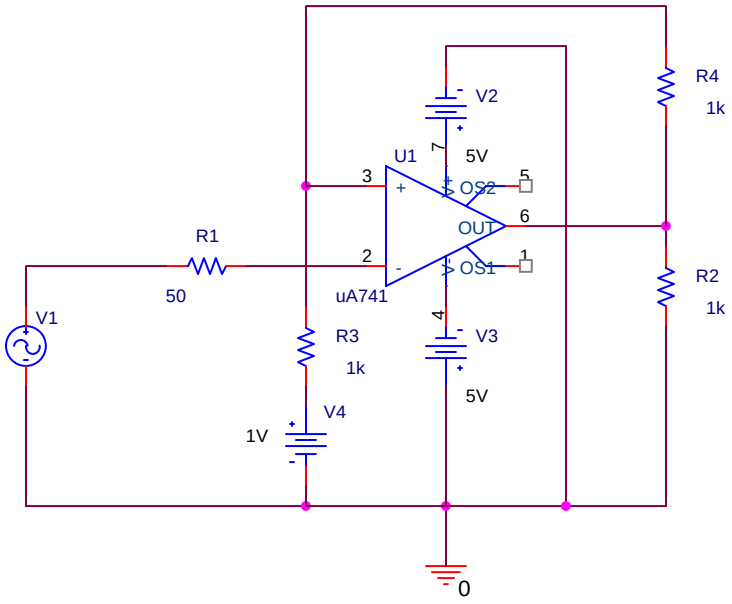
If all we could ever do was to check the sign of a voltage, this kind of logical operation would be of limited usefulness. Also, you should be able to see that a simple comparator circuit is very noise sensitive. If the input signal is approximately zero volts but has a lot of noise on it, the output will keep switching between $+V_{CC}$ and $-V_{CC}$ following the noise. It would be more useful to have a comparator-type circuit that switches output state when the input exceeds some finite threshold rather than just zero. The Schmitt Trigger configuration in circuit A-2 makes this possible. In circuit A-2, the output will switch when the input exceeds BV_{CC} or is less than $-BV_{CC}$ where B = R3/(R3+R4). Show that this is the case. *Hint: the voltage V^+ at the positive input is related to the output voltage V_{out} by the voltage divider action of resistors R3 and R4. R2 is a 1K load resistor. See section 6.5 in Lunn.*



Circuit A-2

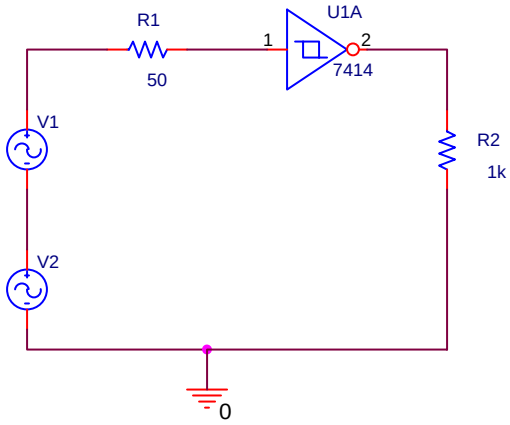
Now simulate this circuit (same transient analysis as above) and show that it indeed changes its output state as it should. Print one plot, again showing the source voltage V1 and the output voltage (pin 6). Be sure that your input level is large enough to make the circuit switch states, but not too large so that it is difficult to observe where the switching occurs. Include this plot in your report.

A Schmitt Trigger can be further generalized as is shown in circuit A-3. Simulate this circuit (same transient analysis as above), print one plot and discuss what it does. Include this plot in your report. Be sure that you use a large enough amplitude for V1 so that the output switches between saturated states, but again not so large that it is difficult to see where the switching occurs.



Circuit A-3

Thus far, we have considered a fairly general model of a Schmitt Trigger. The particular device we will use in our experiments is an SN7414 or equivalent. The 7414 is included with the PSpice program. Circuit A-4 uses this component instead of the model above. In circuit A-4 which we have included two voltage sources to crudely show what happens when noise is added to a signal.



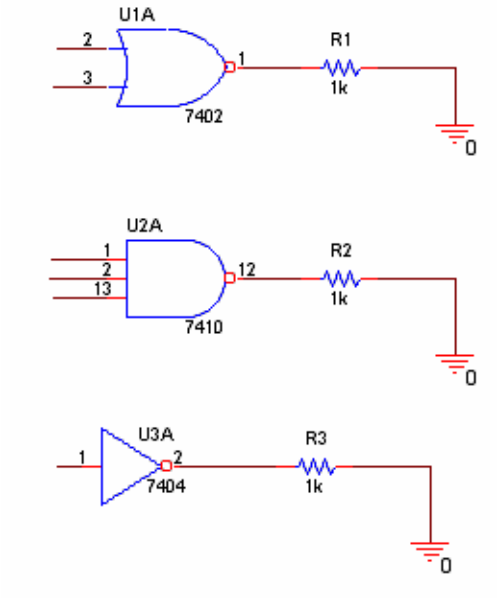
Circuit A-4

Simulate circuit A-4. For V1, use an offset of 1.5V, an amplitude of 1.5V and a frequency of 1k. For V2, use no offset, an amplitude of 0.2V and a frequency of 100k. Again do a transient analysis and produce only one plot. Include this plot in your report. You might want to expand the time scale around one of the transition points to verify that the output changes state only once. Check to be sure that the device performs as it should by looking up the characteristics of the SN7414 on the Texas Instruments website. There is a link to the pdf file for this device on the links page. What are the typical switching thresholds for this device and does the PSpice simulation work as expected?

Part A2 Basic Logic Gates

Binary logic has two values, called TRUE and FALSE or LOGIC 1 and LOGIC 0 or ON and OFF or HIGH and LOW. The corresponding binary number can have two possible values, 1 and 0. In TTL digital electronic circuits, the corresponding definition in terms of voltages is about 5 volts for LOGIC 1 and about 0 volts for LOGIC 0. About 5 volts usually means any voltage between 3 and 5 volts while about 0 volts means any voltage in the range 0 to 2 volts. The two output levels of the Schmitt Trigger you just simulated are examples of practical values for LOGIC 1 and LOGIC 0. (Aside: The output levels from TTL devices will be in the ranges indicated. These are the only output levels one should see with logical devices. This is one characteristic that makes them differ from analog devices. They also switch very fast from one state to the other. Switching speeds are usually much faster than for analog devices, especially cheap devices like the 741 op amp.)

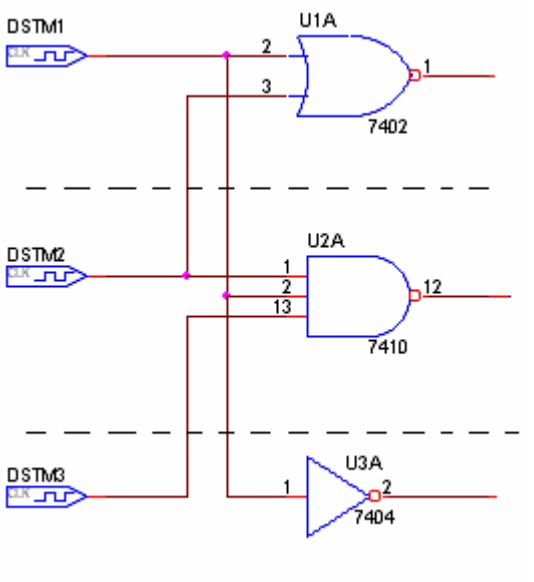
We will now consider three basic logical elements: a two input NOR gate, a three input NAND gate and an INVERTER. By convention, the upper right pin on a digital chip is always connected to HIGH (+5 volts) and the bottom left pin to LOW (0 volts). On a 14 pin chip this corresponds to pin 7 (0V) and pin 14 (5V) and on a 16 pin chip, pin 8 (0V) and pin 16 (5V). These two connections provide reference values for the operations the chips perform. Generally circuit diagrams do not show these two reference connections. If you forget to connect these two pins, your circuit will not function correctly. Wire the circuits below on your protoboard.



Circuit A-5

To test the circuits, you need to consider all combinations of possible inputs to each gate. The NOT gate has only one input. Therefore, we need only consider HIGH (5 volts) and LOW (0 volts). First connect pin 1 to +5 volts and record the output voltage at pin 2. Then, connect pin 1 to 0 volts and record the output at pin 2. Does the gate invert the input? Take a picture of one of the input/output trace combinations. Draw a truth table for this gate on the output plot. Now you will repeat this process for the other two gates. The NOR gate has two inputs, so we must consider the output at pin 1 for all possible combinations of binary inputs at pins 2 and 3: (LOW,LOW), (LOW, HIGH), (HIGH,LOW) and (HIGH, HIGH). Print a sample input and output trace. (Note: You will only be able to show one input on the 'scope.) Record the truth table on the plot. The NAND gate has three inputs. How many combinations of HIGH and LOW are required to fully test this gate? Record the input and output for this gate in a truth table on a sample output plot, as well.

Now the simulation. Wiring the circuit in PSpice is somewhat different that on the protoboard. In the first place, PSpice asumes that the +5 volt and 0 volt references have already been wired, so you do not need to make these connections. Also, in PSpice, we cannot simply move the wires to record all possibilities. Therefore, we use digital clocks with different pulse lengths to create the signals we need to test the gates. The final difference is that we have removed the resistors connecting the gate outputs to ground. This tells PSpice to output timing diagrams by default. Timing diagrams are easier to read when you need to compare many binary signals. Unlike a regular PSpice plot (where all signals are displayed with the same voltage and time axis) a timing diagram displays the signals on separate lines with the same time scale. Wire the circuit below in PSpice:

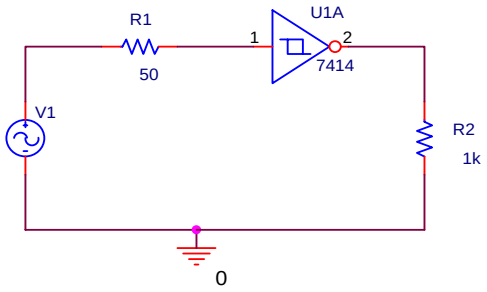


Circuit A-6

Now we need to set the clocks up to work with different pulse lengths. Use the default settings for DSTM1 (no delay, on time = 0.5us, off time = 0.5us). For DSTM2, double the on and off times to 1us. For DSTM3, double them again to 2us. Simulate for 8us with a step size of 0.01us. Display all the inputs from the clocks and the output of each of the three gates. Produce a hardcopy of the timing diagram with the inputs and the outputs for all three gates. Mark the output trace for each gate on the diagram. For each gate, generate the truth table for the device based on the outputs and inputs you observe on the timing diagram. Write them on the output plot. Do your results agree with the truth tables in Gingrich on page 136 and your results from the circuits you built?

Part A3 Application of a Schmitt Trigger

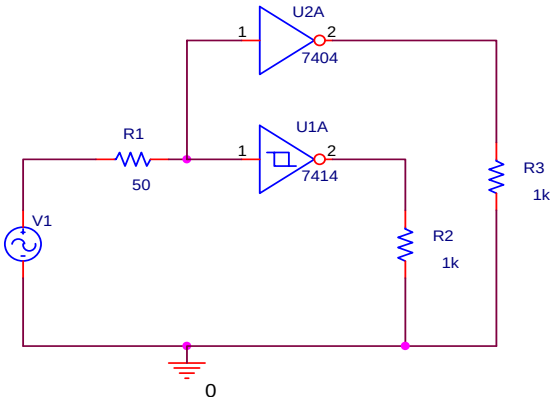
As we saw in Part A1, the purpose of the SCHMITT TRIGGER is to convert an analog voltage into a binary digital voltage. When the input voltage of the SN7414 exceeds a threshold of 1.7volts, the device output switches to LOGIC 0; the input voltage must drop below 0.9volt for the output to switch back to LOGIC 1. The difference in thresholds (called hysteresis) is very important in preventing false triggering on noise. The device is also inverting, but the SCHMITT TRIGGER does not behave in the same manner as the INVERTER.



Circuit A-7

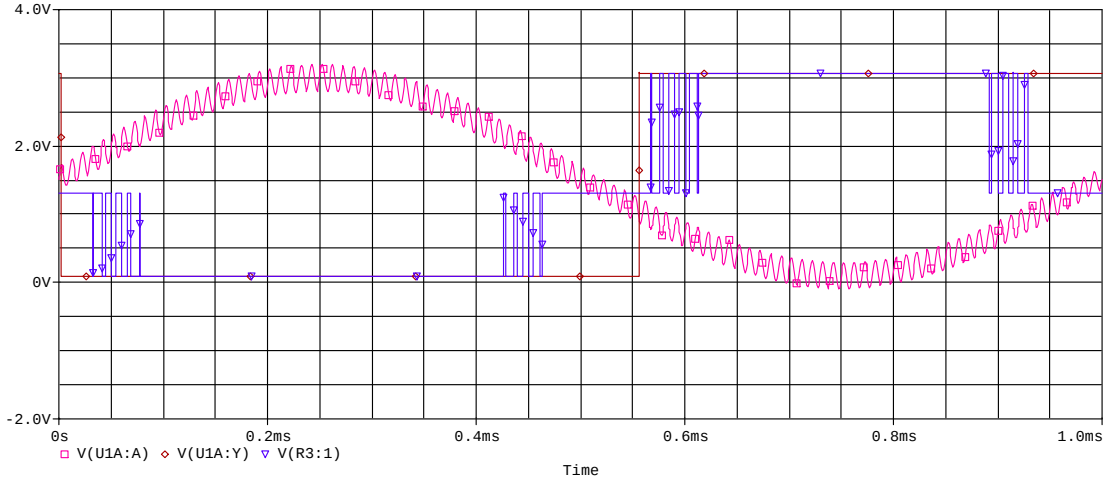
Set up the circuit shown on the protoboard. Remember that the 50ohm resistor is the internal resistance of the function generator. Set the function generator for sine wave output with a frequency of 1kHz and an amplitude of 5 volts. Be sure you have both the input and output connected to the scope. Print out the scope trace. On the plot, indicate the features of the signals that demonstrate hysteresis. Include this plot with your report.

In circuit A-7, we will add an inverter to circuit A-6 in order to examine the difference between a Schmitt trigger and an inverter.



Circuit A-8

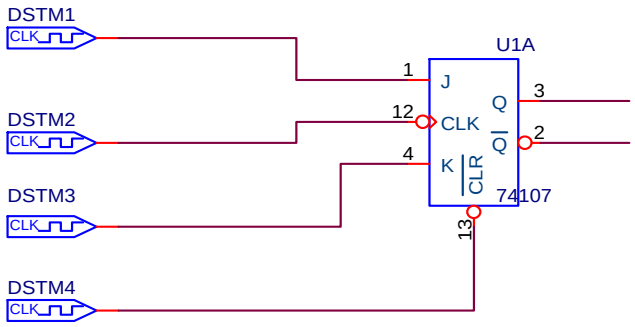
Again, use Agilent software to show what the input and output signals look like. Include this plot in your report. For reference purposes, the output of a PSpice simulation using two sources to show noise effects is shown below.



The PSpice simulation has some problems analyzing this sort of circuit since it mixes analog and digital devices and some digital devices (inverters, for example) have ranges of operating voltages where they are typically confused. Can you see what the problem is? For what range of input voltages does the inverter have trouble? What behavior does your circuit have at these input voltages?

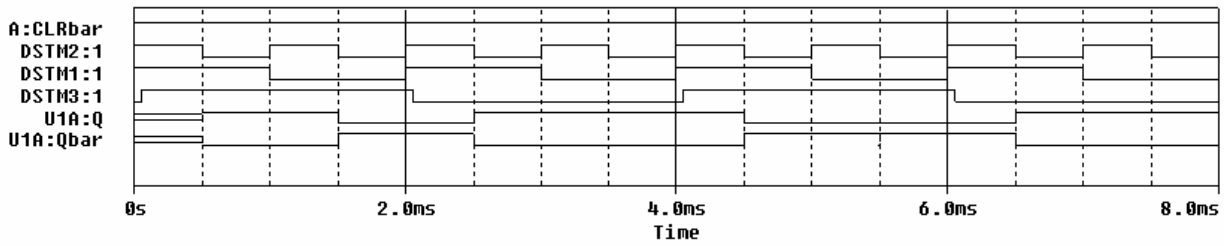
Part B1 Flip Flops

It is possible using basic logic gates to build a circuit that remembers its present condition. Please read through sections 7.9-7.11 of Gingrich with particular emphasis on the JK FLIP FLOP, which we will be using here. You should also look over the datasheet for 74107 JK FLIP FLOP listed on the links page. DO NOT create the circuit below in PSpice.



Circuit B-1

JK FLIP FLOPS, like other FLIP FLOPS have four inputs, two outputs and the usual two power connections (V_{CC} and ground). The outputs are labeled Q and $\overline{Q}$ (also called Qbar and NQ), which are complements of one another. Thus, when Q is LOW, Qbar is HIGH, etc. The input $\overline{CLR}$ (DSTM4), when LOW will reset the outputs to a known state. Since this device has memory, it is very important to be able to first initialize it to a known state. Otherwise, we will not know what it is doing. CLK is the digital clock. A flip flop only changes its output when the clock pulse at CLK goes from HIGH (5V) to LOW (0V). This is called the "falling edge" of the clock. To decide how to set the output, the flip flop "looks" at the values at the inputs at J and K AND at the current value of the output. Based on these three values, it decides how to reset the output. Look at the timing diagram on the next page. DSTM2 is the clock. When the clock falls, look at the values of the inputs at J (DSTM1) and K (DSTM3). Also consider the output value (U1A:Q). How does the output change based on these three inputs? Generate a truth table for the flip flop. Please check the datasheet for the SN74107 FLIP FLOP or section 7.10.3 of Gingrich to see what the truth table for this device should do.



Set up the 74107 JK FLIP FLOP on the protoboard. Use the function generator for the clock (DSTM2). Set it for a square wave frequency of 1kHz. *Use the offset feature to shift the square wave up such that it cycles between 0V and 5V.* Be sure that you use the 'scope to check the operation of the function generator. Use the ground (0V) and +5V connections on your protoboard to supply the required logic levels for the J, K, and CLR. *First set the CLR to zero to be sure that the FLIP FLOP begins in a known*

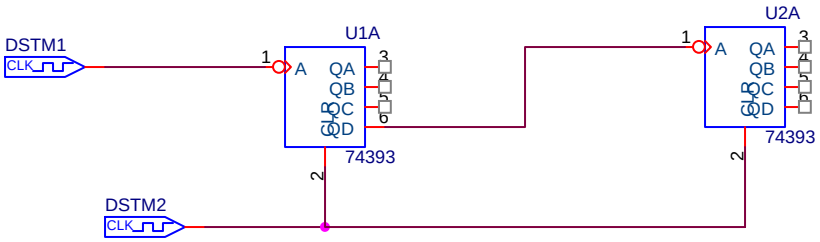
state. Then set it to +5V to check out the four possible combinations of J and K. Connect J and K manually in the same manner as you did for the logic gates. Observe the output Q on channel 2 of your scope and the clock on channel 1. Construct an experimental truth table for this device. Print a single trace, as in the previous part, draw the truth table for the flip flop on it, indicate which combination of inputs and initial state it represents, and demonstrate that the output is correct.

Part B2 Counters

JK FLIP FLOPS can be connected in a counter configuration as shown in figure 7.29 of the Gigrich notes. However, it is not necessary for us to configure several FLIP FLOPS to create a counting circuit, because this is already done in many kinds of chips. The SN74393, for example, has two sets of four JK FLIP FLOPS connected as binary counters. Binary counting is based on powers of 2 and is described in Gingrich section 7.1.1 Here is a table showing the binary numbers from 0 to 16.

Decimal	Binary	Hex	Octal	Decimal	Binary	Hex	Octal
00	00000	00	00	08	01000	08	10
01	00001	01	01	09	01001	09	11
02	00010	02	02	10	01010	0A	12
03	00011	03	03	11	01011	0B	13
04	00100	04	04	12	01100	0C	14
05	00101	05	05	13	01101	0D	15
06	00110	06	06	14	01110	0E	16
07	00111	07	07	15	01111	0F	17
				16	10000	10	20

Simulate the following circuit in PSpice:



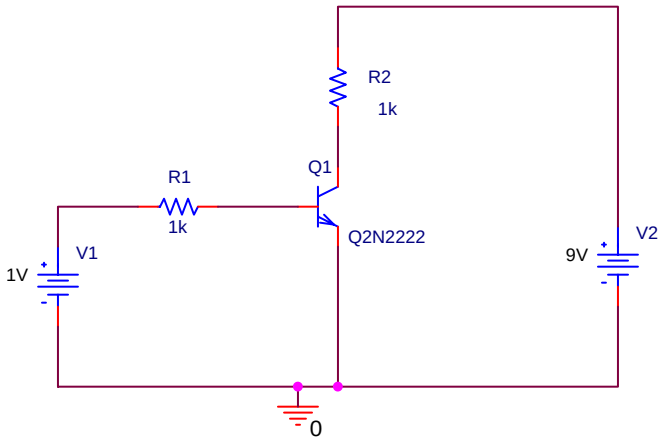
Circuit B-2

For this simulation, DSTM1 is a normal clock with OFFTIME = ONTIME= 0.5us. DSTM2 is set up so that it first clears the counters, lets them count, and then clears them again. (OFFTIME=25us, ONTIME=2us) *If the PSPice models for counters or flip flops are not cleared initially, they will not give any data.* By connecting the two counters together as shown, the sequence of numbers 2QD, 2QC, 2QB, 2QA, 1QD, 1QC, 1QB, 1QA (IN THAT ORDER) form the binary number. Since the counter is set up to count clock pulses, it will count up from 0 (at reset) to the number of pulses sequentially. Generate the output for this circuit for time 0 to 30us using 1us increments. You should display the reset pulse, the input clock at pin 1 of U1A, and all eight of the counter outputs (QA,QB,QC,QD for both counters). Using the timing diagram, verify that the counters are actually counting. You can use the cursor to easily get your binary number. What is the highest number it counts to before it resets? At what time does it reset? Express this number both as a binary number and a decimal number. Write it on the timing diagram for this circuit. How many pulses will the clock have to cycle through between the time it is reset and when it hits its maximum value of 11111111?

Part C1 Transistor Switches

Take a look at the transistor as a switch in Essence (section 8.8). We do not need to consider most of the rest of the chapter on transistors because the operational amplifier is a better device for us to build amplifiers with.

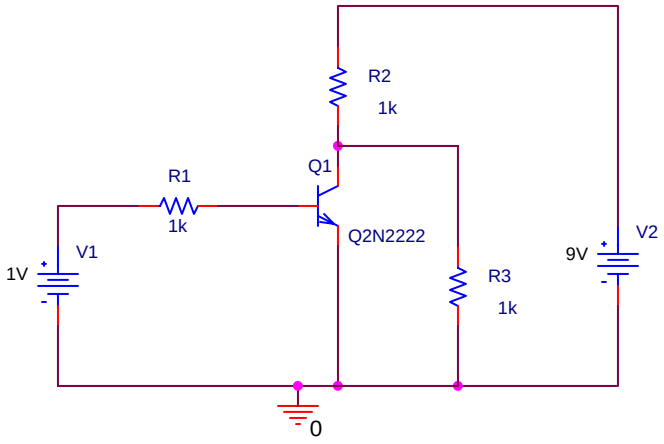
Using PSpice, set up the circuit shown below. For analysis, set up a DC SWEEP for V1 from 0.2 to 9 volts (step = 0.005V). The transistor Q1 is acting as a switch in the loop with resistor R2 and voltage V2. The voltage V1 and resistor R1 are used to turn the switch ON or OFF. Print this plot.



Circuit C-1

The transistor switch will not work exactly like an ideal, simple switch. However, it can be a good approximation to such a switch and, more importantly, it will switch states based on an applied voltage rather than a mechanical act (like turning a switch on and off). From your plot of the voltages in the transistor circuit, determine the range of voltages V1 for which the switch will be OFF and the range of voltages V1 for which the switch will be ON. Indicate this on your plot and include it with your report.

Now we will consider this switch in a configuration that you ordinarily might not think about, but does a good job of switching the voltage across a load. Add the resistor R3 shown below to your circuit.



Circuit C-2

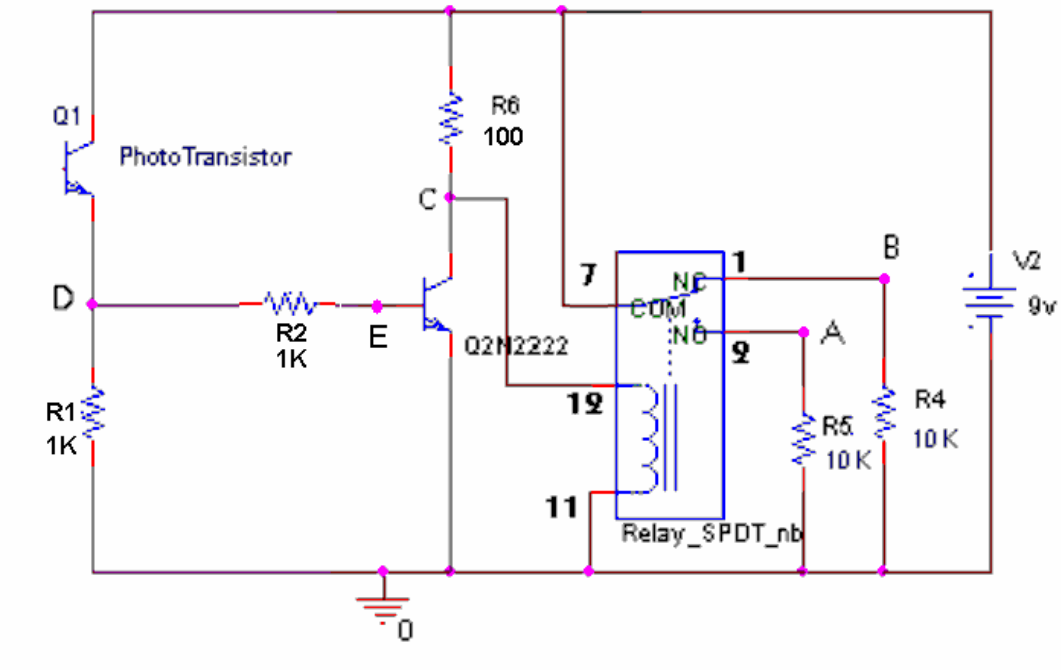
The transistor switch, when open, allows the maximum voltage to occur across R3. When the switch is closed, the voltage across R3 goes near zero. Run your simulation again and print your output this time. Again determine the range of voltages V1 for which the switch is ON and OFF. What is a typical voltage across R3 when the switch is OFF? What is a typical voltage across R3 when the switch is ON? From what you know about the desired range of digital circuits, do you think that these values make sense?

Now we want to take a look at the range of V1 for which the switch is neither ON nor OFF. Replot your PROBE result for V1 from 0.5V to 1V. Now, rather than plotting voltages, plot the collector, base and emitter currents for Q1, each normalized by the current through resistor R1. (Actually, plot the negative of the emitter current so that all three current ratios are positive.) Just for reference purposes, label the collector C, emitter E, and base B on the two circuit diagrams above. You should be able to identify a small range of voltages V1 for which the magnitude of the collector and emitter currents are more that 170 times the base current. Use the cursors to find this range. Print out the plot with the cursors and indicate on the plot where this ratio is 170 or better. Include this plot with your report. This is the range of V1 for which the transistor circuit acts like a very good amplifier. Here it has a current gain of much more than 100. The gain is not a simple constant, nor is it as large as we can obtain with an op-amp.

By looking at the operation of a simple transistor circuit, we have seen that there is a set of input voltages for which is looks like a switch that is OFF, an amplifier, and a switch that is ON.

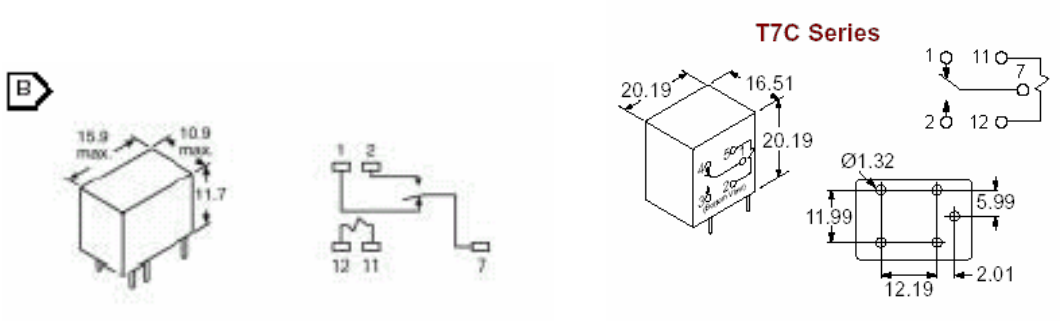
Part C2 Optically Triggered Relay

A relay is a switch that is controlled by an inductor coil. When no current is flowing through the inductor between the pins connected to the coil, the switch remains in the closed (NC) position, as shown in circuit C-3. However, when current flows through the inductor, it forces the switch to open (NO). To see how practical transistor switches can be, we will build a circuit that uses a phototransistor (and light) to switch a relay on and off. We cannot use the very small voltages created by the phototransistor directly to control the relay, but we can use the phototransistor to generate just enough voltage to cause the 2N2222 transistor to switch on and off. When the transistor switch is open, point C is not attached to ground directly and current flows through the inductor in the relay, and when the switch is closed, point C is connected directly to ground and no current flows through the inductor in the relay.



Circuit C-3

Here are the pinouts for two sample relays. Yours may be different than the ones shown here. Check the pdf file for your chip on the links page.



After you have wired the circuit, ask your TA for a test light. You can connect this light directly to the power supply at 11V to generate enough light to power the phototransistor. The relay switch should switch one way when you move the light over the phototransistor and switch the other when you take it away. If you cannot hear it click, try reversing the polarity of your phototransistor. Warning: Do not leave the light on the phototransistor for long periods of time because the 100 ohm resistor will get very hot. Measure the voltage at points A, B, C, D and E when the light is on and off. Record your results in the following table:

	A	B	C	D	E
on					
off					

Report and Conclusions

The following should be included in your written report. Everything should be clearly labeled and easy to find. Partial credit will be deducted for poor labeling or unclear presentation.

Part A

Include the following plots:
1) PSpice transient for circuit A-1 (0.5 pt)
2) PSpice transient for circuit A-2 (0.5 pt)
3) PSpice transient for circuit A-3 (0.5 pt)
4) PSpice transient for circuit A-4 (0.5 pt)
5) Agilent plot of circuit A-5 single trace from NOR gate with truth table (0.5 pt)
6) Agilent plot of circuit A-5 single trace from NAND gate with truth table (0.5 pt)
7) Agilent plot of circuit A-5 single trace from NOT gate with truth table (0.5 pt)
8) PSpice timing diagram for the three gates in circuit A-6 with output traces marked (1.5 pt)
9) Agilent plot of circuit A-7 with hysteresis marked. (1 pt)
10) Agilent plot of circuit A-8. (1 pt)

Answer the following questions:
1) What are the switching thresholds for the 7414? (1 pt)
2) What are the actual voltage values you observed as HIGH and LOW states in the hardware realization of the circuit A-5? (1 pt)
3) What is the difference between the Schmitt Trigger output and the inverter output? In what voltage range does the inverter act poorly? Why? (1 pt)
4) Why do you think the Schmitt trigger is preferable to an inverter in the presence of noise? (1 pt)

Part B

Include the following plots:
1) Agilent plot of single trace from flip flop with truth table, etc. (1 pt)
2) PSpice timing diagram of counters (1 pt)

Answer the following questions:
1) Flip flops are called memory devices. Why do you think this is true? (1 pt)
2) For the counter circuit configuration just studied, what is the highest number it counts to in the time shown on your output? Express as both a binary and decimal number. (1 pt)
3) How many pulses will the clock have to cycle through after it resets before the counter hits its maximum value? (1 pt)

Part C

Include the following plots:
1) PSpice sweep for circuit C-1 with range indicated. (0.5 pt)
2) PSpice sweep for circuit C-2 with range indicated. (0.5 pt)

Answer the following questions:
1) In part C1, what is a typical voltage across R3 when the switch is OFF? when the switch is ON? (1 pt)
2) Why do you think that the values in question 1) make sense? (1 pt)
3) Draw a simplified circuit diagram for part C1 that includes just V2, R2 and a simple switch to represent the transistor. (1 pt)
4) For your simplified circuit, when the switch is open (OFF), how much voltage will be across it? When the switch is closed (ON), how much voltage will be across it? (1 pt)
5) In part C2, what were the voltages at points A, B, C, and D when the light was on? when it was off? (1 pt)
6) Explain how the circuit in part C2 works in terms of the voltages at the four points and the function of the components in the circuit. (1 pt)

Summarize key points (1 pt)

Mistakes and problems (0.5 pt)

Member responsibilities (0.5 pt)