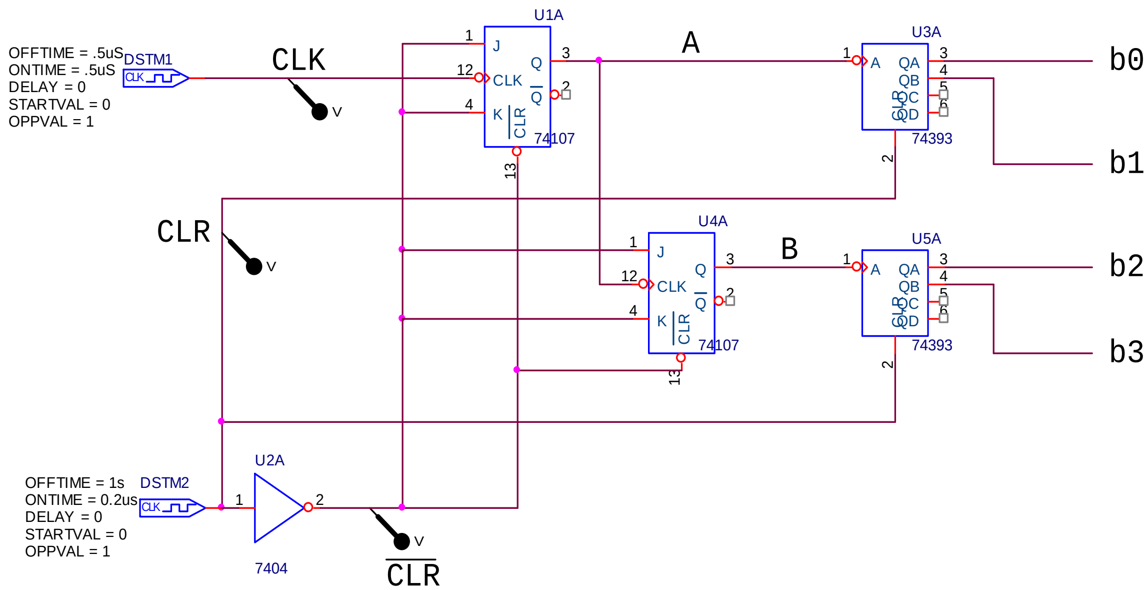
Questions about Flip Flops and Counters

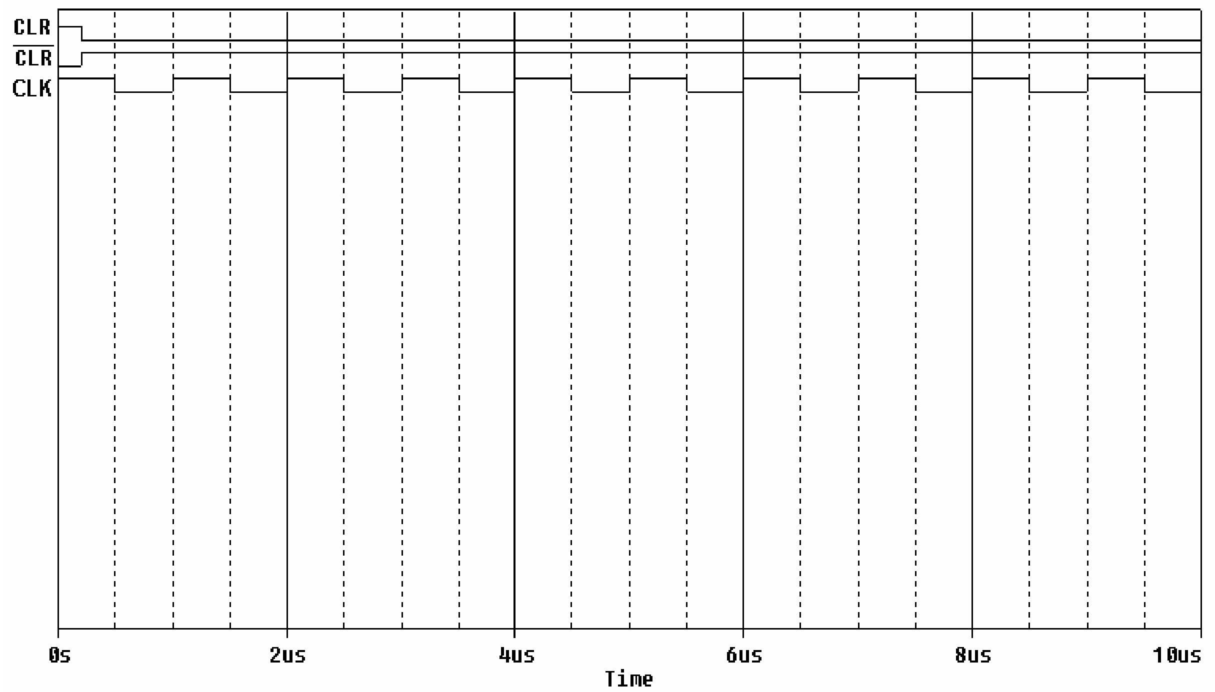
Fall 2004

Question 1: Flip Flops and Counters *(20 points)*



a) In the above circuit, the CLR signal resets the counters at t=0.2us and the ~(CLR) resets the flip flops at t=0.2us. The input clock to the first flip flop (UA1) is the CLK signal. These signals are shown below. Draw a trace for the signals at point A and point B. Also draw a trace for the output signals: b0, b1, b2 and b3. Note that the flip flops and the counters all trigger on the falling edge of their input clocks.

(2 points per trace=12 points)


CLR
CLR
CLK
0s
2us
4us
6us
8us
10us
Time

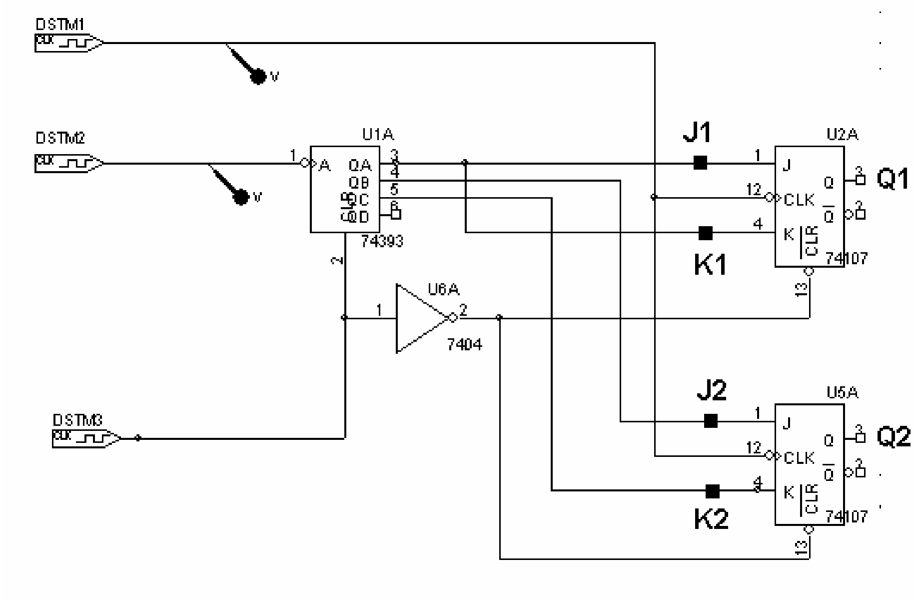
b) The output of the above circuit forms a binary number with b0 as the lowest order bit: (b3 b2 b1 b0). At time t=9us, what binary number will you see at the output? What is this in digital? *(2 points)*

c) Two of the bits in the binary output are always identical. Which bits are these and why are they always the same? *(4 points)*

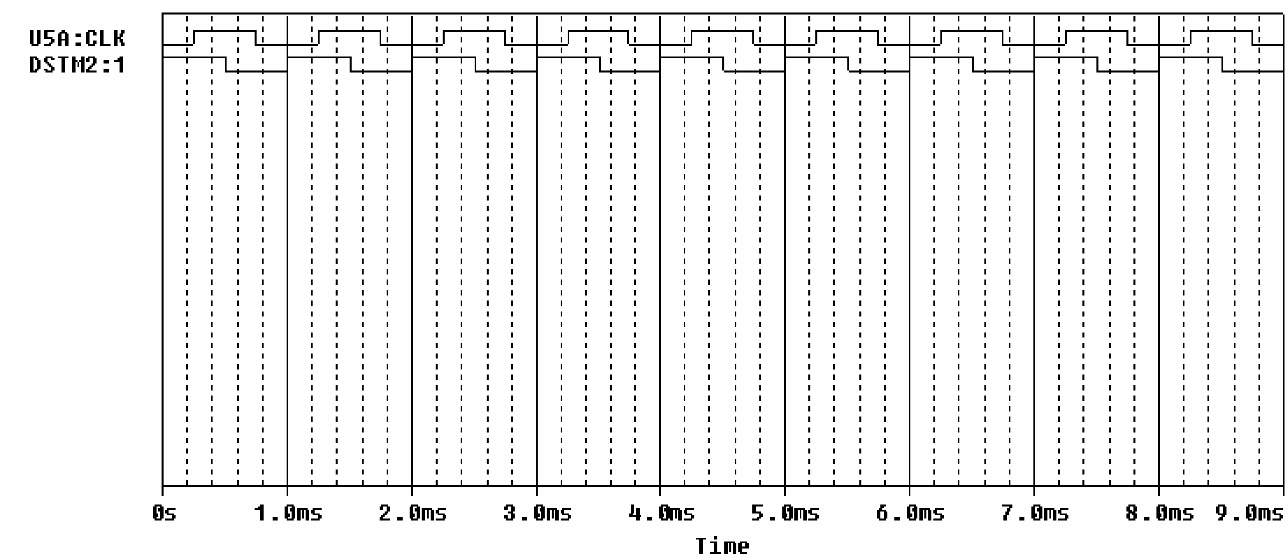
d) Does the output (b3 b2 b1 b0) correspond to a correct count of the input clock pulses at CLK? Why or why not? *(2 points)*

Fall 2004 Solution
(not available)

Spring 2004
Question 1 -- Flip Flops and Counters (20 points)



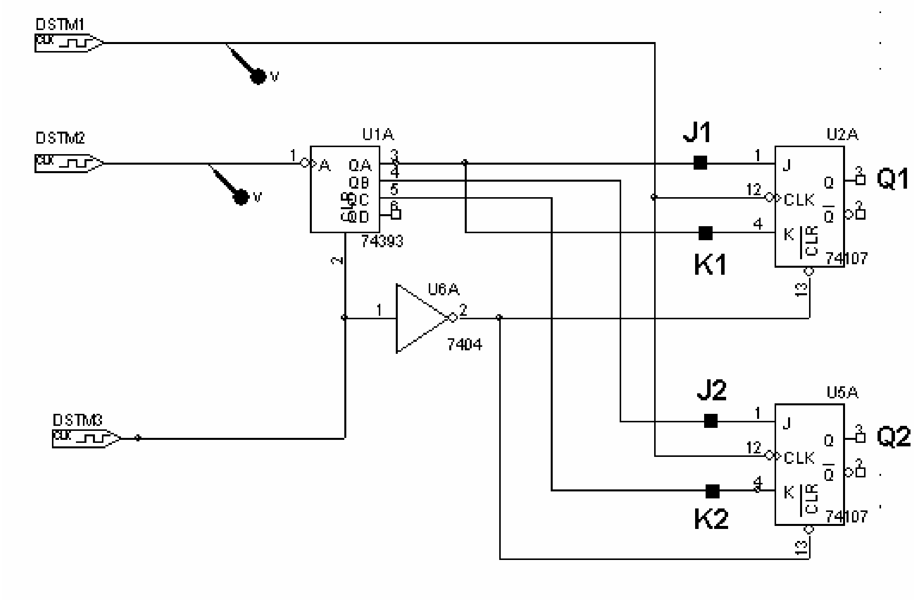
a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (flip flop clock), the second trace shown is DSTM2 (counter clock), and DSTM3 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0 and that all three devices change on the falling edge of the clock.. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2)
(3 points each = 18 points)



b) To what value does the counter count in the time frame indicated? *(2 points)*

Spring 2004 solution

Question 1 -- Flip Flops and Counters (20 points)



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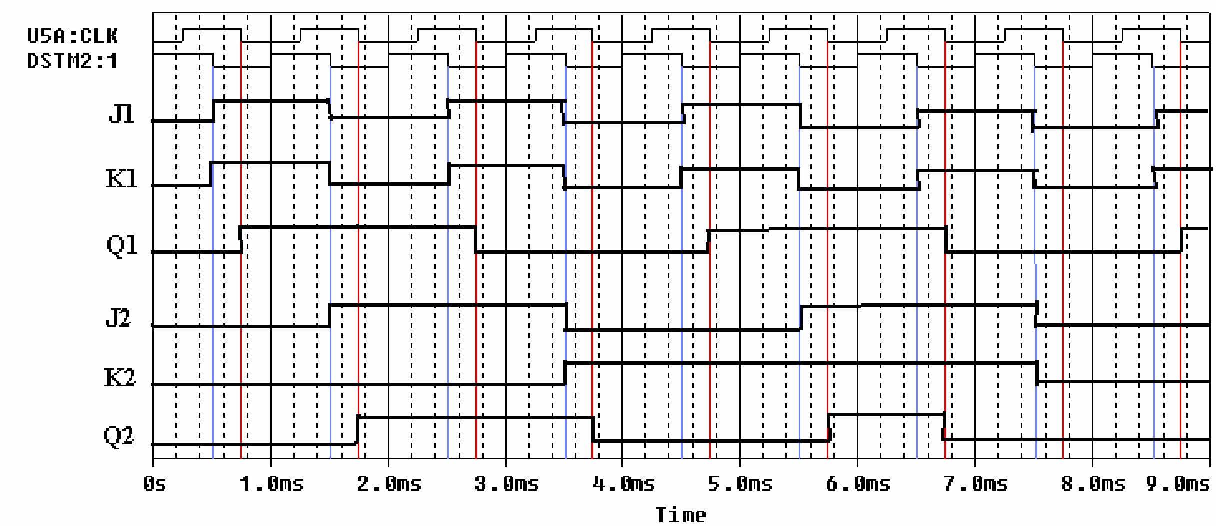
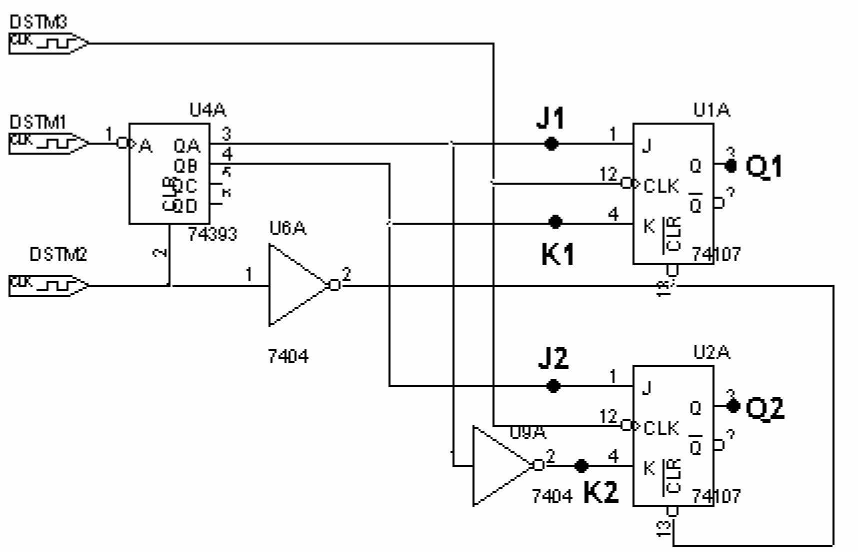


c) To what value does the counter count in the time frame indicated? *(2 points)*

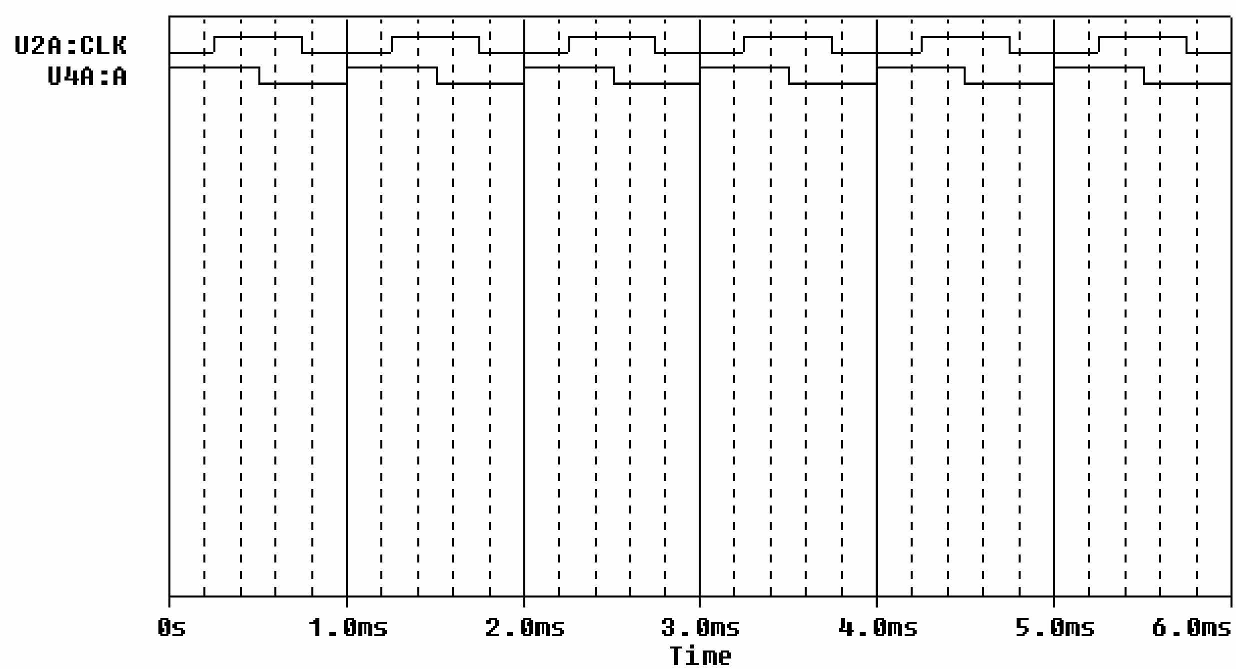
1001 = ***9***

Fall 2003

Question 1 -- Flip Flops and Counters (20 points)

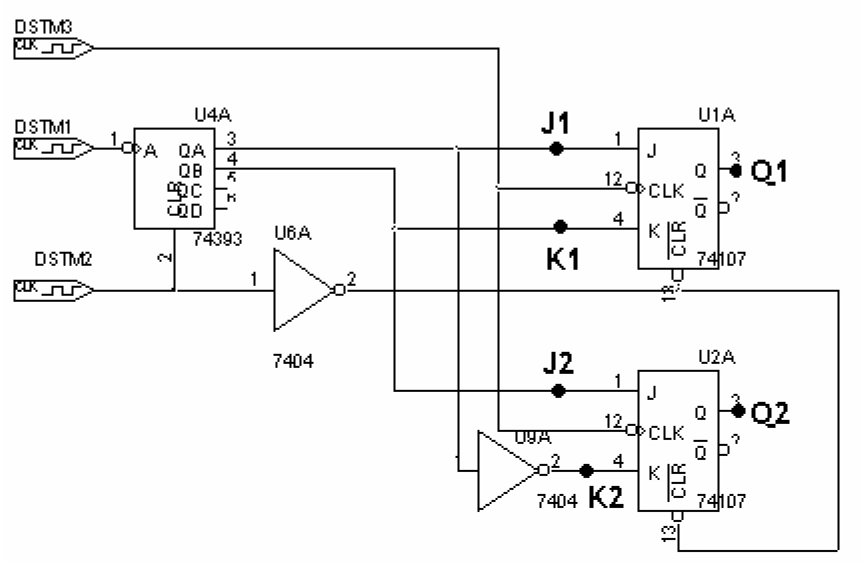


a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (counter clock), the second trace shown is DSTM3 (flip flop clock), and DSTM2 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2) *(3 points each = 18 points)*

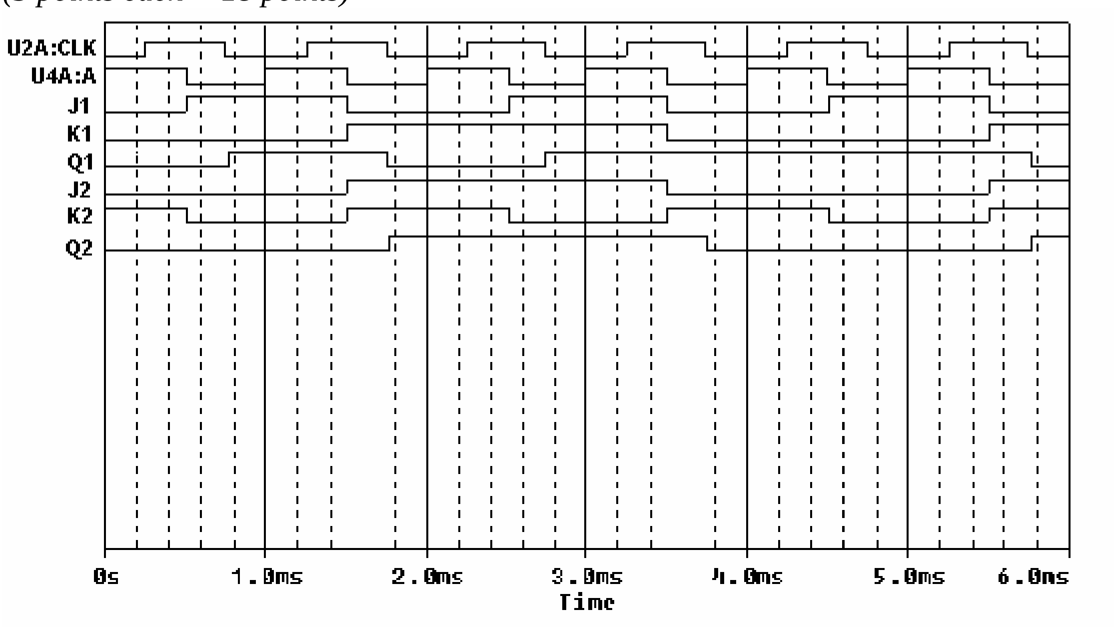


d) To what value does the counter count in the time frame indicated? *(2 points)*

Fall 2003 Solution
Question 1 -- Flip Flops and Counters (20 points)



a) Complete the timing diagram for the circuit above. Note that the first trace shown is DSTM1 (counter clock), the second trace shown is DSTM3 (flip flop clock), and DSTM2 provides an initial reset pulse to both of the devices. You can assume that all outputs are initially 0. Draw traces for all six of the points indicated: (J1, K1, Q1, J2, K2, Q2) *(3 points each = 18 points)*

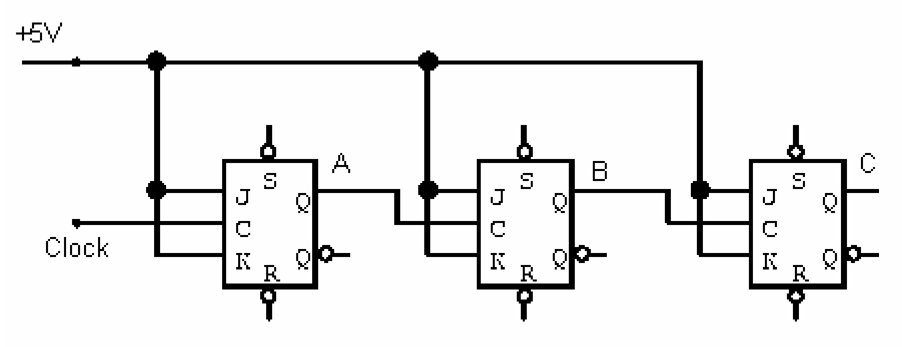


e) To what value does the counter count in the time frame indicated? *(2 points)*

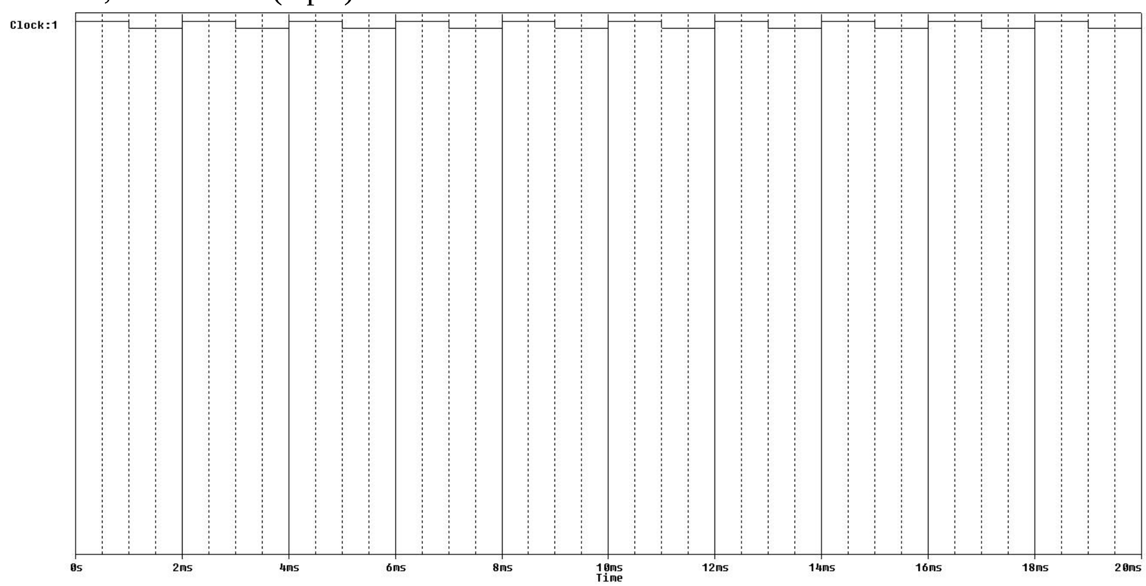
110 (binary) = ***6*** *(decimal)*
(The highest order bit is not pictured.)

Spring 2003

Question 2) Flip-Flops and Counters (20 pts)

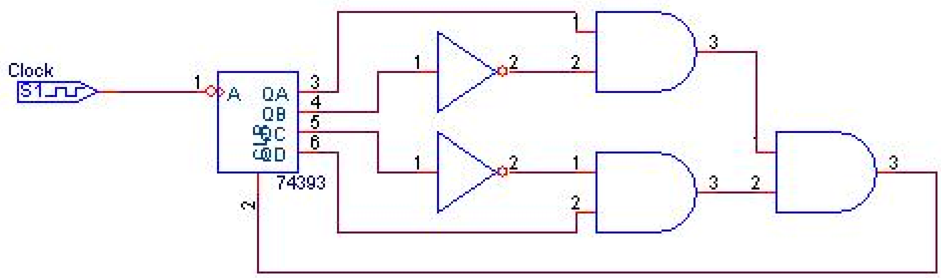


a) i. In the circuit above, draw the waveforms for points A, B and C. Assume that at time t=0, A=B=C=0. (6 pts)



ii. Based on your plots in the previous section, show that this circuit is a 3 bit counter. (2 pts) Explain which bit is the least significant bit and which is the most significant bit. (2 pts)

b) i. In the circuit below find the CLR signal (pin 2) as a Boolean function of QA, QB, QC and QD. (4 pts)



ii. Write down the complete counting cycle of the counter (in decimal), in the above formation. Show that the counter resets after the counting cycle has finished. (3 pts)

iii. How would you configure the circuit to have the cycle (0-1-2-3-…-7-0)? Draw the circuit diagram. (3pts)

Spring 2003 solution
(not available)

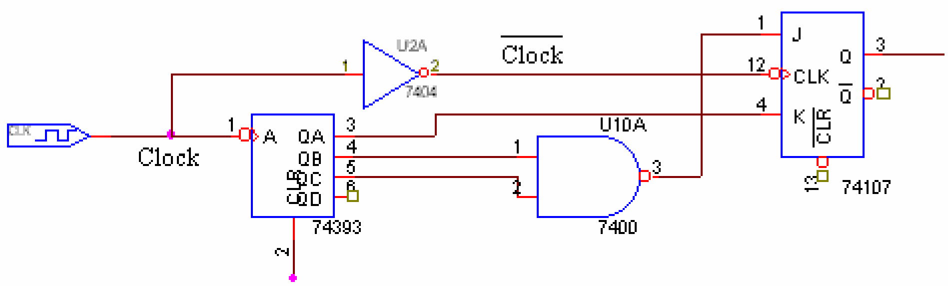
Fall 2002

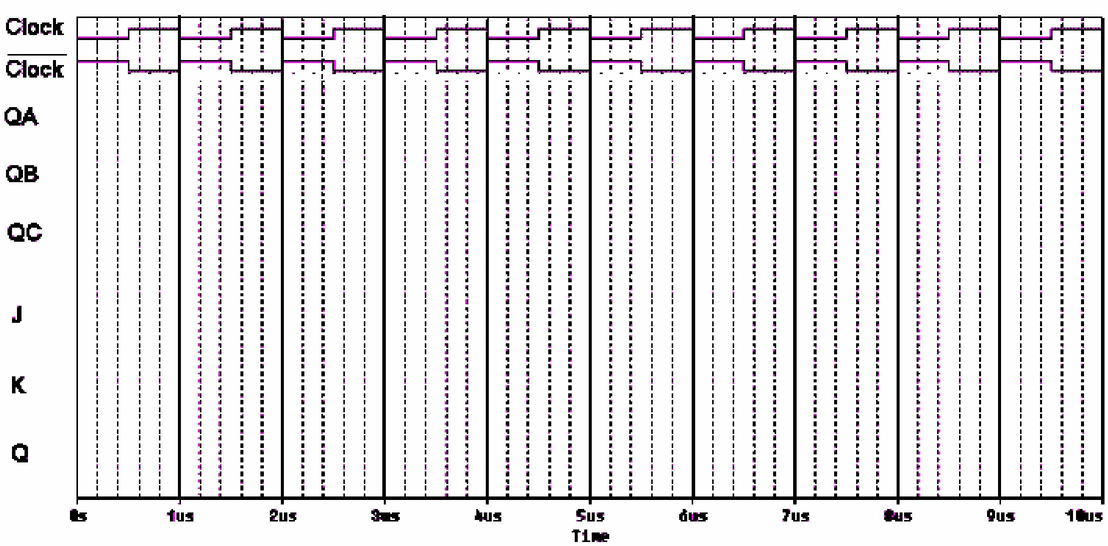
Question 1) Flip Flops and Counters (15 points)

a) Fill in the truth table for a JK flip flop. Use Q_0 or $\overline{Q}_0$ to denote the previous value of Q and $\overline{Q}$. (6 pts)

J	K	CLK	Q	$\overline{Q}$
		↓		
		↓		
		↓		
		↓		

b) In Figure 1a we show a counter connected to the inputs of a JK flip flop. Draw the output versus time at each of the points specified in the diagram below. Assume that initially both the counter and the JK flip flop are cleared (i.e., at time 0: QA=0, QB=0, QC=0, QD=0, Q_0=0, and $\overline{Q}_0$ =1) . Note that since both the counter and the flip flop trigger on the falling edge of the clock, we have added an inverter to one of them to prevent race conditions. (9 pts)



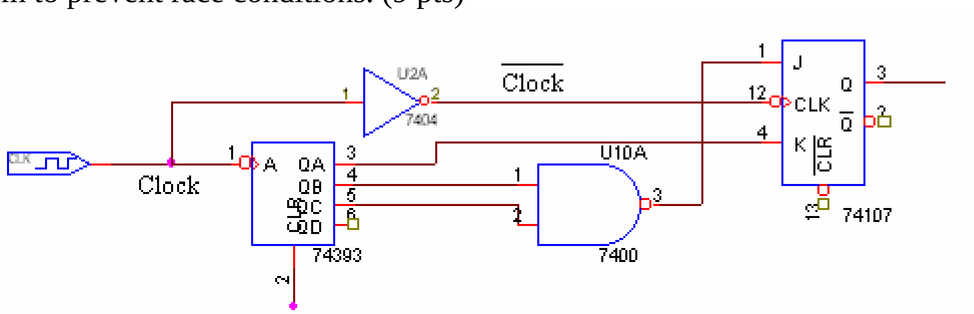


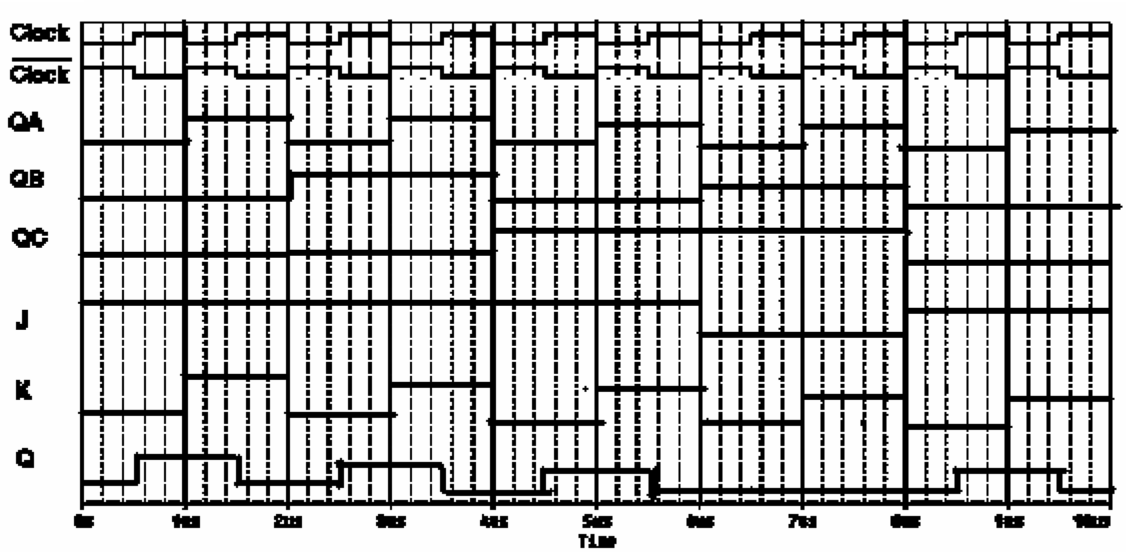
Fall 2002 Solution
Question 1) Flip Flops and Counters (15 points)

c) Fill in the truth table for a JK flip flop. Use Q_0 or $\overline{Q}_0$ to denote the previous value of Q and $\overline{Q}$. (6 pts)

J	K	CLK	Q	$\overline{Q}$
0	***0***	↓	***Q***	$\overline{Q}$
0	***1***	↓	***0***	***1***
1	***0***	↓	***1***	***0***
1	***1***	↓	$\overline{Q}$	***Q***

d) In Figure 1a we show a counter connected to the inputs of a JK flip flop. Draw the output versus time at each of the points specified in the diagram below. Assume that initially both the counter and the JK flip flop are cleared (i.e., at time 0: QA=0, QB=0, QC=0, QD=0, Q_0=0, and $\overline{Q}_0$=1) . Note that since both the counter and the flip flop trigger on the falling edge of the clock, we have added an inverter to one of them to prevent race conditions. (9 pts)

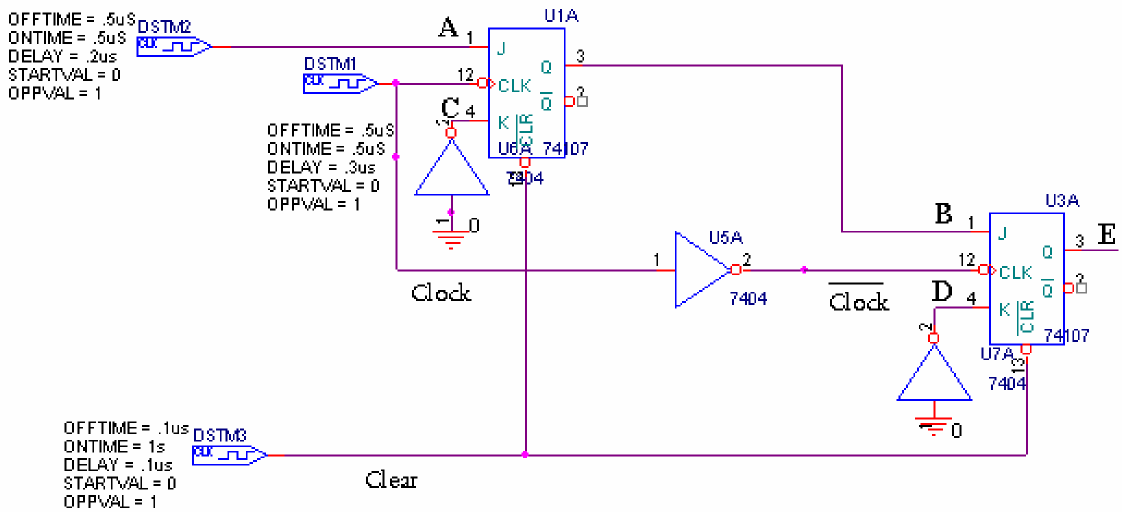




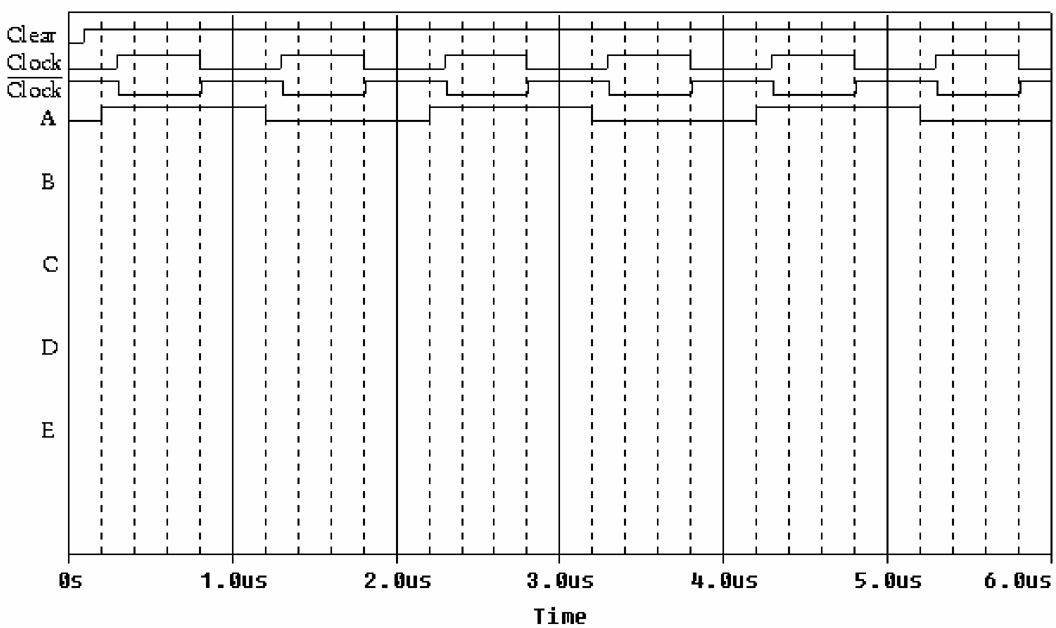
Spring 2002

Sample Question: Flip Flops and Counters

The following is a diagram of a circuit from PSpice. The “Clear” signal initializes the flip flop. Therefore, once it goes high, the flip flop outputs Q=0 and $\overline{Q}$ =1. The clock for the first flip flop is DSTM1 and the clock for the second flip flop is DSTM1 *inverted.* Remember that flip flops and counters trigger on the falling edge of the clock pulse.



a) The following figure shows the clear signal, the clocks and the input at A. Draw the traces at B, C, D and E.

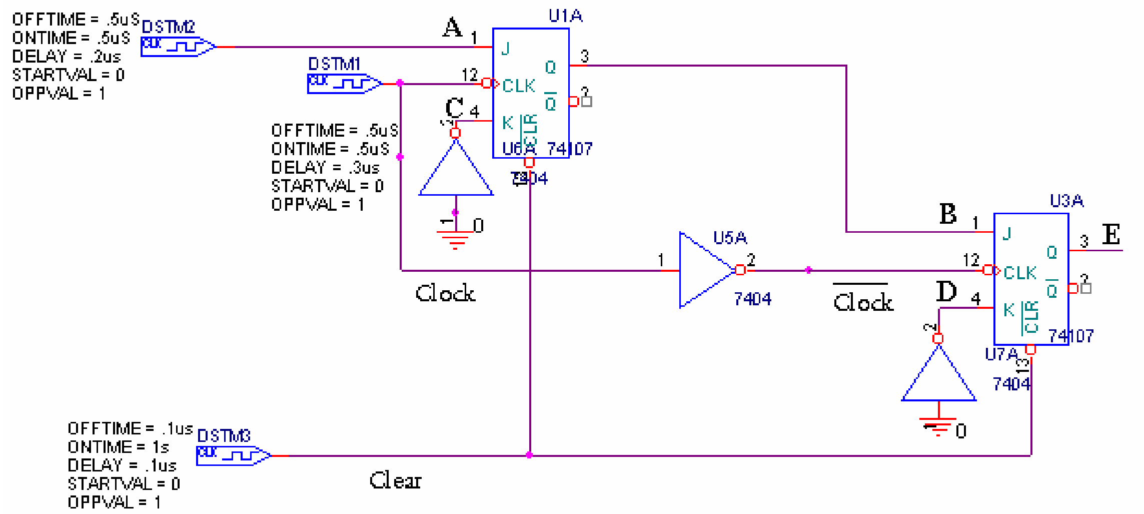


b) If the clock for a counter (74393) was attached to signal A, what would the output look like after 3.0us. (Assume the counter has also been cleared, therefore QA=0V, QB=0V, QC=0V, QD=0V at time 0s). Express your answer in volts.

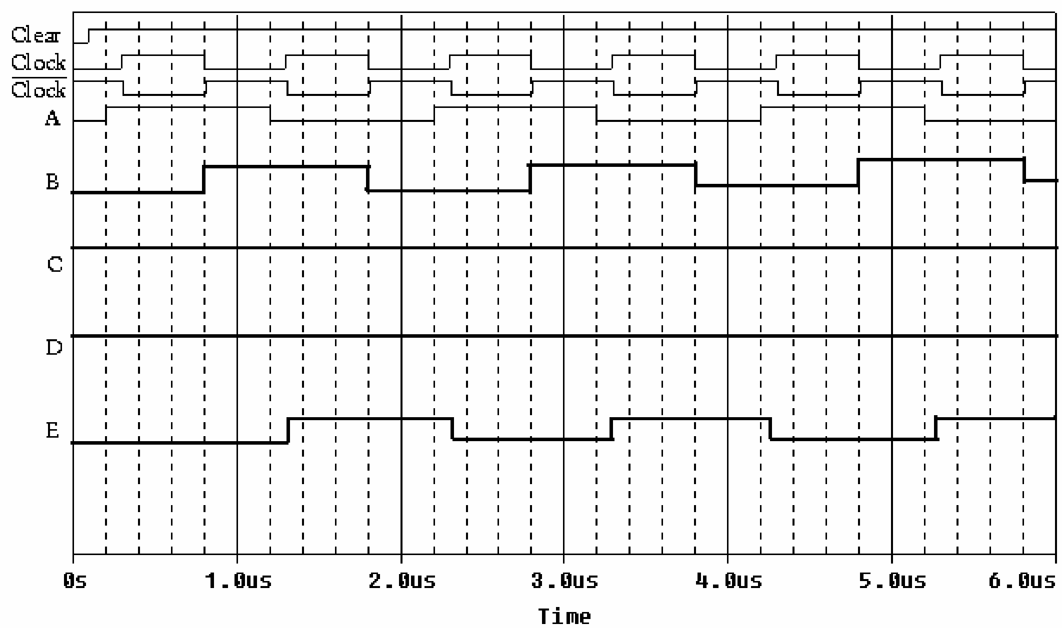
QA = QB = QC = QD =

Spring 2002 solution
Sample Question: Flip Flops and Counters ****** ANSWER ******

The following is a diagram of a circuit from PSpice. The "Clear" signal initializes the flip flop. Therefore, once it goes high, the flip flop outputs Q=0 and $\overline{Q}$ =1. The clock for the first flip flop is DSTM1 and the clock for the second flip flop is DSTM1 *inverted.* Remember that flip flops and counters trigger on the falling edge of the clock pulse.



a) The following figure shows the clear signal, the clocks and the input at A. Draw the traces at B, C, D and E.



[Some explanation: C and D are inverted from ground. This means they are always high. Note that the flip flops only change on the falling edges of the clock. The first flip flop will look at J and K when Clock goes down at 0.8 us. Since at that time A(=J) is high and C(=K) is high, the flip flop toggles and B goes high. The next time that Clock goes high to low at 1.8us, A is low and C is still high. This time, the flip flop should be equal

to J(A) and B goes low again. This sequence continues for B. The signal at E changes on the falling edge of Clockbar(the inverted clock signal). Its inputs are J=B and K=5V. At 0.3us, B is low, so E stays low. At 1.3us, B is high, so E toggles to high. At 2.3us, B is low, so E goes low again. The sequence continues.]

b) If the clock for a counter (74393) was attached to signal B, what would the output look like after 6.0us. (Assume the counter has also been cleared, therefore QA=0V, QB=0V, QC=0V, QD=0V at time 0s). Express your answer in volts.

QA =   *5V*   QB =   *5V*   QC =   *0V*   QD = *0V*

[Some explanation: The counter "counts" on the falling edge of the clock. Since B has three pulses since 0s, the counter should count up to three. In binary, that is 0011. Note that QA is the lowest order bit.]