Lecture 6. 555 Timer

Problem – Create a repeating signal without using a function generator.

Specifics – Create a square wave with a specific frequency, amplitude, and duty cycle.

Frequency – The number of cycles per second of a signal.

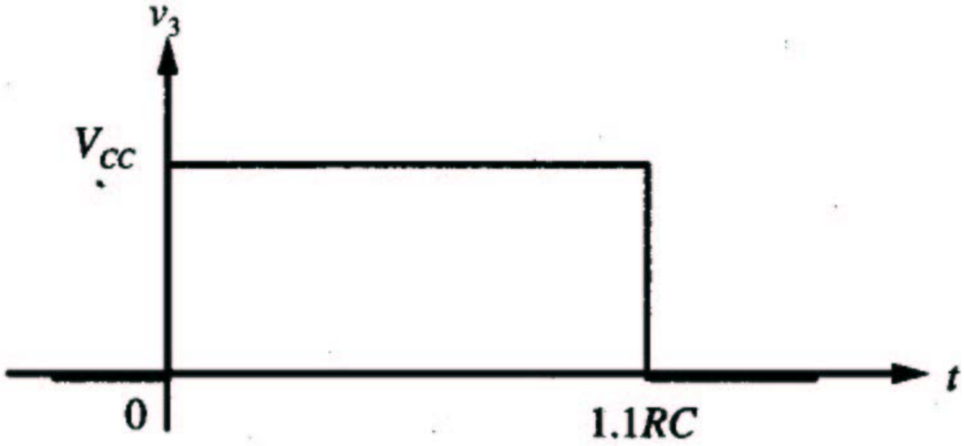
Amplitude – The height of a signal. Using a scope usually measured from the bottom of one peak to the top of another, $V_{PEAK\ TO\ PEAK}$, V_{P-P}.

Duty Cycle – The ratio of how long a signal is low compared to the period.

SOLUTION – Use a 555 timer.

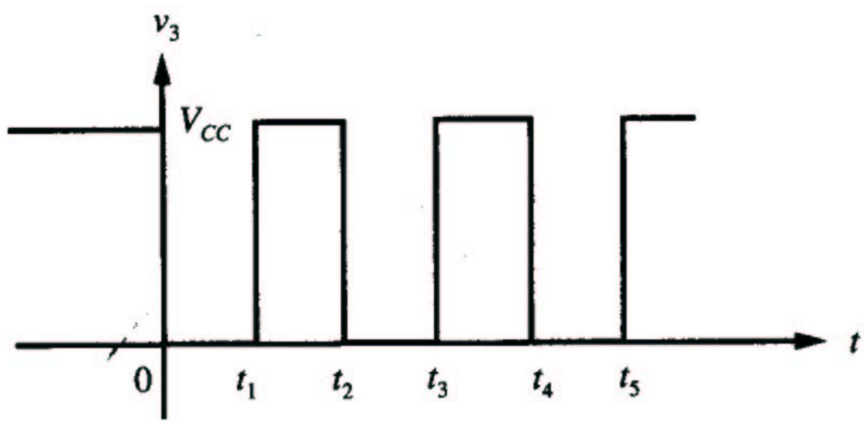
The 555 timer comes in a variety of number designations. The most common are NE555 and LM555. There are two modes of operation, monostable and astable. In monostable mode a single pulse with a fixed pulse width is created by means of connecting an external resistor and capacitor to the appropriate pins. The output pulse occurs after a trigger signal is sent to the timer. If different pulse widths are required the easiest way to implement this is to replace the resistor with a potentiometer. Adjust the potentiometer for the new pulse width setting and then trigger the timer. In astable mode, some times called free running, multiple pulses are produced using two external resistors and one external capacitor. The waveform has a fixed period and duty cycle. Selecting different values of resistors and the capacitor can change the period and duty cycle. No trigger signal is required for pulses to be generated in astable mode.

MONOSTABLE WAVEFORM

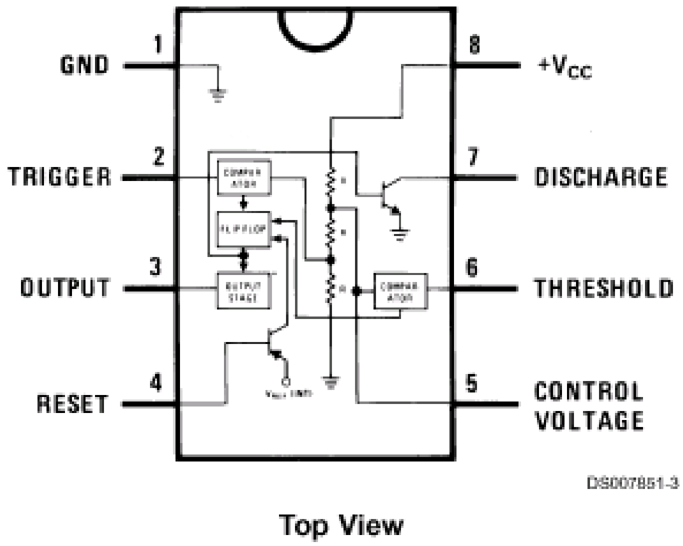


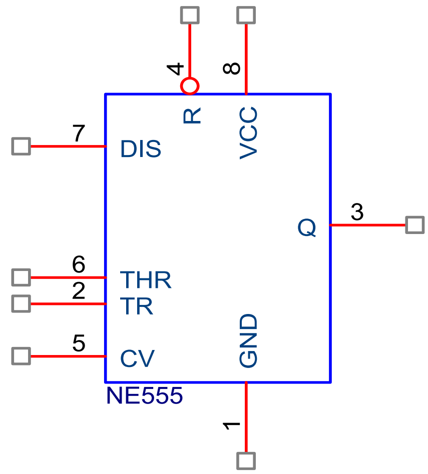
(b)

ASTABLE WAVEFORM



PIN LAYOUT

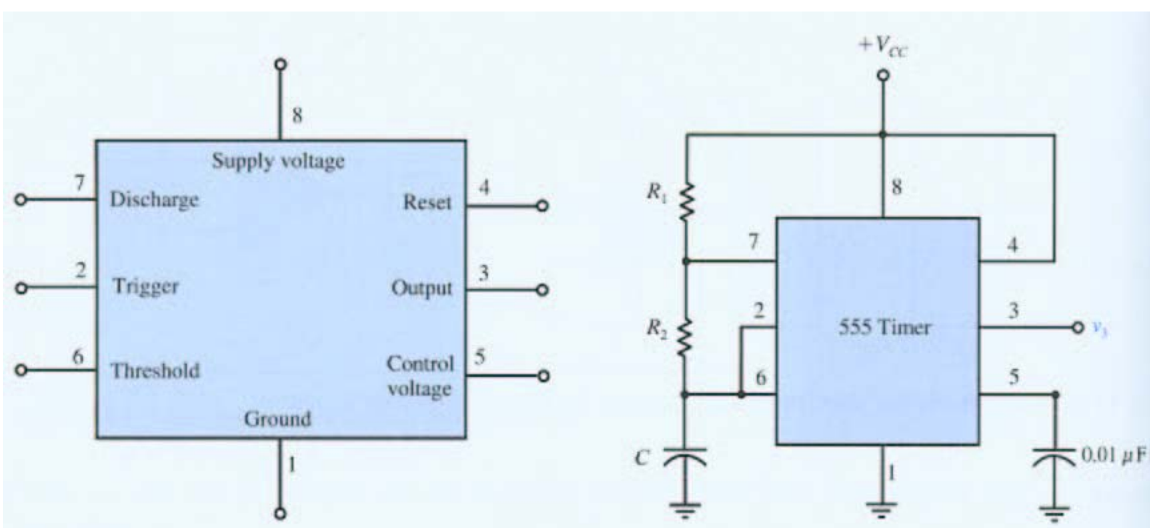




PIN DESCRIPTION

Pin 1 - ground
Pin 2 - trigger input signal, starts waveform
Pin 3 - output signal
Pin 4 - reset terminal, forces output to zero volts
Pin 5 - control voltage
Pin 6 - threshold, resets output waveform to zero volts
Pin 7 - discharge, discharges capacitor charge to zero volts
Pin 8 - power

ASTABLE OPERATION



Internally the 555 timer consists of two comparators, resistors, transistors, and a digital circuit called a flip-flop (which you will study later in the course). Connecting the external resistors and capacitors as shown above results in the timer operating in the following fashion. When an applied voltage at pin 6, the threshold voltage, is > 2/3(V_{CC}), the output at pin 3, v_3, is low, that is pin 3 is at zero volts. At the same time an internally connected switch transistor that is connected between the discharge, pin 7, and ground, pin 1, is turned ON. With the discharge transistor reducing the voltage at pin 6 towards zero volts, the voltage at pin 2, the threshold voltage, is also being reduced. When the voltage at the threshold, pin 2, $\leq$ 2/3(V_{CC}) then the output goes high, $v_3 = V_{CC}$ and the discharge transistor is turned OFF.

When the reset voltage, pin 4 is low, the discharge transistor is turned ON. To disable the reset function connect pin 4 to V_{CC}.

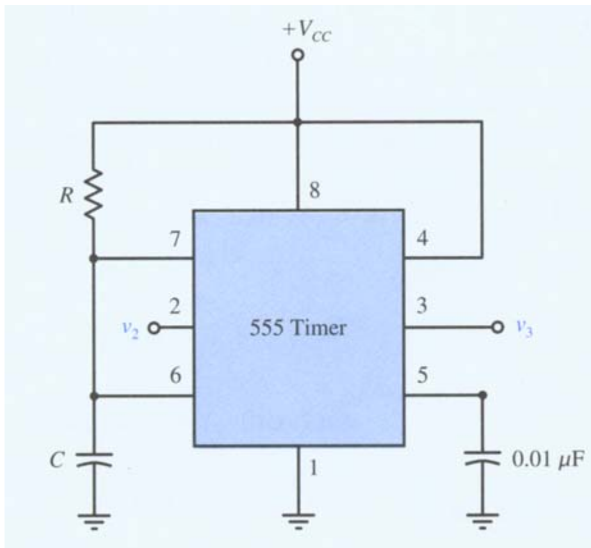
Let us assume that when the timer is properly wired and initially powered, the capacitor C is initially uncharged. That means the voltage at pins 2 and 6 is <2/3(V_{CC}) and the discharge transistor is turned OFF. Consequently the output voltage at pin 3, v_3, equals V_{CC}. The capacitor then begins to charge through the R_1 and R_2 resistors and the capacitor. When the capacitor charges to a voltage level such that the voltage at pin 6, the threshold voltage, equals 2/3(V_{CC}), the discharge transistor turns ON and the output goes to zero volts. When the capacitor discharges so that $v_2 = v_6 = 1/3(V_{CC})$, the output equals V_{CC} and the discharge transistor is OFF. The process keeps repeating until the power is turned off.

To summarize:

$v_2 = 1/3(V_{CC})$, $v_3 = V_{CC}$

$v_6 = 2/3(V_{CC})$, $v_3 = 0$ volts

<u>MONOSTABLE OPERATION</u>



In the diagram above, pin 2, labeled v_2, is the input trigger signal and pin 3, labeled v_3, is the output signal. In its normal state of operation the signal at pin 2 is held to the power supply voltage, V_{CC}. The output at pin 3 is zero volts. When the signal at pin 2 is momentarily connected to ground, the voltage at pin 2 will become zero volts. As the voltage at pin 2 decreases and becomes $< 2/3(V_{CC})$, the output at pin 3 goes high to the V_{CC} value. When pin 3 equals V_{CC} the internal discharge transistor turns off. The capacitor C begins to charge with a time constant of λ=RC. As the capacitor is charging the voltage at pin 6, the threshold voltage, is increasing. When the voltage at pin 6 is $>2/3(V_{CC})$, the output goes to zero because the discharge transistor turns on and discharges the capacitor. For the output to go low after a trigger pulse, the trigger signal must return to the high, V_{CC} state. Otherwise the output will not reset to zero volts.

To summarize:

$v_2 < 1/3(V_{CC})$, $v_3 = V_{CC}$

$v_6 > 2/3(V_{CC})$, $v_3 = 0$ volts

GENERATING WAVEFORMS

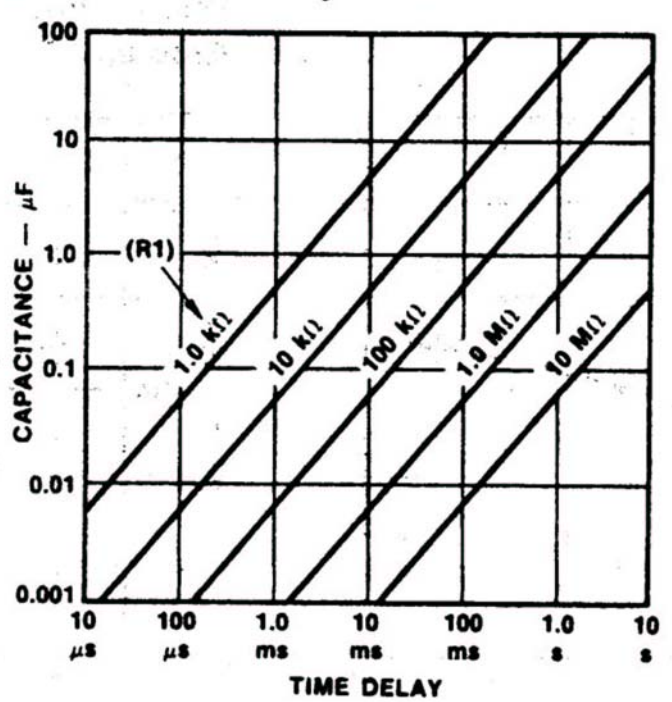
MONOSTABLE

To determine the value of the resistor and capacitor needed to produce a pulse with the correct pulse width, the following equation may be used.

$$t \approx 1.1(RC)$$

An easier method is to use the nomograph below once the pulse width is known to select the proper values.

Figure 3 Time Delay vs R1 and C1



MONOSTABLE NOMOGRAPH

It is important to note that in order to not draw too much current through the timer the resistor value should be large and the capacitor should be low.

ASTABLE

The following information refers to the resistors as R_A and R_B while the above schematic uses R_1 and R_2. For this discussion $R_A = R_1$ and $R_B = R_2$.

To figure out the values for R_A, R_B, and C you can use the chart below or the following equations:

The charge time (output high) is given by:

$$t1 = 0.693 (R_A + R_B)C$$

And the discharge time (output low) by:

$$t2 = 0.693 (R_B)C$$

Thus the total period is:

$$T = t1 + t2 = 0.693 (R_A + 2R_B)C$$

The frequency of the waveform is given by:

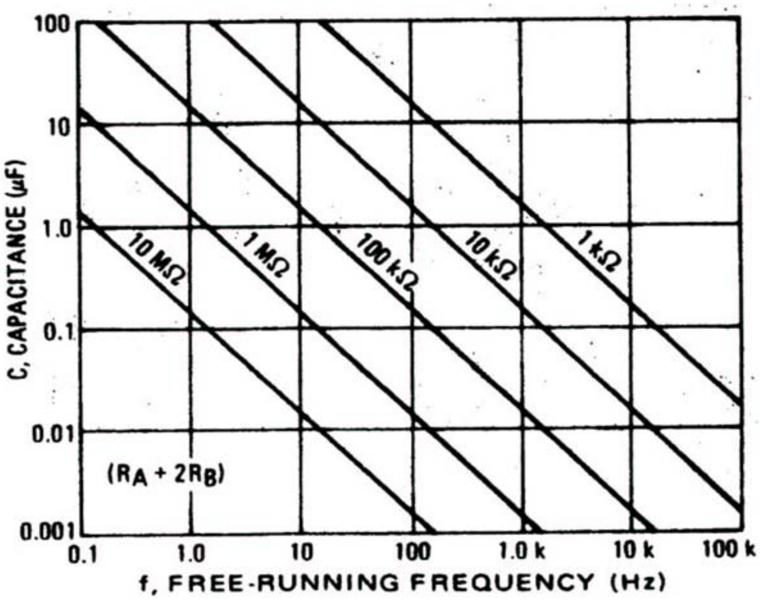
$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2 R_B) C}$$

The duty cycle (ratio of low time to entire period) may be determined from the following equation:

$$D = \frac{R_B}{R_A + 2R_B}$$

The nomograph below may also be used.

FIGURE 19 — FREE-RUNNING FREQUENCY



ASTABLE MONOGRAPH

APPLICATIONS

De-bounce circuit – in a situation where you have a computer monitoring a switch closure, you only wish to count the initial contact. Many times when a switch is closed the contacts bounce apart and come into contact again until the energy generated by the closure spring has dissipated. To a computer, each closure caused by bouncing is a unique closure and you will get the wrong number of counts. Using a 555 timer in monostable mode would have the computer count the rising edge of the output pulse as a closure happens. While the contacts are bouncing the pulse is still high and the computer ignores any subsequent closures until the output of the timer goes low.

Voltage Controlled Oscillator

Pulse Width Modulator

Square Wave Generator with a 50% duty cycle

Frequency Divider