# ESD - Electrostatic Discharge

**EPOW6860 – Project**

**RPI**

**12/14-2007**

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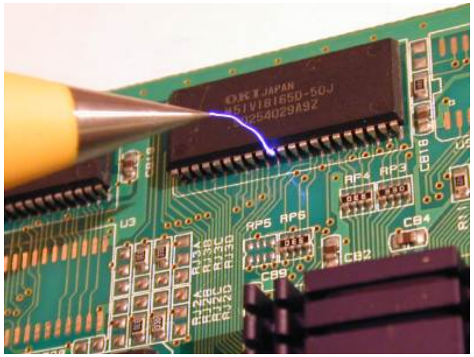
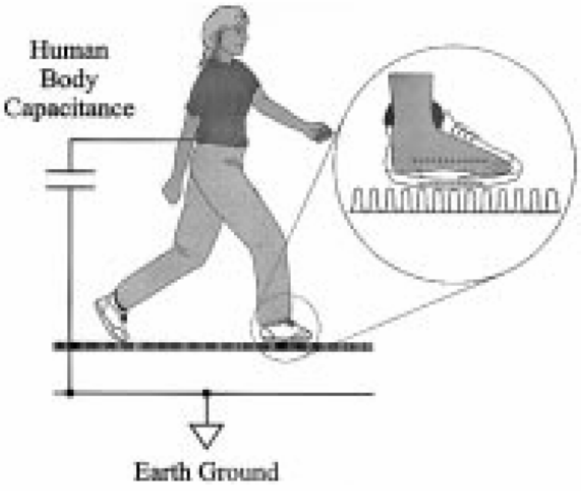
# What is ESD?

- A charged body, which gets discharged
- Arcs at high voltages
- Triboelectrification
  - Friction between two different materials, at least one insulator
- Properties of ESD
  - 100 to 35000 voltages
  - Up to 1000µ Jules of energy
  - 3000 - 4000V to se, feel or hear it





# Why is ESD of concern?

- Potential damage of semiconductive devices
  - The high voltages makes the layers or isolation between the layers breakdown
  - The energy is allocated faster than the material can dissipate it, and can make it melt

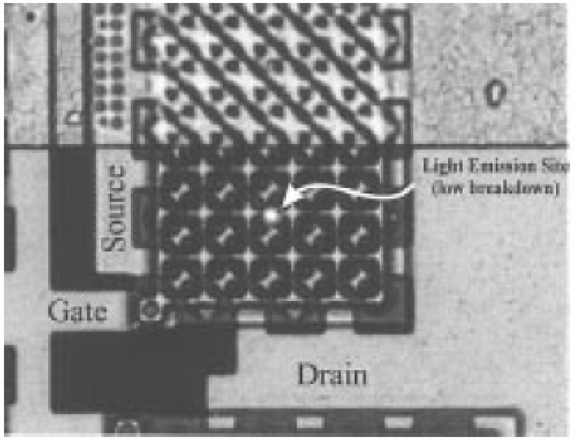



Fig. 15. EMMI photograph showing defect site causing lower breakdown of junction.

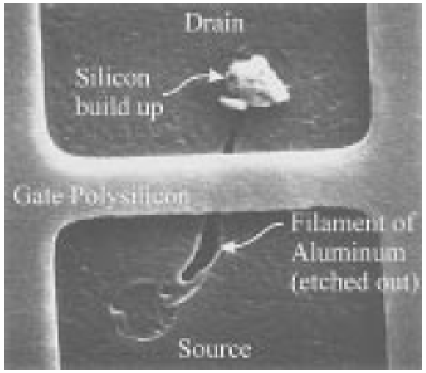
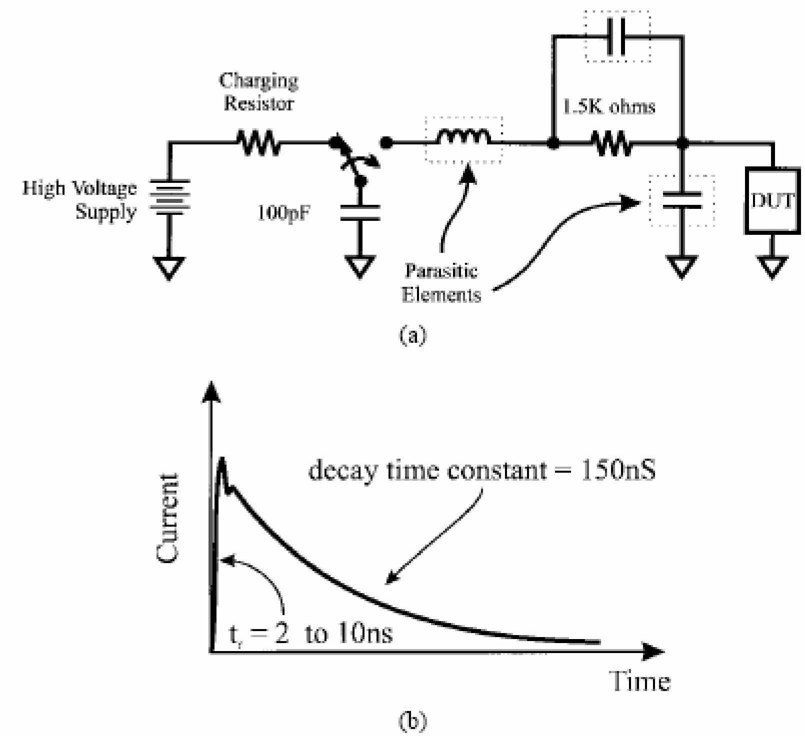



Fig. 16. Resulting short site when the transistor was subjected to EOS.

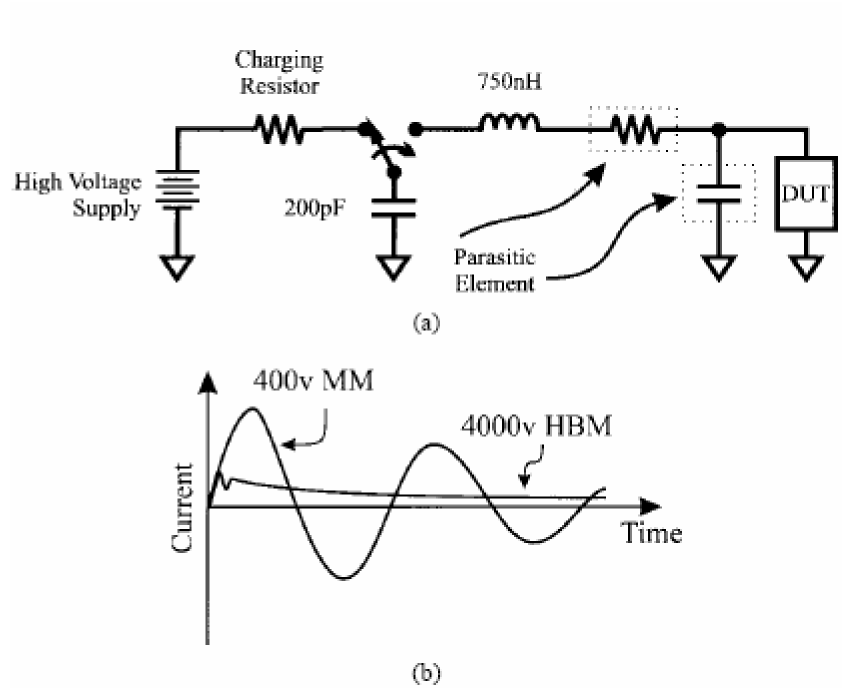
# ESD - Human Body Model(HBM)

- Charged human body
- Modeled as a capacitor and a series resistor
- Values specified in ESD standards
  - 100pF body capacitance
  - 1500Ω body resistance
  - 4000V
  - 0.4µC or 800µJ of energy



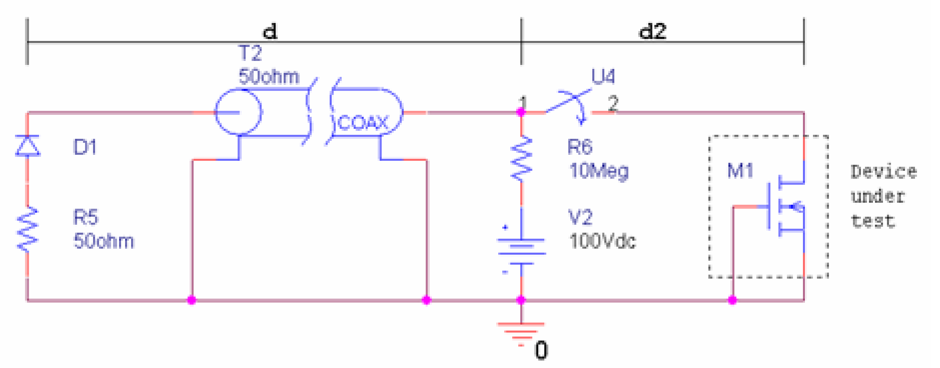
# ESD - Machine Model(MM)

- Charged machine body
  - Production machine, typically made of metal
  - Therefore no series resistance
- Modeled as a capacitor and series inductor
- Values specified in ESD standards
  - 200pF body capacitance
  - 750nH series inductance
  - 400V



# ESD - Transmission Line Pulsing(TLP)

- Charged transmission line
  - Grate Immunity to parasitic components
  - And therefore a good tool for ESD testing
- Basic circuit
  - Diode clamps any negative reflections, so the pulse doesn't bounce back again
  - High quality switch
  - 50Ω coaxial cable
  - Charged trough 10MΩ resistor
- Typical values for testing purposes
  - 50Ω coaxial cable
  - 90 - 100 nF/m
  - 10m generating a pulse of 100ns



# TLP - Basic principle

- Coaxial cable

$$Z_0 = 50[\Omega] \quad C_m \simeq 100[pF/m] \quad d = 10[m]$$

$$Z_0 = \sqrt{\frac{L_m}{C_m}} \;\Rightarrow\; L_m = {Z_0}^2 \cdot C_m \;\Rightarrow$$

$$L_m = 50^2 \cdot 100 \cdot 10^{-12} = 250[nH/m]$$

$$\nu = \frac{1}{\sqrt{L_m \cdot C_m}} \;\Rightarrow$$

$$\nu = \frac{1}{\sqrt{250[nH/m] \cdot 100[pF/m]}} = 2 \cdot 10^8[m/s]$$

$$T_1 = \frac{2 \cdot d}{\nu} = \frac{2 \cdot 10[m]}{2 \cdot 10^8[m/s]} = 100[ns]$$

$$T_2 = \frac{2 \cdot d_2}{\nu} = \frac{2 \cdot 0.5[m]}{2 \cdot 10^8[m/s]} = 5[ns]$$

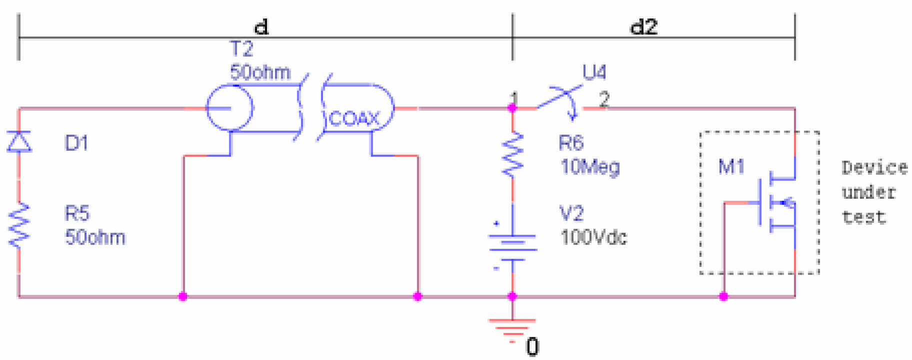
- Reflections

$$Z_{DUT} = 25[\Omega] \quad R_{Open} \simeq \infty$$

$$\Gamma_{a-b} = \frac{Z_b - Z_a}{Z_b + Z_a} \;\Rightarrow$$

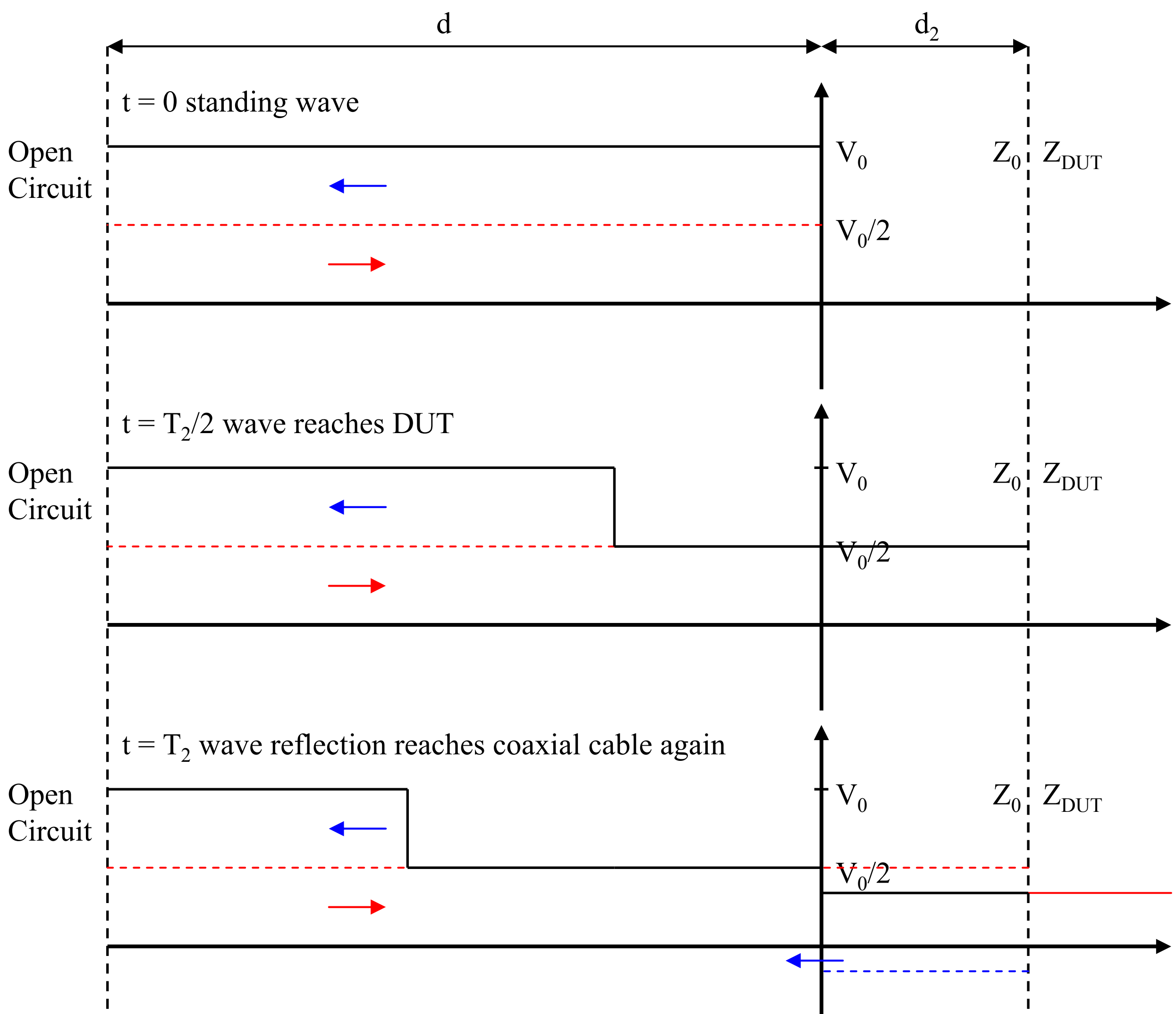
$$\Gamma_{DUT} = \frac{25 - 50}{25 + 50} = -0.333$$

$$\Gamma_{Open} = \frac{\infty - 50}{\infty + 50} = 1$$



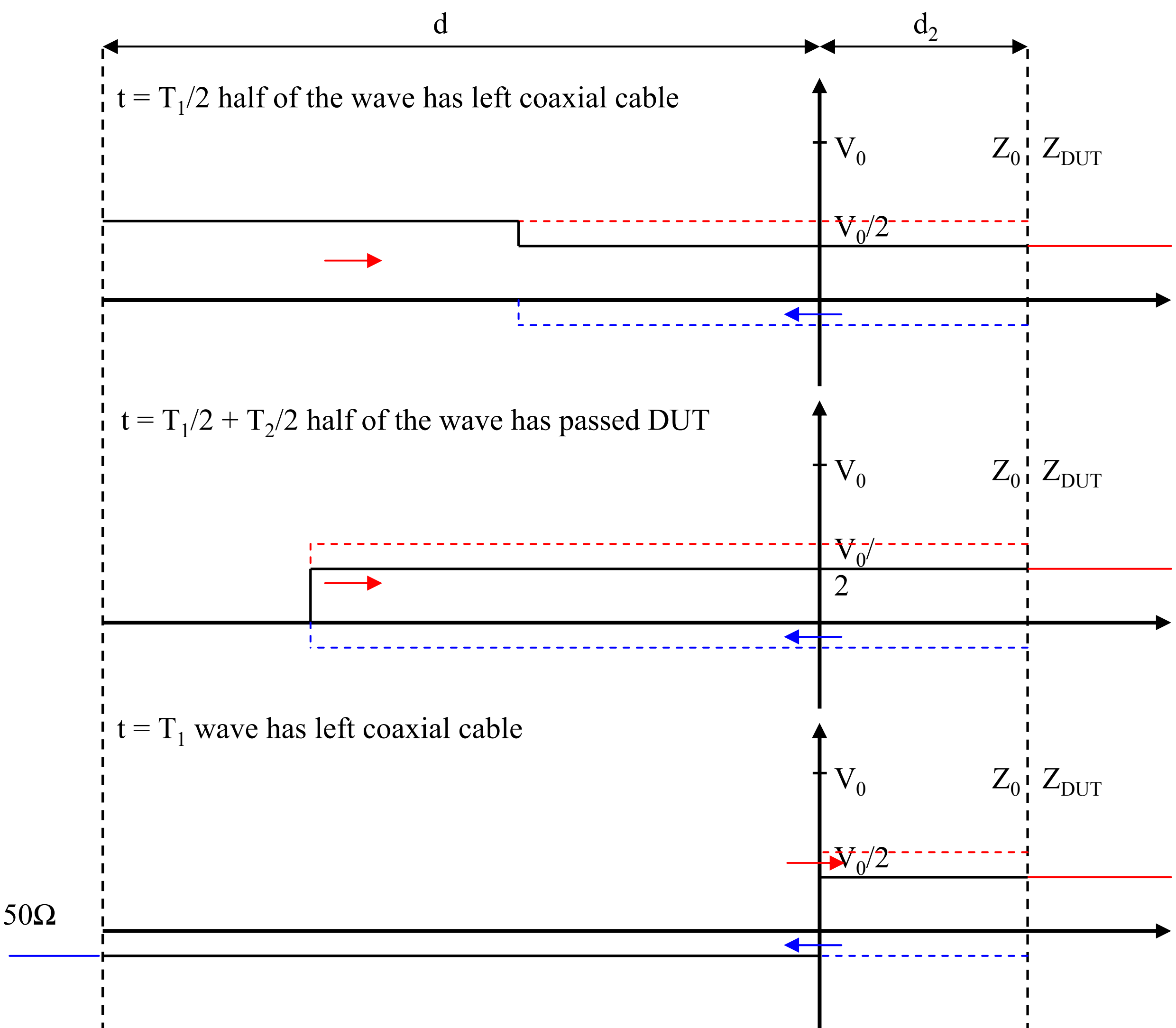
# TLP - Wave forms

Wave reflected by a factor of 1, du to the open circuit




Wave reflected by a factor of -0.333, du to the $Z_{DUT}$

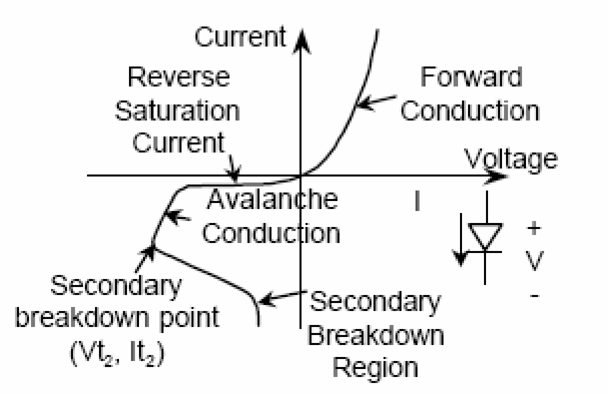
# TLP - Waveforms

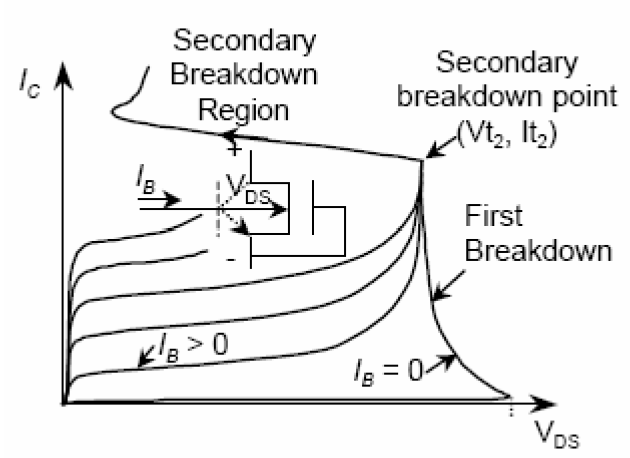



No reflection of wave, du to the 50Ω termination

# TLP - How to use this tool?

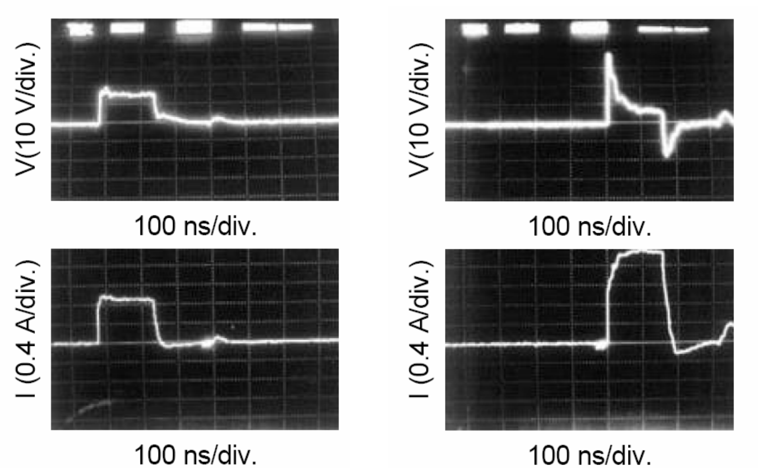
- Mapping the I-V characteristics
  - Trough a step increment of the voltage
- Finding the Secondary breakdown point($It_2$)
  - Where the semiconductor gets permanently damaged

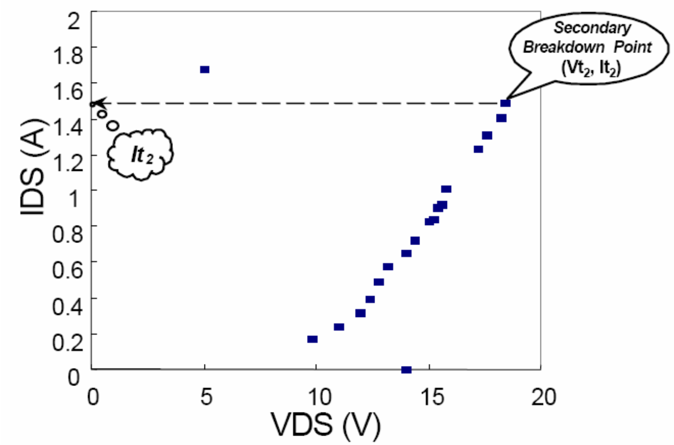


# TLP, I-V characteristics and ESD

- Linear connection between $It_2$ and HBM ESD voltage level
  - The higher $It_2$, the higher ESD robustness
  - So by finding $It_2$, you get a wary good idea of a components ESD robustness



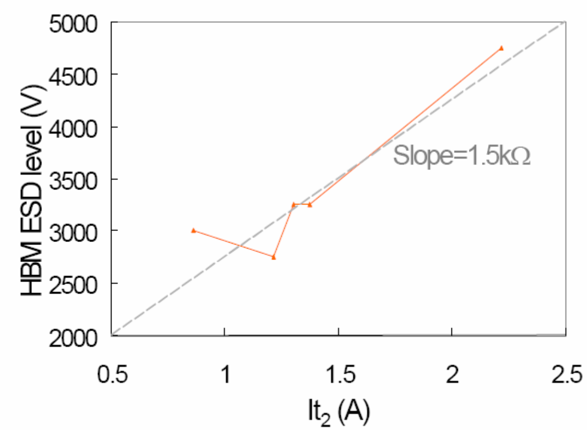
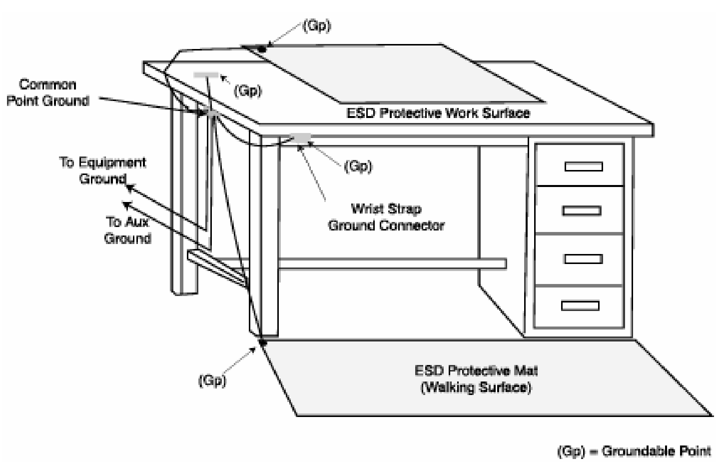




Fig.19 Dependence of the HBM ESD level on the $It_2$ of the ESD protection device.

# ESD protection

- ESD controlled workspace
  - Reducing the potential ESD build up
  - ESD packaging
  - ESD grounded workspace
  - Clean room(Controlled humidity and particles)




- ESD protection circuits on chip
  - Simplest form is clamp diodes, trying to direct the current away
  - Digital circuits is easier to protect, compared to a sensitive amplifier input

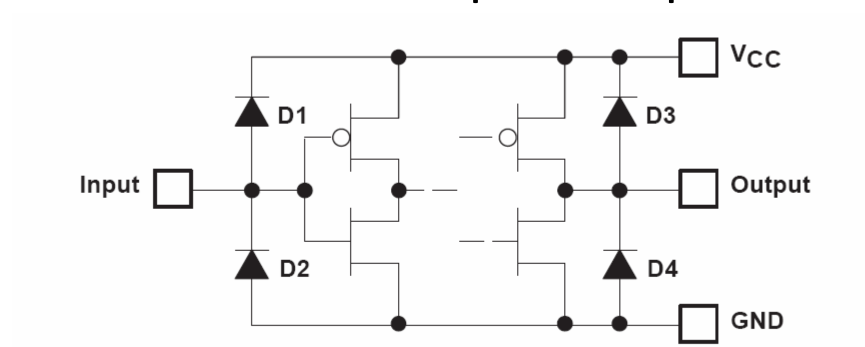



Figure 11. ESD-Protection Circuits Using Diodes