PHYSICS
LECTURE NOTES

PHYS 395
ELECTRONICS

University of Alberta
Department of Physics
1997

Preface

Electronics is one of the fastest expanding fields in research, application development and commercialization. Substantial growth in the field has occured due to World War II, the invention of the transistor, the space program, and now, the computer industry. The research grants are high, jobs are available and there is much money to be made in areas related to electronics. With the begin of the "information superhighway" and computerized video coming to your home, it is hard to imagine that electronics will not continue to expand in the future. Electronics is everywhere in our lives.

It is difficult for the practicing engineer to stay informed of the most recent developments in electronics. What is taught in this course could well be out of date by the time you actually go to use it. However the physical concepts of circuit behavour will be largely applicable to any future development.

The approach to electronics taken in this course will be a mixture of physical concepts and design principles. The course will thus appear more qualitative and wordy compare to other physics courses. Nevertheless, it is hoped that this course will become a useful tool for your future physics laboratories and research.

We can not begin to scratch the surface of the field of electronics in a one term course. Rather than cover a few topics in detail you will be exposed to most of the concepts and areas of design. The knowledge you gain will hopefully allow you to communicate with design engineers and technicians to enable them to design and build the electronics you require. You should also be equip to pursue any area of electronics that may interest you in the future. This will include reading more detailed texts, the component data sheets and manuals. As well as, understand the popular literature, including manuals for your stereo, computer, etc.. But above all I hope you find electronics interesting and enjoyable.

Contents

Chapter 1

Direct Current Circuits

These lectures follow the traditional review of direct current circuits, with emphasis on two-terminal networks and equivalent circuits. The idea is to bring you up to speed for what is to come. The course will get less quantitative as we go along. In fact, you will probably find the course gets easier as we go.

1.1 Basic Concepts

Direct current (DC) circuit analysis deals with constant currents and voltages, while alternating current (AC) circuit analysis deals with time-varying voltage and current signals whose time average values are zero. Circuits with time-average values of non-zero are also important and will be mentioned briefly in the section on filters. The DC circuit components considered in this course are the constant voltage source, constant current source, and resistor. Electronics also deals with charge Q, electric $\mathbf{E}$ and magnetic $\mathbf{B}$ fields, as well as, potential V. We will not be concerned with a detailed description of these quantities but will use approximation methods when dealing with them. Hence electronics can be considered as a more practical approach to these subjects. For the details look at your classical physics and quantum mechanics courses.

1.1.1 Current

The fundamental quantity in electronics is charge and at its basic level is due to the charge properties of the fundamental particles of matter. For all intensive purposes it is the electron (or lack of electrons) that matter. The role of the proton charge is negligible.

The aggregate motion of charges is called current I

$$I = \frac{dq}{dt}, \tag{1.1}$$

where dq is the amount of *positive* charge crossing a specified surface in a time dt. Be aware that the charges in motion are actually negative electrons. Thus the electrons move in the opposite direction to the current flow.

The SI unit for current is the ampere (A). For most electronic circuits the ampere is a rather large unit so the mA unit is more common.

1.1.2 Potential Difference

It is often more convenient to consider the electrostatic potential V rather than electric field $\mathbf{E}$ as the motivating influence for the flow of electric charge. The generalized vector properties of $\mathbf{E}$ are usually unimportant. The change in potential dV across a distance $d\vec{r}$ in an electric field is

$$dV = -\mathbf{E} \cdot d\vec{r}. \tag{1.2}$$

A positive charge will move from a higher to a lower potential. The potential is also referred to as the potential difference or, incorrectly, as just voltage:

$$V = V_{21} = V_2 - V_1 = \int_{V_1}^{V_2} dV. \tag{1.3}$$

Remember that current flowing in a conductor is due to a potential difference between its ends. Electrons move from a point of less positive potential to more positive potential and the current flows in the opposite direction.

The SI unit of potential difference is the volt (V).

1.1.3 Resistance and Ohm's Law

For most materials

$$V \propto I; \quad V = RI, \tag{1.4}$$

where $V = V_2 - V_1$ is the voltage **across** the object, I is the current **through** the object, and R is a proportionality constant called the resistance of the object. Resistance is a function of the material and shape of the object, and has SI units of ohms (Ω). It is more common to find units of kΩ and MΩ. The inverse of resistivity is conductivity.

> Resistor tolerances can be as bad as $\pm 20\%$ for general-purpose resistors to $\pm 0.1\%$ for ultra-precision resistors. Only wire-wound resistors are capable of ultra-precision applications.

The concept of *current through* and *potential across* are key to the understanding of and sounding intelligent about electronics.

Now comes the most useful visual tool of this course.

1.2 The Schematic Diagram

The schematic diagram consists of *idealized* circuit elements each represents some property of the *actual* circuit. Figure 1.1 shows some common circuit elements encountered in DC circuits. A two-terminal network is a circuit that has only two points of interest, say A and B.

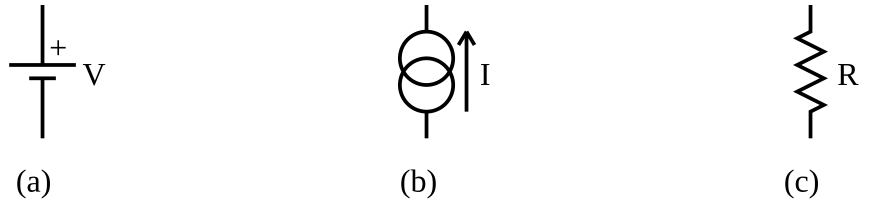


Figure 1.1: Common circuit elements encountered in DC circuits: a) ideal voltage source, b) ideal current source and c) resistor.

1.2.1 Electromotive Force (EMF)

Charge can flow in a material under the influence of an external electric field. Eventually the internal field due to the repositioned charge cancels the external electric field resulting in zero current flow. To maintain a potential drop (and flow of charge) requires an external energy source, ie. EMF (battery, power supply, signal generator, etc.). We will deal with two types of EMFs:

The *ideal voltage source* is able to maintain a constant voltage regardless of the current it must put out ($I \to \infty$ is possible).

The *ideal current source* is able to maintain a constant current regardless of the voltage needed ($V \to \infty$ is possible).

Because a battery cannot produce an infinite amount of current, a model for the behavior of a battery is to put an internal resistance in series with an ideal voltage source (zero resistance). Real-life EMFs can always be approximated with ideal EMFs and appropriate combinations of other circuit elements.

1.2.2 Ground

A voltage must always be measured relative to some reference point. It is proper to speak of the voltage across an electrical component but we often speak of voltage at a point. It is then assumed that the reference voltage point is ground.

Under strict definition, ground is the body of the earth. It is an infinite electrical sink. It can accept or supply any reasonable amount of charge without changing its electrical characteristics.

It is common, but not always necessary, to connect some part of the circuit to earth or ground, which is taken, for convenience and by convention, to be at zero volts. Frequently, a common (or reference) connection of the metal chassis of the instrument suffices. Sometimes there is a *common* reference voltage that is not at 0 V. Figure 1.2 show some common ways of depicting grounds on a circuit diagram.

When neither a ground nor any other voltage reference is shown explicitly on a schematic diagram, it is useful for purposes of discussion to adopt the convention that the bottom line on a circuit is at zero potential.

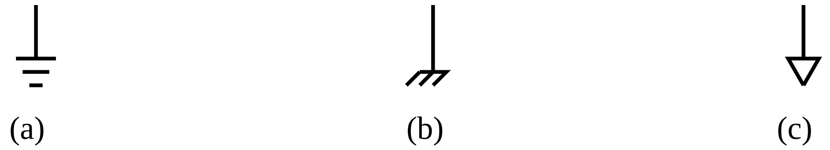


Figure 1.2: Some grounding circuit diagram symbols: a) earth ground, b) chassis ground and c) common.

1.3 Kirchoff's Laws

The conservation of energy and conservation of charge when applied to electrical circuits are known as Kirchoff's laws.

Conservation of energy – zero algebraic sum of the voltage drops V_i around a closed circuit loop (imaginary loop)

$$\sum_i V_i = 0. \tag{1.5}$$

Conservation of charge – zero algebraic sum of the currents I_k flowing into a point (total charge in, equals total charge out)

$$\sum_k I_k = 0. \tag{1.6}$$

When applying these laws to solve for circuit unknowns we will find the following definitions useful:

- an *element* is an impedance (resistance) or EMF (ideal voltage source or ideal current source),
- a *node* is a point where three or more current-carrying elements are connected,
- a *branch* is one element or several in series connecting two adjacent nodes, and
- an *interior loop* is a circuit loop not subdivided by a branch.

Using these definitions we can apply Kirchoff's laws to a circuit to solve for the unknown quantities. The general procedure is:

1. define the currents and voltages on a diagram,
2. apply Kirchoff's laws to loops and nodes,
3. write down a set of linear algebraic equations, and
4. solve for the unknowns.

But before we look at general circuits lets consider how simple resistors add.

1.3.1 Series and Parallel Combinations of Resistors

Circuit elements are connected in *series* when a common current passes through each element. The equivalent resistance R_{eq} of a combination of resistors R_i connected in series is given by summing the voltage drops across each resistor.

$$V = \sum_i V_i = I \sum_i R_i, \tag{1.7}$$

$$R_{\text{eq}} = \sum_i R_i. \tag{1.8}$$

If $R_j \gg R_k$, where R_k are all the other resistors than $R_{\text{eq}} \approx R_j$; the largest resistor wins.

Circuit elements are connected in *parallel* when a common voltage is applied across each element. The equivalent resistance R_{eq} of a combination of resistors R_i connected in parallel is given by summing the current through each resistor

$$I = \sum_i I_i = \sum_i \frac{V}{R_i}, \tag{1.9}$$

$$\frac{1}{R_{\text{eq}}} = \frac{I}{V} = \sum_i \frac{1}{R_i}, \tag{1.10}$$

$$R_{\text{eq}} = \frac{\prod_i R_i}{\sum_i \prod_{j\neq i} R_j}. \tag{1.11}$$

If $R_j \ll R_k$, where R_k are all the other resistors than $R_{\text{eq}} \approx R_j$; the smallest resistor wins.

The following "divider" circuits are useful combinations of resistors. Believe it or not, they are a super useful concept that will often be used in one form or another; learn it.

1.3.2 Voltage Divider

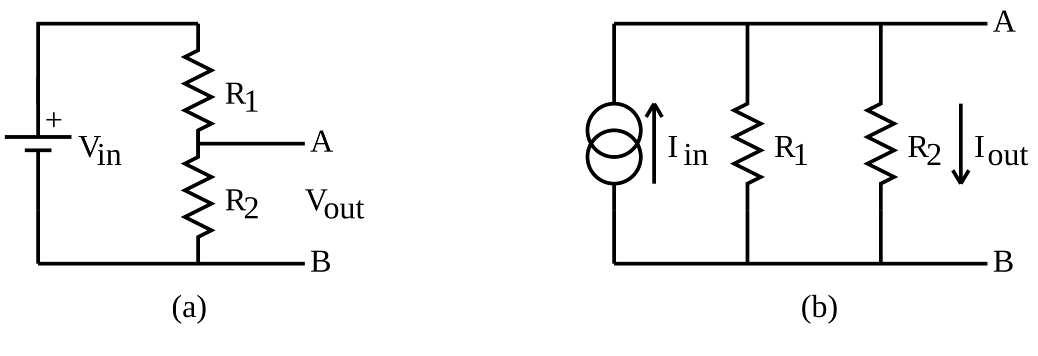


Figure 1.3: Divider circuits: a) voltage divider and b) current divider.

Consider the voltage divider shown in figure 1.3a. The voltage across the input source is $V_{\text{in}} = (R_1 + R_2)I$ and the voltage across the output between terminals A and B is $V_{\text{out}} = R_2 I$. The output voltage from the voltage divider in thus

$$V_{\rm out} = \frac{R_2}{R_1 + R_2} V_{\rm in}. \tag{1.12}$$

Example: *Determine an expression for the voltage V_2 on the voltage divider in figure 1.4.*

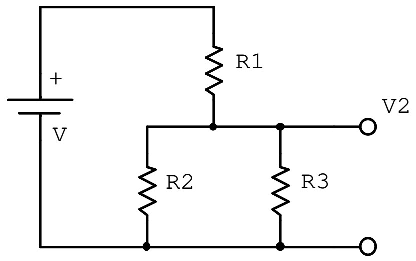


Figure 1.4: Example voltage divider.

We take the bottom line in figure 1.4 to be at ground and define the current flowing between V_2 and ground to be I. Ohm's law gives

$$V_2 = IR_{23}, \quad where \quad R_{23} = \frac{R_2 R_3}{R_2 + R_3}. \tag{1.13}$$

Applying Kirchoff's voltage law for the input source gives

$$V = IR, \quad where \quad R = R_1 + R_{23}. \tag{1.14}$$

Combining the above two results and solving for V_2 leads to

$$V_2 = \frac{R_{23}}{R} V = \frac{\frac{R_2 R_3}{R_2 + R_3}}{R_1 + \frac{R_2 R_3}{R_2 + R_3}} V \tag{1.15}$$

$$= \frac{R_2 R_3}{R_1 R_2 + R_2 R_3 + R_3 R_1} V. \tag{1.16}$$

1.3.3 Current Divider

Consider the current divider shown in figure 1.3b. The source current is divided between the two resistors and is given by $I_{in} = I_1 + I_2 = V/R_1 + V/R_2$. The current at the output is $V = I_{out} R_2$. The output current from the current divider is thus

$$I_{\rm out} = \frac{R_1}{R_1 + R_2} I_{\rm in}. \tag{1.17}$$

Example: *Determine an expression for the current I_3 through the resistor R_3 in the circuit shown in figure 1.5.*
The current I is divided amongst the three resistors and hence we use our expression for resistors in parallel

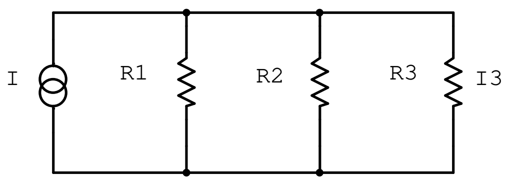


Figure 1.5: Example current divider.

$$V = R_{123} I = \frac{R_1 R_2 R_3}{R_1 R_2 + R_2 R_3 + R_3 R_1} I. \tag{1.18}$$

Let V be the common voltage across the three parallel resistors. The current through R_3 is thus

$$I_3 = \frac{V}{R_3} = \frac{R_1 R_2}{R_1 R_2 + R_2 R_3 + R_3 R_1} I. \tag{1.19}$$

Now lets consider some general approaches to solving for unknowns in circuits.

1.3.4 Branch Current Method

Use both of Kirchoff's laws. *But be aware that an arbitrary application of Kirchoff's two equations will not always yield an independent set of equations.* But the following approach will probably work.

1. Label the current in each branch (do not worry about the direction of the actual current).
2. Use only interior loops and all but one node.
3. Solve the system of algebraic equations.

1.3.5 Loop Current Method

This method is also refereed to as the mesh loop method. The independent current variables are taken to be the circulating current in each of the interior loops.

1. Label interior loop currents on a diagram.
2. Obtain expressions for the voltage changes around each interior loop.
3. Solve the system of algebraic equations.

Depending on the problem, it may ultimately be necessary to algebraically sum two loop currents in order to obtain the needed interior branch current for the final answer.

Lets consider the example of the Wheatstone bridge circuit shown in figure 1.6. We wish to calculate the currents around the loops. The three currents are identified as: I_a the clockwise current around the large interior loop which includes the EMF, I_b the clockwise current around the top equilateral triangle, and I_c the clockwise current around the bottom equilateral triangle. The voltage loop expressions for the three current loops are

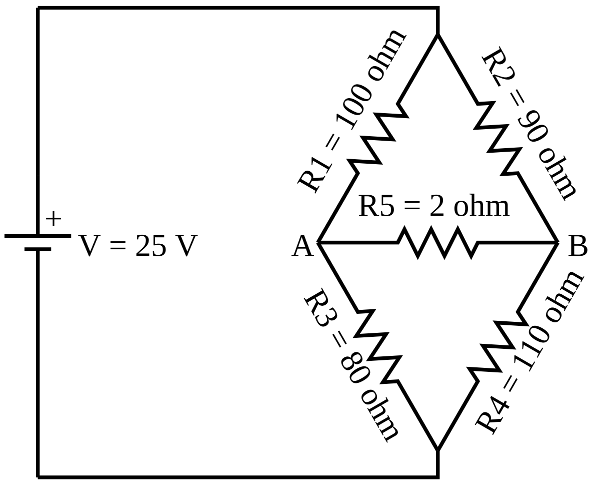


Figure 1.6: Loop method for the Wheatstone bridge circuit.

$$V = R_1(I_a - I_b) + R_3(I_a - I_c) \tag{1.20}$$

$$0 = R_1(I_b - I_a) + R_2 I_b + R_5(I_b - I_c) \tag{1.21}$$

$$0 = R_3(I_c - I_a) + R_5(I_c - I_b) + R_4 I_c. \tag{1.22}$$

Collecting terms containing the same current,

$$V = I_a(R_1 + R_3) - I_b R_1 - I_c R_3 \tag{1.23}$$

$$0 = -I_a R_1 + I_b(R_1 + R_2 + R_5) - I_c R_5 \tag{1.24}$$

$$0 = -I_a R_3 - I_b R_5 + I_c(R_3 + R_4 + R_5). \tag{1.25}$$

If the values for the parameters shown in the diagram are used, the current values can be found by solving the set of simultaneous equations to give

$$I_a = 0.267A, \quad I_b = 0.140A, \quad \text{and} \quad I_c = 0.113A. \tag{1.26}$$

Moreover, if we number the individual currents through each resistor using the same scheme as we have for each component (current through R_1 is I_1, R_2 has I_2, etc.) and identify I_0 as the current out of the battery, then

$$I_0 = I_a = 0.267A \tag{1.27}$$

$$I_1 = I_a - I_b = 0.127A \tag{1.28}$$

$$I_2 = I_b = 0.140A \tag{1.29}$$

$$I_3 = I_a - I_c = 0.154A \tag{1.30}$$

$$I_4 = I_c = 0.113A \tag{1.31}$$

$$I_5 = I_b - I_c = 0.027A. \tag{1.32}$$

These are the same currents that would be found using only Kirchoff's equations; however, here we had to handle only three simultaneous equations instead of six.

Example: *Use the loop current method to determine the voltage developed across the terminals AB in the circuit shown in figure 1.7.*

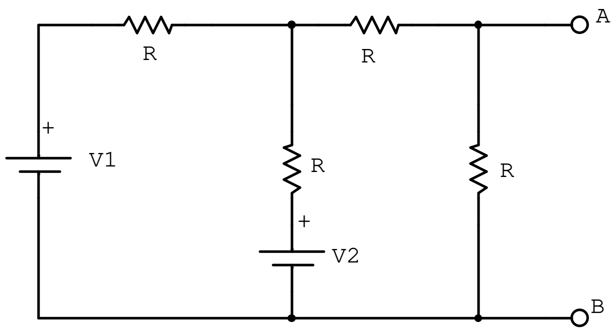


Figure 1.7: Example circuit for analysis using the loop current method.

Consider the clockwise current loop I_A through the two resistors and the two potentials. Similarly consider the clockwise current I_B around the other internal loop consisting of the three resistors and V_2. Kirchoff's law gives

$$V_1 - I_A(2R) + I_B R - V_2 = 0 \quad loop\ A. \tag{1.33}$$

$$V_2 - I_B(3R) + I_A R = 0 \quad loop\ B. \tag{1.34}$$

Solving the above two equations for the unknown loop currents I_A and I_B gives

$$\begin{aligned} V_1 - V_2 &= 2RI_A - RI_B && (1.35)\\ V_2 &= -RI_A + 3RI_B, && (1.36)\end{aligned}$$

$$\begin{pmatrix} V_1 - V_2 \\ V_2 \end{pmatrix} = \begin{pmatrix} 2R & -R \\ -R & 3R \end{pmatrix} \begin{pmatrix} I_A \\ I_B \end{pmatrix} \equiv \mathcal{R} \begin{pmatrix} I_A \\ I_B \end{pmatrix}, \quad (1.37)$$

$$\mathcal{R}^{-1} = \frac{1}{R} \begin{pmatrix} 3/5 & 1/5 \\ 1/5 & 2/5 \end{pmatrix}, \quad (1.38)$$

$$\begin{aligned} I_A &= \frac{1}{R}\left[\frac{3}{5}(V_1 - V_2) + \frac{1}{5}V_2\right] = \frac{1}{R}\left(\frac{3}{5}V_1 - \frac{2}{5}V_2\right) && (1.39)\\ I_B &= \frac{1}{R}\left[\frac{1}{5}(V_1 - V_2) + \frac{2}{5}V_2\right] = \frac{1}{R}\left(\frac{1}{5}V_1 + \frac{1}{5}V_2\right). && (1.40)\end{aligned}$$

The voltage across AB is given simply by

$$\begin{aligned} V_{AB} &= I_B R && (1.41)\\ &= \frac{1}{5}(V_1 + V_2). && (1.42)\end{aligned}$$

1.4 Equivalent Circuits

Equivalent circuits is often the hardest concept and most numerically intensive in the course. Learning them well could make a difference on your midterm exam. Look in several books until you find the explanation you understand best.

Since Ohm's law and Kirchoff's equations are linear, we can replace any DC circuit by a simplified circuit. Just like a combination of resistors and Ohm's law could give an equivalent resistor, a combination of circuit elements and Kirchoff's laws can give an equivalent circuit. Two possibilities are shown in figure 1.8.

1.4.1 Thevenin's and Norton's Theorems

A Thevenin equivalent circuit contains an equivalent voltage source V_{Th} in series with an equivalent resistor R_{Th}. A Norton equivalent circuit contains an equivalent current source I_{N} in parallel with an equivalent resistor R_{N}.

1.4.2 Determination of Thevenin and Norton Circuit Elements

One approach to determine the equivalent circuits is:

1. Thevenin – calculate the open-circuit voltage $V_{AB} = V_{\mathrm{Th}}$.

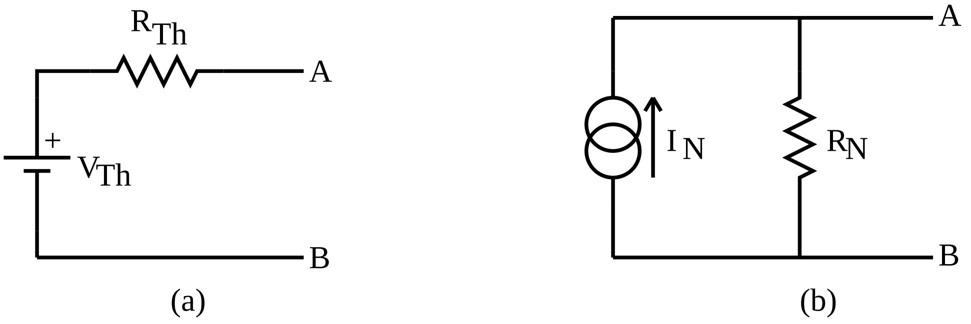


Figure 1.8: Thevenin and Norton equivalent circuits.

2. Norton – calculate the short-circuit current between A and B; I_{N}.

3. $R_{\mathrm{Th}} = R_{\mathrm{N}} = V_{\mathrm{Th}}/I_{\mathrm{N}}$.

An alternative to step 2 is to short all voltage sources, open all current sources, and calculate the equivalent resistance remaining between A and B. We will use this later approach whenever manageable. To see if you understand equivalent circuits so far, convince yourself that $R_{\mathrm{Th}} = R_{\mathrm{N}}$.

Solution: *From Thevenin's theorem*

$$V_{\mathrm{AB}}(\mathrm{open}) = V_{\mathrm{Th}} \tag{1.43}$$
$$I_{\mathrm{AB}}(\mathrm{short}) = \frac{V_{\mathrm{Th}}}{R_{\mathrm{Th}}}. \tag{1.44}$$

According to Notron's theorem

$$V_{\mathrm{AB}}(\mathrm{open}) = I_{\mathrm{N}} R_{\mathrm{N}} \tag{1.45}$$
$$I_{\mathrm{AB}}(\mathrm{short}) = I_{\mathrm{N}}. \tag{1.46}$$

Therefore

$$V_{\mathrm{Th}} = I_{\mathrm{N}} R_{\mathrm{N}} \quad \text{and} \tag{1.47}$$
$$\frac{V_{\mathrm{Th}}}{R_{\mathrm{Th}}} = I_{\mathrm{N}}. \tag{1.48}$$

$$\Rightarrow R_{\mathrm{Th}} = R_{\mathrm{N}} \tag{1.49}$$

Lets now return to our Wheatstone bridge example shown in figure 1.6. We will calculate the current through R_5 by replacing the rest of the circuit by its Thevenin equivalent.

- R_5 is removed and the open terminals are labeled V_{Th}. The polarity assigned is arbitrary and will be verified in the calculations.

- The evaluation of V_{Th} is performed using Kirchoff's laws:

$$0 = 25 - (100 + 80)I_1 \tag{1.50}$$

$$0 = 25 - (90 + 110)I_2 \tag{1.51}$$

$$0 = 100I_1 + V_{\mathrm{Th}} - 90I_2 \tag{1.52}$$

The result is $V_{\mathrm{Th}} = -2.64$ V. The minus sign means only that the arbitrary choice of polarity was incorrect.

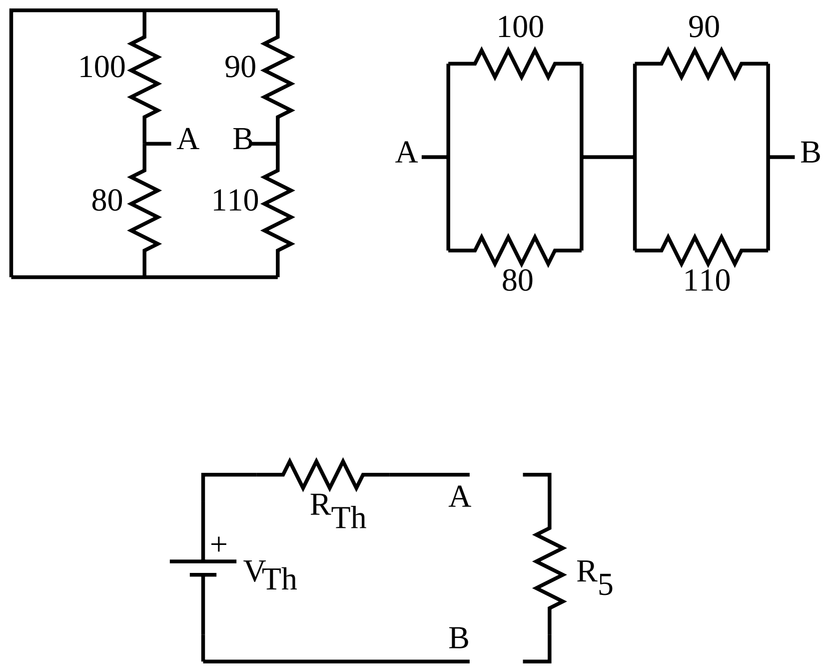


Figure 1.9: Thevenin's theorem applied to the Wheatstone bridge circuit.

- The voltage source is shorted out and R_{Th} is calculated (figure 1.9):

$$R_{\mathrm{Th}} = \frac{(100)(80)}{100 + 80} + \frac{(90)(110)}{90 + 110} = 93.94\Omega \tag{1.53}$$

Note that when the source is shorted out, the resistors that were in series (R_1 and R_3; R_2 and R_4) become parallel combinations.

- The network is assembled in series as shown in figure 1.9 and the current through R_5 is calculated.

$$I_5 = \frac{V_{\rm Th}}{R_{\rm Th} + R_5} = \frac{-2.64}{93.94 + 2} = -0.027A \tag{1.54}$$

Note that the numerical value of the current is the same as that in the preceding calculations, but the sign is opposite. This is simply due to the incorrect choice of polarity of $V_{\rm Th}$ for this calculation. In fact, the current flow is in the same direction in both examples, as would be expected.

Example: *Find the Thevenin equivalent components $V_{\rm Th}$ and $R_{\rm Th}$ for the circuit in figure 1.10.*

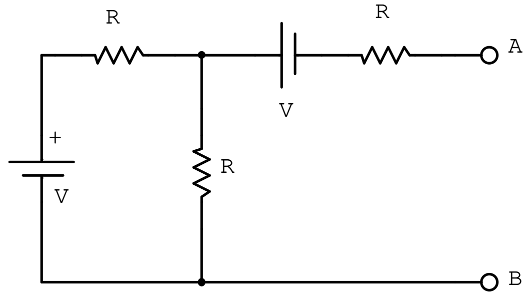


Figure 1.10: Example circuit for analysis using a Thevenin equivalent circuit.

Shorting the V's to find R_{Th} gives two resistors in parallel, which are in series with a third resistor:

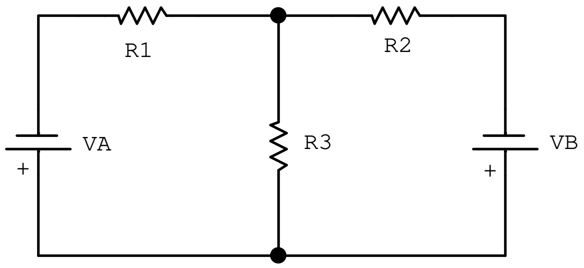
$$R_{\rm Th} = R + \frac{RR}{R+R} = \frac{3}{2}R. \tag{1.55}$$

The open circuit voltage gives V_{Th}. For the open circuit no current flows from the node joining the two resistors to A. A is thus at -V relative to this node. Around the interior loop $V_{loop} = \frac{V}{2}$ (cf. voltage divider).
Therefore

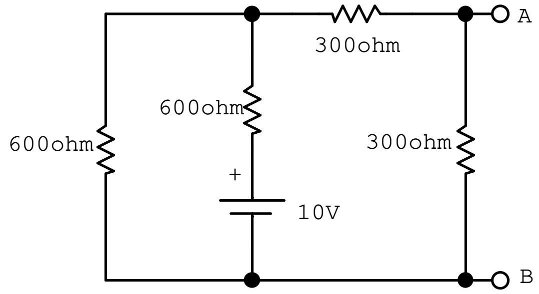
$$V_{AB} = V_{loop} - V = -\frac{V}{2}. \tag{1.56}$$

1.5 Problems

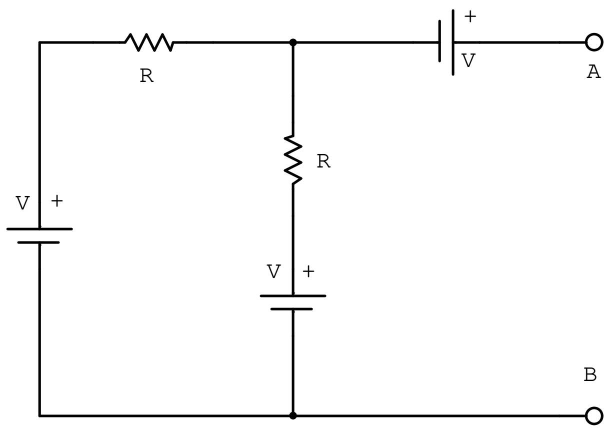
1. Find the current in each resister in the circuit shown below. $V_A = 2$ V, $V_B = 4$ V, $R_1 = 100\ \Omega, R_2 = 500\ \Omega$ and $R_3 = 600\ \Omega$. *Hint: writing down the loop-current equations in terms of the symbols will give you most of the marks.*



2. Determine the Thevenin equivalent circuit of the circuit shown below. *Hint: determine V_{th} and R_{th}.*



3. Consider the following circuit:

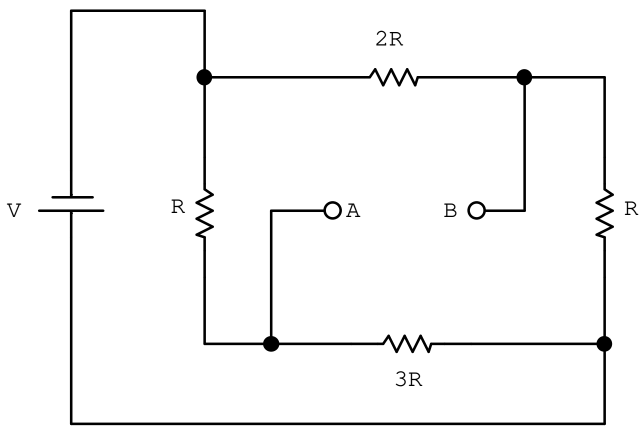


   (a) What is the Thevenin equivalent voltage?

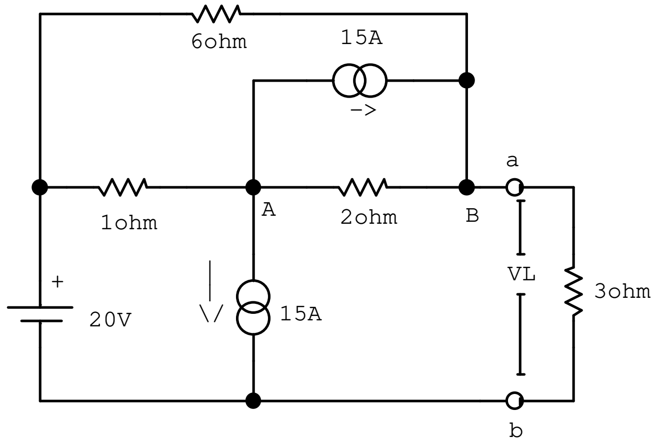
(b) What is the Thevenin equivalent resistance?

(c) For a variable load resistance placed externally between the terminals A and B, plot the current through the load as a function of V_{AB}. Label the intercepts on both axes.

4. Sketch the current though a load resistance as a function of V_{AB} for the circuit shown below. Label both intercepts and the slope.



5. Find the voltage, V_L, across the 3 Ω load resistor for the circuit below by replacing the remaining circuit by its Thevenin equivalent. *Hint: You can check your answer by direct analysis of the entire circuit.*



Chapter 2

Alternating Current Circuits

We now consider circuits where the currents and voltages may vary with time ($V = V(t)$, $I = I(t)$ (also $Q = Q(t)$)). These lectures will concentrate on the special case in which the signals are periodic, with time average values of zero ($\langle v(t) \rangle = \langle i(t) \rangle = 0$). Circuits with these signals are referred to as alternating current (AC) circuits. In general signals will have both DC and AC properties ($v(t) = V_{\mathrm{AC}}(t) + V_{\mathrm{DC}}$). We will concentrate only on the AC components and assume that the DC properties can be treated separately using the methods of the previous lectures.

The algebraic equations representing Kirchoff's laws for DC circuits will take the form of differential equations for AC circuits. So now is a good time to review your differential equations and complex number theory because we will use it.

2.1 AC Circuit Elements

In physical terms, EMFs can be regarded as circuit elements which put energy into a circuit and a resistor R as an element which removes energy from a circuit. The energy is dissipated in the resistor as heat. In AC circuits we have the additional circuit elements, capacitance C and inductance L, which store energy in electric and magnetic fields respectively. C and L are referred to as *reactive* elements while R is a resistive element. All three of these element are considered passive elements. We will encounter *active* circuit elements in the lectures to follow. For simplicity we will ignore radiation that might be emitted from high frequency circuits.

2.1.1 Capacitance

The fundamental property of a capacitor is that it can store charge and hence electric field energy. The capacitance C between two appropriate surfaces is defined by

$$V = \frac{Q}{C}, \tag{2.1}$$

where V is the potential difference between the surfaces and Q is the magnitude of the charge distributed on either surface.

In terms of current, $I = dQ/dt$ implies

$$\frac{dV}{dt} = \frac{1}{C}\frac{dQ}{dt} = \frac{I}{C}. \tag{2.2}$$

In electronics we take $I = I_D$ (displacement current). In other words, the current flowing from or to the capacitor is taken to be equal to the displacement current through the capacitor. You should be able to show that capacitors add linearly in when placed in parallel.

There are four principle functions of a capacitor in a circuit.

1. Since Q and $\mathbf{E}$ can be stored a capacitor can be used as (non-ideal) source of I and V.

2. Since a capacitor passes AC current but not DC current it can be used to connect parts of a circuit that must operate at different DC voltage levels.

3. A capacitor and resistor in series will limit current and hence smooth sharp edges in voltage signals.

4. Charging or discharging a capacitor with a constant current results in the capacitor have a voltage signal with a constant slope, ie. $dV/dt = I/C =$ constant if I is a constant.

Some capacitors (electrolytic) are asymmetric devices with a polarity that must be hooked-up in a definite way. You will learn this in the lab. The SI unit for capacitance is farad (F). The capacitance in a circuit is typically measured in μF or pF. Non-ideal circuits will have stray capacitance, leakage currents and inductive coupling at high frequency. Although important in real circuit design we will slip over these nasties at this point.

> Capacitors can be obtained in various tolerance rating from $\pm 20\%$ to $\pm 0.5\%$. Because of dimensional changes, capacitors have a high temperature dependence of capacitance. A capacitor does not hold a charge indefinitely because the dielectric is never a perfect insulator. Capacitors are rated for leakage, the conduction through the dielectric, by the leakage resistance-capacitance product in $\mathrm{M}\Omega \cdot \mu$F. High temperature increases leakage.

2.1.2 Inductance

Faraday's law applied to an inductor states that a changing current induces a back EMF that opposes the change. Or

$$V = V_A - V_B = L\frac{dI}{dt}. \tag{2.3}$$

Where V is the voltage across the conductor and L is the inductance measured in henry (H). The more common units encountered in circuits are μH and mH.

The inductance will tend to smooth sudden changes in current just as the capacitance smoothes sudden changes in voltage. Of course, if the current is constant there will be no induced EMF. So unlike the capacitor which behaves like an open-circuit in DC circuits, an inductor behaves like a short-circuit in DC circuits.

Applications using inductors are less common than those using capacitors, but inductors are very common in high frequency circuits. We will again skip over the unpleasantness – that non-ideal inductors have some resistance and some capacitance.

> Inductors are never pure inductances because there is always some resistance in and some capacitance between the coil windings. When choosing an inductor (occasionally called a choke) for a specific application, it is necessary to consider the value of the inductance, the DC resistance of the coil, the current-carrying capacity of the coil windings, the breakdown voltage between the coil and the frame, and the frequency range in which the coil is designed to operate. To obtain a very high inductance it is necessary to have a coil of many turns. The inductance can be further increased by winding the coil on a closed-loop iron or ferrite core. To obtain as pure an inductance as possible, the DC resistance of the windings should be reduced to a minimum. This can be done by increasing the wire size, which of course, increases the size of the choke. The size of the wire also determines the current-handling capacity of the choke since the work done in forcing a current through a resistance is converted to heat in the resistance. Magnetic losses in an iron core also account for some heating, and this heating restricts any choke to a certain safe operating current. The windings of the coil must be insulated from the frame as well as from each other. Heavier insulation, which necessarily makes the choke more bulky, is used in applications where there will be a high voltage between the frame and the winding. The losses sustained in the iron core increases as the frequency increases. Large inductors, rated in henries, are used principally in power applications. The frequency in these circuits is relatively low, generally 60 Hz or low multiples thereof. In high-frequency circuits, such as those found in FM radios and television sets, very small inductors (of the order of microhenries) are frequently used.

2.2 Circuit Equations

Recall that voltage V is related to current I, via the passive DC circuit element resistance R, by Ohm's law $V = IR$. Analogously, the change in voltage and change in current are related to the current and voltage, via the passive AC circuit elements C and L, by

$$\frac{dV}{dt} = \frac{I}{C} \quad \text{and} \quad V = L\frac{dI}{dt}. \tag{2.4}$$

Applying the above three equations, along with Kirchoff's loop rule, to AC circuits results in a set of differential equations. These differential equations are linear with constant coefficients and can easily be solve for $Q(t)$, $I(t)$, and $V(t)$. In general the solutions will consist of a *transient* response and a *steady-state* response. The transient response describes the return to equilibrium after the EMFs change suddenly. The steady-state response describes the long term behaviour when the circuit is driven by a sinusoidal source.

We will first consider the transient response. This will be one of the few times we consider non-oscillating AC behaviour. Since Ohm's law and Kirchoff's laws are linear we can use complex exponential signals and take real or imaginary parts in the end. This is not true for power, since it is non-linear (product of signals).

2.2.1 RC Circuit

Consider the resistor R and capacitance C in the circuit loop in figure 2.1. Notice that there is no source.

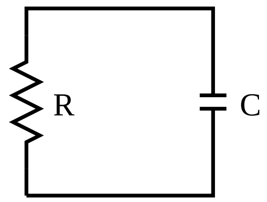


Figure 2.1: RC circuit.

We start with a differential version of Kirchoff's voltage law.

$$\frac{d}{dt}\sum_i V_i = \sum_i \frac{dV_i}{dt} = 0. \tag{2.5}$$

When applied to our circuit

$$\frac{dV_C}{dt} + \frac{dV_R}{dt} = 0, \tag{2.6}$$

where V_C is the voltage drop across the capacitor and V_R is the voltage drop across the resistor.

The change in the voltage drop across the capacitor is give by our previous expression.

$$\frac{dV_C}{dt} = \frac{I}{C}. \tag{2.7}$$

The change in the voltage drop across the resistor can be obtained from Ohm's law

$$V_R = RI \Rightarrow \frac{dV_R}{dt} = R\frac{dI}{dt}. \tag{2.8}$$

Substituting these changes in voltage into Kirchoff's equation gives

$$\frac{I}{C} + R\frac{dI}{dt} = 0, \tag{2.9}$$

where the current due to the flow of charge on or off the capacitor is the same as through the resistor.

Now we need some initial conditions. Notice that although the capacitor behaves as an open circuit to DC, current must flow to charge or discharge the capacitor. Lets take the case where the capacitor is initially charged and then the circuit is closed and the charge is allow to drain off the capacitor (eg. closing a switch). The resulting current will flow through the resistor.

Solving for the current we obtain

$$I(t) = I_0 e^{-t/RC}, \tag{2.10}$$

where $I(t=0) = I_0$ is the initial current given by Ohm's law

$$I_0 = \frac{V_0}{R}. \tag{2.11}$$

Using a time dependent version of Ohm's law we can solve for the voltage across the resistor

$$V(t) = RI(t) = RI_0 e^{-t/RC} = V_0 e^{-t/RC} = V_0 e^{-t/\tau}, \tag{2.12}$$

where $V(t=0) \equiv V_0$ is the initial voltage across the capacitor and $\tau \equiv RC$ is the commonly defined time constant of the decay. You should also be able to solve for the voltage across the capacitor and charge on the capacitor.

For the case of an applying voltage V_B being suddenly place into the circuit (inserting a battery) the capacitor is initial not charged and the voltage across the capacitor is

$$V(t) = V_B(1 - e^{-t/\tau}). \tag{2.13}$$

In the first case, current and voltage exponentially decay away with time constant τ when the switch is closed. The charge flows off the capacitor and through the resistor. The energy initially stored in the capacitor is dissipate in the resistor.

In the second case the capacitor charges to a voltage V_B until no current flows and hence the voltage drop across the resistor is zero. Energy from the battery is stored in the capacitor.

In both cases the characteristic RC time constant occurs. In general this is true of all resistor-capacitor combinations and will be of importance throughout the course.

2.2.2 RL Circuit

The response of the RL circuit, shown in figure 2.2, is similar to that of the RC circuit. There are however some significant differences.

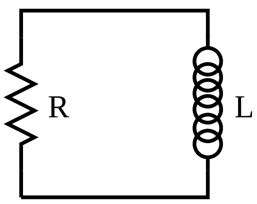


Figure 2.2: RL circuit.

If a battery is inserted into the circuit the current raises quickly from zero to some finite value. The EMF generated in the inductor impedes the current flow until it is constant.

The expression for the current in the RL circuit is

$$i(t) = \frac{V_B}{R}(1 - e^{-tR/L}) \tag{2.14}$$

where the time constant is now

$$\tau = \frac{L}{R}. \tag{2.15}$$

The voltage across the resistor is an increasing exponential unlike the RC circuit in which the voltage across the resistor decreased exponentially. Likewise, the voltage across the inductor decreases with time while in the RC circuit the voltage across the capacitor increased with time.

There are other initial conditions we could work with in this circuit but these can now be worked out by the student.

2.2.3 LC Circuit

Lets now consider the LC circuit in figure 2.3 which has no resistive element.

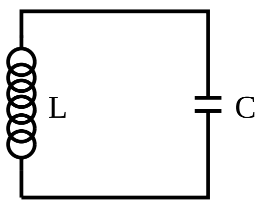


Figure 2.3: LC circuit.

Kirchoff's voltage law applied to the loop is

$$V_L + V_C = 0. \tag{2.16}$$

Substituting our previous expressions for V_L and V_C gives

$$L\frac{dI}{dt} + \frac{Q}{C} = 0. \tag{2.17}$$

Using $I = dQ/dt$ gives

$$L\frac{d^2Q}{dt^2} + \frac{Q}{C} = 0. \tag{2.18}$$

The circuit equation is second-order in Q and one possible solution is

$$Q(t) = Q_0 \cos(\omega t + \phi), \tag{2.19}$$

where $Q(t = 0) = Q_0$ is the initial charge on the capacitor and ϕ is an arbitrary phase constant. Considering the cases of $Q_0 = Q_{\max}$, gives $\phi = 0$. The angular frequency ω is totally determined by the other parameters of the circuit

$$\omega^2 = 1/(LC) \tag{2.20}$$

and $\omega_r \equiv 1/\sqrt{LC}$ is the natural or resonance frequency of the circuit.

We can also solve for the current and voltage across the capacitor

$$\begin{aligned}
Q(t) &= Q_0 \cos(\omega_r t), && (2.21)\\
I(t) &= \frac{dQ}{dt} = -Q_0\omega_r \sin(\omega_r t), && (2.22)\\
&= -I_0 \sin(\omega_r t) = I_0 \cos(\omega_r t + \pi/2), \quad \text{and} && (2.23)\\
V(t) &= \frac{Q(t)}{C} = \frac{Q_0}{C}\cos(\omega_r t) = V_0 \cos(\omega_r t). && (2.24)
\end{aligned}$$

Notice that unlike the transient current and voltage responses of the RC and RL circuits, the LC circuit oscillates. The energy in the circuit is shared back and forth between the inductor and capacitor.

2.2.4 RCL Circuit

Lets now consider the case of all three passive circuit elements in series, as in figure 2.4.

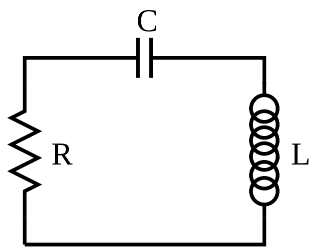


Figure 2.4: RCL circuit.

Applying Kirchoff's law around the loop and using $I = dQ/dt$ gives

$$\begin{aligned}
L\frac{dI}{dt} + RI + \frac{Q}{C} &= 0 \quad \text{and} && (2.25)\\
L\frac{d^2Q}{dt^2} + R\frac{dQ}{dt} + \frac{Q}{C} &= 0. && (2.26)
\end{aligned}$$

The solution will not only depend on the initial conditions but also the relative values of R, C and L.

There are three possible solutions:

1. under damped ($R^2 < 4L/C$): $Ae^{-t/\tau}\cos(\omega t + \phi)$,
2. over damped ($R^2 > 4L/C$): $A_1 e^{-t/\tau_1} + A_2 e^{-t/\tau_2}$, and
3. critically damped ($R^2 = 4L/C$): $(A_1 + A_2 t)e^{-t/\tau}$.

RCL circuits have a variety of properties, especially when driven by sinusoidal sources, which will not be investigate here. My aim is simply to expose you to the area and get on to more interesting topics. Driven oscillating systems also appear in other areas of physics and hopefully you will encounter them there. The detailed considerations lead to discussions on resonance and quality-factor Q.

2.3 Sinusoidal Sources and Complex Impedance

We now consider current and voltage sources with time average values of zero. We will use periodic signals but the observation time could well be less than one period. Periodic signals are also useful in the sense that arbitrary signals can usually be expanded in terms of a Fourier series of periodic signals. Lets start with

$$v(t) = V_0\cos(\omega t + \phi_V) \quad \text{and} \tag{2.27}$$
$$i(t) = I_0\cos(\omega t + \phi_I). \tag{2.28}$$

Notice that I have now switched to lowercase symbols. Lowercase is generally used for AC quantities while uppercase is reserved for DC values.

Now is the time to get into complex notation since it will make our discussion easier and is encounter often in electronics. The above voltage and current signals can be written

$$\vec{v}(t) = V_0 e^{j(\omega t + \phi_V)} \quad \text{and} \tag{2.29}$$
$$\vec{i}(t) = I_0 e^{j(\omega t + \phi_I)}. \tag{2.30}$$

To be cleaver we will defined one EMF in the circuit to have $\phi = 0$. In other words, we will pick $t = 0$ to be at the peak of one signal. The vector notation is used to remind us that complex numbers can be considered as vectors in the complex plane. Although not so common in physics, in electronics we refer to these vectors as phasors. Hence you should now review complex notation.

The presence of sinusoidal $\vec{v}(t)$ or $\vec{i}(t)$ in circuits will result in a inhomogeneous differential equation with a time-dependent source term. The solution will contain sinusoidal terms with the source frequency.

The extension of Ohm's law to AC circuits can be written as

$$\vec{v}(\omega, t) = \mathbf{Z}(\omega)\vec{i}(\omega, t), \tag{2.31}$$

where ω is the source frequency. $\mathbf{Z}$ is a generalized resistance refereed to as the impedance.

We can cancel out the common time dependent factors to obtain

$$\vec{v}(\omega) = \mathbf{Z}(\omega)\vec{i}(\omega) \tag{2.32}$$

and hence you see the power of the complex notation. For a physically quantity we take the amplitude of the real signal

$$|\vec{v}(\omega)| = |\mathbf{Z}(\omega)||\vec{i}(\omega)|. \tag{2.33}$$

We will now examine each circuit element in turn with a voltage source to deduce its impedance.

2.3.1 Resistive Impedance

Kirchoff's voltage law for a voltage source and resistor is

$$\vec{v}(t) - R\vec{i}(t) = 0. \tag{2.34}$$

Trying the solutions

$$\vec{i}(t) = \vec{i}e^{j\omega t} \quad \text{and} \quad \vec{v}(t) = \vec{v}e^{j\omega t} \tag{2.35}$$

lead to

$$\vec{v} = R\vec{i} \quad \Rightarrow \quad \mathbf{Z}_R = R. \tag{2.36}$$

The impedance is equal to the resistance, as expected.

2.3.2 Capacitive Impedance

Kirchoff's voltage law for a voltage source and capacitor is

$$\vec{v}(t) - \frac{q(t)}{C} = 0. \tag{2.37}$$

Or

$$\frac{d\vec{v}(t)}{dt} - \frac{\vec{i}(t)}{C} = 0. \tag{2.38}$$

Solving this equation gives

$$j\omega\vec{v} = \frac{\vec{i}}{C} \quad \Rightarrow \quad \mathbf{Z}_C = \frac{1}{j\omega C} \tag{2.39}$$

For DC circuits $\omega = 0$ and hence $\mathbf{Z}_C \to \infty$. The capacitor acts like an open circuit (infinite resistance) in a DC circuit.

2.3.3 Inductive Impedance

Kirchoff's voltage law for a voltage source and inductor is

$$\vec{v}(t) - L\frac{d\vec{i}(t)}{dt} = 0. \tag{2.40}$$

Solving this equation gives

$$\vec{v} = j\omega L\vec{i} \quad \Rightarrow \quad \mathbf{Z}_L = j\omega L. \tag{2.41}$$

For DC circuits $\omega = 0$ and hence $\mathbf{Z}_L = 0$. There is no voltage drop across an inductor in DC (zero resistance).

2.3.4 Combined Impedances

We now know the impedance for each of our passive circuit elements:

$$\mathbf{Z}_R = R; \quad \mathbf{Z}_L = j\omega L; \quad \mathbf{Z}_C = -j/(\omega C). \tag{2.42}$$

The equivalent impedance of a circuit can be obtained by using the following rules for combining impedances.
In series

$$\mathbf{Z}_{\mathrm{eq}} = \sum_i \mathbf{Z}_i. \tag{2.43}$$

In parallel

$$\mathbf{Z}_{\mathrm{eq}} = \frac{\prod_i \mathbf{Z}_i}{\sum_i \prod_{j\neq i} \mathbf{Z}_j}. \tag{2.44}$$

Appealing to the complex notation we can write

$$\mathbf{Z}_{\mathrm{eq}} = R + jX(\omega), \tag{2.45}$$

where R is the resistance and X is called the reactance (always a function of ω).
For a series combination of R, L and C

$$\begin{aligned} \mathbf{Z}_{\mathrm{eq}} &= R + j\omega L + \frac{1}{j\omega C}, && (2.46)\\ &= R + j\left(\omega L - \frac{1}{\omega C}\right). && (2.47) \end{aligned}$$

$(\omega L - 1/\omega C) = 0$ gives a special frequency, $\omega = 1/\sqrt{LC}$.

> **Example:** *An inductor and capacitor in parallel form the tank circuit shown in figure 2.5.*

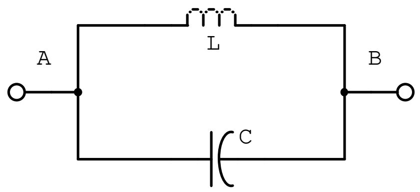


Figure 2.5: Tank circuit with inductor and capacitor.

1. *Determine an expression for the impedance of this circuit.*
   The impedance of an inductor and a capacitor are

$$Z_L = j\omega L; \quad Z_C = \frac{1}{j\omega C}. \tag{2.48}$$

   Combining the impedances in parallel gives

$$\begin{aligned} Z &= \left(\frac{1}{\sum_i Z_i}\right)^{-1} = \left(\frac{1}{Z_L} + \frac{1}{Z_C}\right)^{-1} = \frac{Z_C Z_L}{Z_C + Z_L} && (2.49)\\ &= \frac{(1/(j\omega C))(j\omega L)}{1/(j\omega C) + j\omega L} = \frac{-jL/C}{\omega L - 1/(\omega C)} && (2.50)\\ &= \frac{j\omega L}{1 - \omega^2 LC}. && (2.51) \end{aligned}$$

2. *What is the impedance when $\omega = 1/\sqrt{LC}$?*
   Substituting this value for ω into the above result gives

$$\begin{aligned} Z &= \frac{j\frac{L}{\sqrt{LC}}}{1 - \frac{LC}{LC}} = \frac{j\sqrt{\frac{L}{C}}}{0} && (2.52)\\ &\to \infty. && (2.53) \end{aligned}$$

Example: *The tank circuit schematic shown in figure 2.6 results from the use of a real inductor.*

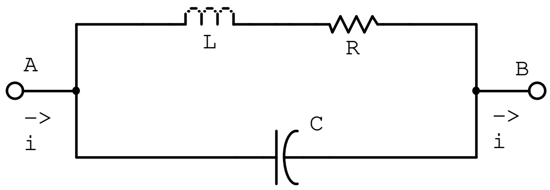


Figure 2.6: Tank circuit with real inductor

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1. *Find an expression for the impedance of this circuit.*
   The impedance of an inductor, capacitor and resistor are

$$Z_L = j\omega L; \quad Z_C = \frac{1}{j\omega C}; \quad Z_R = R. \tag{2.54}$$

The resistor and inductor are in series and this combination of impedance is in parallel with the capacitor. Combining the impedances gives

$$\begin{aligned} Z &= \left(\frac{1}{\sum_i Z_i}\right)^{-1} = \left(\frac{1}{Z_L + Z_R} + \frac{1}{Z_C}\right) = \frac{Z_C(Z_L + Z_R)}{Z_C + Z_R + Z_L} && (2.55) \\ &= \frac{(1/(j\omega C))(j\omega L + R)}{1/(j\omega C) + R + j\omega L} && (2.56) \\ &= \frac{L/C - jR/(\omega C)}{R + j(\omega L - 1/(\omega C))}. && (2.57) \end{aligned}$$

2. *If $L = 1H$, $R = 100\Omega$, and $C = 0.01\mu F$, what is the impedance when $\omega = 1/\sqrt{LC}$?*
   Substituting this value for ω into the above equation gives

$$Z = \frac{L/C - jR\sqrt{L/C}}{R + j(\sqrt{L/C} - \sqrt{L/C})} = \frac{L}{RC} - j\sqrt{\frac{L}{C}} \tag{2.58}$$

Substituting the numerical values for the inductance, resistance and capacitance gives

$$\begin{aligned} Z &= \frac{1}{10^2 \times 10^{-8}} - j\sqrt{\frac{1}{10^{-8}}} && (2.59) \\ &= (10^6 - j10^4)\Omega && (2.60) \\ &= (100 - j) \times 10^4\Omega. && (2.61) \end{aligned}$$

3. *What is the impedance when ω is very small?*

$$\begin{aligned} Z &\approx \frac{-jR/\omega C}{-j1/\omega C} && (2.62) \\ &= R. && (2.63) \end{aligned}$$

4. *What is the phase angle between the voltage $\vec{v}_{AB}$ and $\vec{i}$ at resonance and at $\omega = 10^5$ rad/s?*
   Rationalizing the denominator of the impedance gives

$$Z = \frac{[L/C - jR/(\omega C)][R - j(\omega L - 1/(\omega C))]}{R^2 + [\omega L - 1/(\omega C)]^2}. \tag{2.64}$$

Taking the real and imaginary components gives

$$\mathcal{R}e[Z] = \frac{RL/C - R/(\omega C)[\omega L - 1/(\omega C)]}{R^2 + [\omega L - 1/(\omega C)]^2} \tag{2.65}$$

$$= \frac{R/(C^2\omega^2)}{R^2 + [\omega L - 1/(\omega C)]^2}, \tag{2.66}$$

$$\mathcal{I}m[Z] = \frac{-R^2/(\omega C) - L/C[\omega L - 1/(\omega C)]}{R^2 + [\omega L - 1/(\omega C)]^2}. \tag{2.67}$$

The inverse tangent of the ratio of the imaginary to real parts is

$$\phi = \tan^{-1}\left[\frac{-R^2/(\omega C) - \omega L^2/C + L/(\omega C^2)}{R/(C^2\omega^2)}\right] \tag{2.68}$$

$$= \tan^{-1}\left[\frac{-R^2 C\omega - CL^2\omega^3 + L\omega}{R}\right] \tag{2.69}$$

$$= \tan^{-1}\left[\frac{\omega}{R}(L - CR^2 - CL^2\omega^2)\right]. \tag{2.70}$$

There is a resonance at $\omega L - 1/(\omega C) = 0 \Rightarrow \omega = 1/\sqrt{LC}$
and hence

$$\phi_{res} = \tan^{-1}\left[\frac{1}{R\sqrt{LC}}(L - CR^2 - L)\right] \tag{2.71}$$

$$= \tan^{-1}\left(-R\sqrt{\frac{C}{L}}\right) \tag{2.72}$$

$$= -\tan^{-1}\left(R\sqrt{\frac{C}{L}}\right). \tag{2.73}$$

At $\omega = 10^5$ *rad/s.*

$$\phi = \tan^{-1}\left[\frac{10^5}{10^2}\left(1 - 10^{-8}(10^2)^2 - 10^{-8}(1)^2(10^5)^2\right)\right] \tag{2.74}$$

$$= \tan^{-1}[10^3(1 - 10^{-4} - 10^4)] \tag{2.75}$$

$$\approx \tan^{-1}(-10^7) \tag{2.76}$$

$$\approx -\pi/2. \tag{2.77}$$

2.4 Resonance and the Transfer Function

Lets now consider putting a sinusoidal source in our series RCL circuit and consider the voltage across one of the circuit elements. The resistor for example in figure 2.7

Applying Ohm's law $\vec{v}(j\omega) = R\vec{i}(j\omega)$ across the resistor gives (cf. a voltage divider)

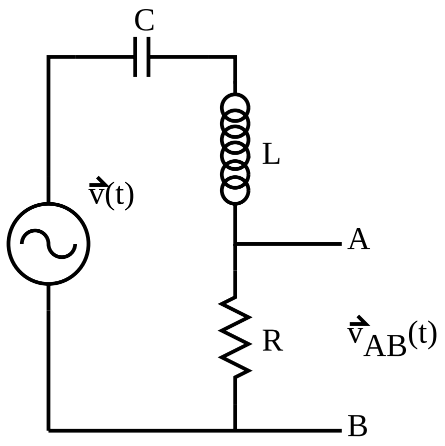


Figure 2.7: Driven series RCL circuit.

$$\vec{v}_{AB}(j\omega) = \frac{\mathbf{Z}_R}{\mathbf{Z}_R + \mathbf{Z}_L + \mathbf{Z}_C}\vec{v}(j\omega), \tag{2.78}$$

$$= \frac{R}{R + j(\omega L - 1/(\omega C))}\vec{v}(j\omega), \tag{2.79}$$

$$\equiv \mathbf{H}(j\omega)\vec{v}(j\omega), \tag{2.80}$$

where $\mathbf{H}(j\omega)$ is known as the transfer function in the frequency domain. We have changed independent variables from ω to $j\omega$ for convenience.

We define

$$\mathbf{H}(j\omega) = \frac{\vec{v}_{AB}(j\omega)}{\vec{v}(j\omega)} = \frac{R}{R + j(\omega L - 1/(\omega C))}. \tag{2.81}$$

$\mathbf{H}(j\omega)$ contains all the information needed to characterize the circuit. In exponential form

$$\mathbf{H}(j\omega) = H(j\omega)e^{j\phi(\omega)}, \tag{2.82}$$

where

$$H(j\omega) = \frac{R}{\sqrt{R^2 + (\omega L - 1/(\omega C))^2}} \tag{2.83}$$

and

$$\phi(\omega) = \tan^{-1}\left(\frac{1/(\omega C) - \omega L}{R}\right). \tag{2.84}$$

$\mathbf{H}(j\omega)$ has a maximum (resonance) given by $\omega L - 1/(\omega C) = 0$. Or $\omega = 1/\sqrt{LC} \equiv \omega_r$ is the resonant frequency.

Example: *Consider the series LCR circuit (figure 2.8) driven by a voltage phasor $\vec{v}(t) = v_0 \exp(j\omega t)$.*

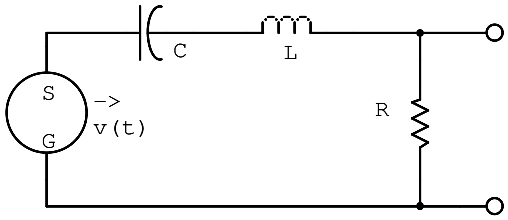


Figure 2.8: Driven series LCR circuit.

1. *At an angular frequency such that $\omega L = 2R$ and $1/(\omega C) = R$, write the current phasor in terms of $\vec{v}(t)$ and R.*
   $v(t)$ is given by $v(t) = Zi(t)$, where $Z = Z_C + Z_L + Z_R = \frac{1}{j\omega C} + j\omega L + R$. At $\omega L = 2R$ and $\frac{1}{\omega C} = R$

$$\begin{aligned} \Rightarrow Z &= \frac{R}{j} + 2jR + R = R(1+j) && (2.85) \\ &= \sqrt{2}Re^{j\pi/4}. && (2.86) \end{aligned}$$

   Therefore

$$\begin{aligned} i(t) &= \frac{v(t)}{Z} = \frac{v_0 e^{j\omega t}}{\sqrt{2}Re^{j\pi/4}} && (2.87) \\ \vec{i}(t) &= \frac{v_0}{\sqrt{2}R} e^{j(\omega t - \pi/4)}. && (2.88) \end{aligned}$$

2. *At the instant when $\vec{v}(t)$ is exactly real, calculate the three phasors representing the voltage developed across the R, C, and L circuit elements.*
   $v(t)$ is real at $t = 0$. Thus

$$\begin{aligned} v_R &= Ri(t=0) && (2.89) \\ &= \frac{v_0}{\sqrt{2}} e^{-j\pi/4} && (2.90) \end{aligned}$$

   And

$$\begin{aligned} v_L &= Z_L i(0) = j\omega L i(0) = j2R\frac{v_0}{\sqrt{2}R} e^{-j\pi/4} && (2.91) \\ &= \sqrt{2}v_0 e^{j\pi/2} e^{-j\pi/4} && (2.92) \\ &= \sqrt{2}v_0 e^{j\pi/4} && (2.93) \end{aligned}$$

   Also

$$\begin{aligned} v_C &= Z_C i(0) = \frac{i(0)}{j\omega C} = \frac{e^{-j\pi/2}}{1/R}\frac{v_0}{\sqrt{2}R} e^{-j\pi/4} && (2.94) \\ &= \frac{v_0}{\sqrt{2}} e^{-j3\pi/4}. && (2.95) \end{aligned}$$

3. *Algebraically and with a sketch on the complex plane, show that the complex voltage sum around the closed loop is zero.*
   The three voltage phasors are

$$v_R = \frac{v_0}{\sqrt{2}} e^{-j\pi/4} = \frac{v_0}{\sqrt{2}}[\cos(-\pi/4) + j\sin(-\pi/4)] \quad (2.96)$$

$$= \frac{v_0}{2}(1-j) \quad (2.97)$$

$$v_L = \sqrt{2} v_0 e^{j\pi/4} = \sqrt{2} v_0 [\cos(\pi/4) + j\sin(\pi/4)] \quad (2.98)$$

$$= v_0(1+j) \quad (2.99)$$

$$v_C = \frac{v_0}{\sqrt{2}} e^{-j3\pi/4} = \frac{v_0}{\sqrt{2}}[\cos(-3\pi/4) + j\sin(-3\pi/4)] \quad (2.100)$$

$$= -\frac{v_0}{2}(1+j) \quad (2.101)$$

Around the closed loop $\sum_i v_i = v - v_R - v_L - v_C$. *If this expression is zero at* $t = 0$ *it will be zero for all time. Therefore* $v_0 - \frac{v_0}{2}(1-j) - v_0(1+j) + \frac{v_0}{2}(1+j) = 0$.

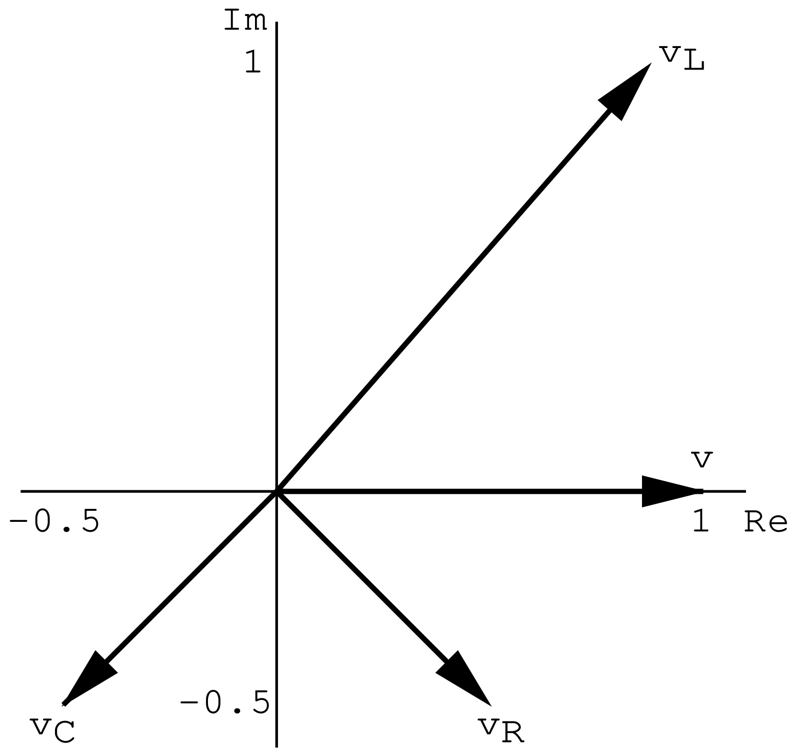


Figure 2.9: Complex voltage sum around the closed loop of the driven LCR circuit.

Example: *Sketch simplified versions of the circuit shown in figure 2.10 that would be valid at:*

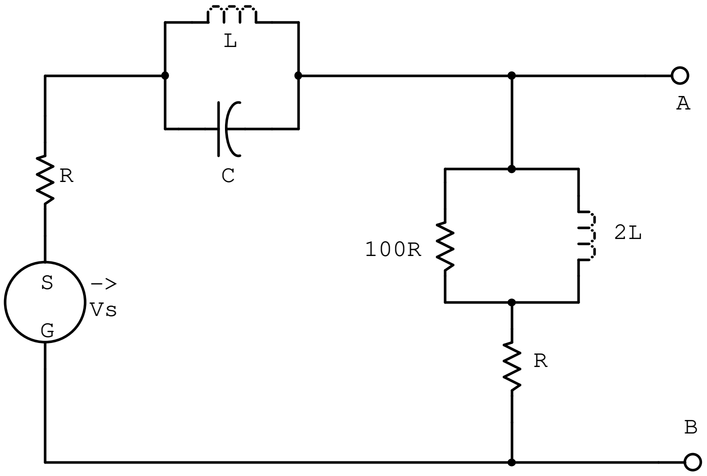


Figure 2.10: Example LCR circuit.

1. $\omega = 0$;
   $\omega = 0 \Rightarrow Z_C \to \infty; Z_L \to 0.$

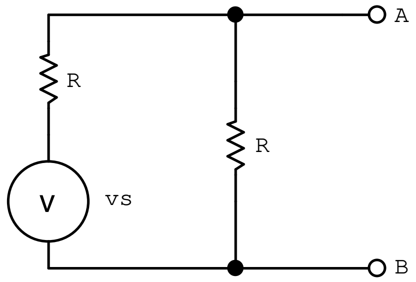


Figure 2.11: Example circuit for $\omega = 0$.

2. *very low frequencies but not* $\omega = 0$;
   When ω *is small* $(\omega \neq 0)$ C *and* L *are in parallel and*

$$\begin{aligned} Z_{eq} &= \frac{Z_C Z_L}{Z_C + Z_L} = \frac{[1/(j\omega C)](j\omega L)}{1/(j\omega C) + j\omega L} = \frac{jL/C}{1/(\omega C) - \omega L} & (2.102) \\ &\approx j\omega L = Z_L. & (2.103) \end{aligned}$$

$2L$ *and* $100R$ *in parallel gives*

$$Z_{eq} = \frac{Z_R Z_L}{Z_R + Z_L} = \frac{(100R)(j\omega 2L)}{100R + j\omega 2L}. \tag{2.104}$$

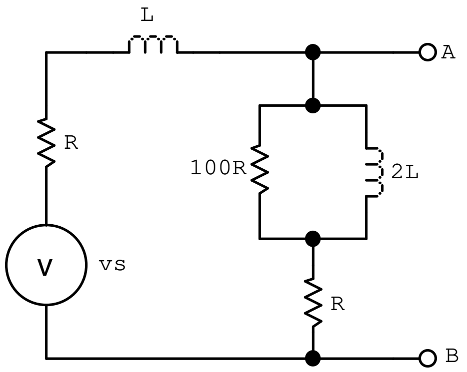


Figure 2.12: Example circuit for very low frequencies but not $\omega = 0$.

3. *very high frequencies but not* $\omega = \infty$*;*
   ω *large* $(\omega \neq \infty)$.

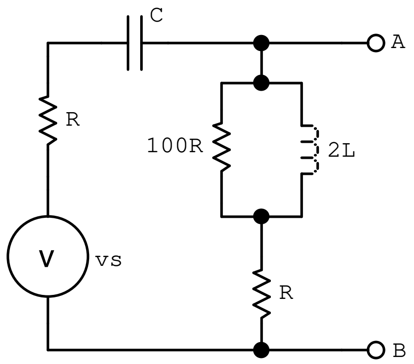


Figure 2.13: Example circuit for very high frequencies but not $\omega = \infty$.

4. $\omega = \infty$.
   $\omega = \infty \Rightarrow Z_C = 1/j\omega C \to 0; Z_L = j\omega L \to \infty$ *(note:* $100R + R \approx 100R$*).*

Example: *For the circuit shown in figure 2.15 plot* $|\mathbf{Z}_{eq}|$ *as a function of frequency over the range* $\omega = 1$ *rad/s to* $\omega = 10^6$ *rad/s.*
The equivalent impedance for the three components in parallel is

$$Z_{eq} = \frac{Z_R Z_L Z_C}{Z_L Z_R + Z_L Z_C + Z_C Z_R} \tag{2.105}$$

$$= \frac{(R)(j\omega L)(1/j\omega C)}{(j\omega L)(R) + (j\omega L)(\frac{1}{j\omega C}) + (\frac{1}{j\omega C})(R)} \tag{2.106}$$

$$= \frac{RL/C}{\frac{L}{C} + jR(\omega L - \frac{1}{\omega C})} \tag{2.107}$$

$$|Z_{eq}| = \frac{RL/C}{\sqrt{(\frac{L}{C})^2 + R^2(\omega L - \frac{1}{\omega C})^2}}. \tag{2.108}$$

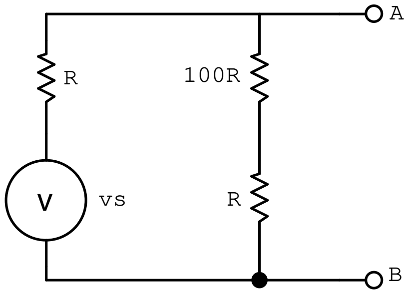


Figure 2.14: Example circuit for $\omega = \infty$.

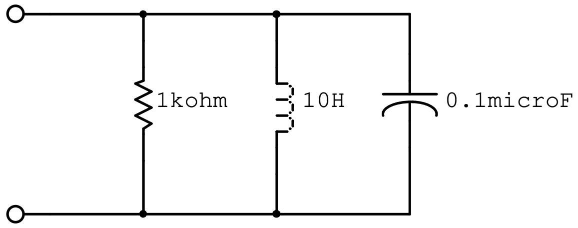


Figure 2.15: Example circuit with components in parallel.

Plugging in the numerical values gives

$$|Z_{eq}| = \frac{10^3 \times 10 \times 10^7}{\sqrt{(\frac{10}{10^{-7}})^2 + 10^6(10\omega - \frac{10^7}{\omega})^2}} \tag{2.109}$$

$$= \frac{10^{11}}{\sqrt{10^{16} + 10^8(\omega - \frac{10^6}{\omega})^2}} \tag{2.110}$$

$$= \frac{10^7}{\sqrt{10^8 + (\omega - \frac{10^6}{\omega})^2}}. \tag{2.111}$$

A table of values and its plot follows.

Table 2.1: Numerical values for example circuit.

$\omega(rad/s)$	$\log_{10}\omega$	$\lvert Z_{eq}\rvert$	$\log_{10}\lvert Z_{eq}\rvert$
$1(10^0)$	0	10^1	1
10^1	1	10^2	2
10^2	2	$1/\sqrt{2}\times 10^3$	2.8
10^3	3	10^3	3
10^4	4	$1/\sqrt{2}\times 10^3$	2.8
10^5	5	10^2	2
10^6	6	10^1	1

2.5 Four-Terminal Networks

Our previous resonance circuit is an example of a two-terminal network. A source is present but no load. A four-terminal network also has the source removed. The four-terminal network can be described by a transfer function. A generic four-terminal network is shown in figure 2.17. Such a circuit can be analyzed simply by considering it as a voltage divider. In general

$$\mathbf{H} = \frac{\mathbf{Z}_2}{\mathbf{Z}_1 + \mathbf{Z}_2}. \tag{2.112}$$

2.6 Single-Term Approximations of H

A circuit with a few components quickly leads to a complicated expression for the transfer function. It is often sufficient, and of course, easier to work with approximations to the transfer function.

Let $\mathbf{H}$ be the ratio of two polynomials

$$\mathbf{H}(j\omega) = \frac{\mathbf{P}(j\omega)}{\mathbf{Q}(j\omega)}, \tag{2.113}$$

where

$$\mathbf{P}(j\omega) = \sum_{i=0}^{N} P_i(j\omega)^i \quad \text{and} \quad \mathbf{Q}(j\omega) = \sum_{k=0}^{M} Q_k(j\omega)^k. \tag{2.114}$$

If one term dominates in each polynomial

$$\mathbf{P}(j\omega) \approx P_n(j\omega)^n \quad \text{and} \quad \mathbf{Q}(j\omega) \approx Q_m(j\omega)^m. \tag{2.115}$$

Thus

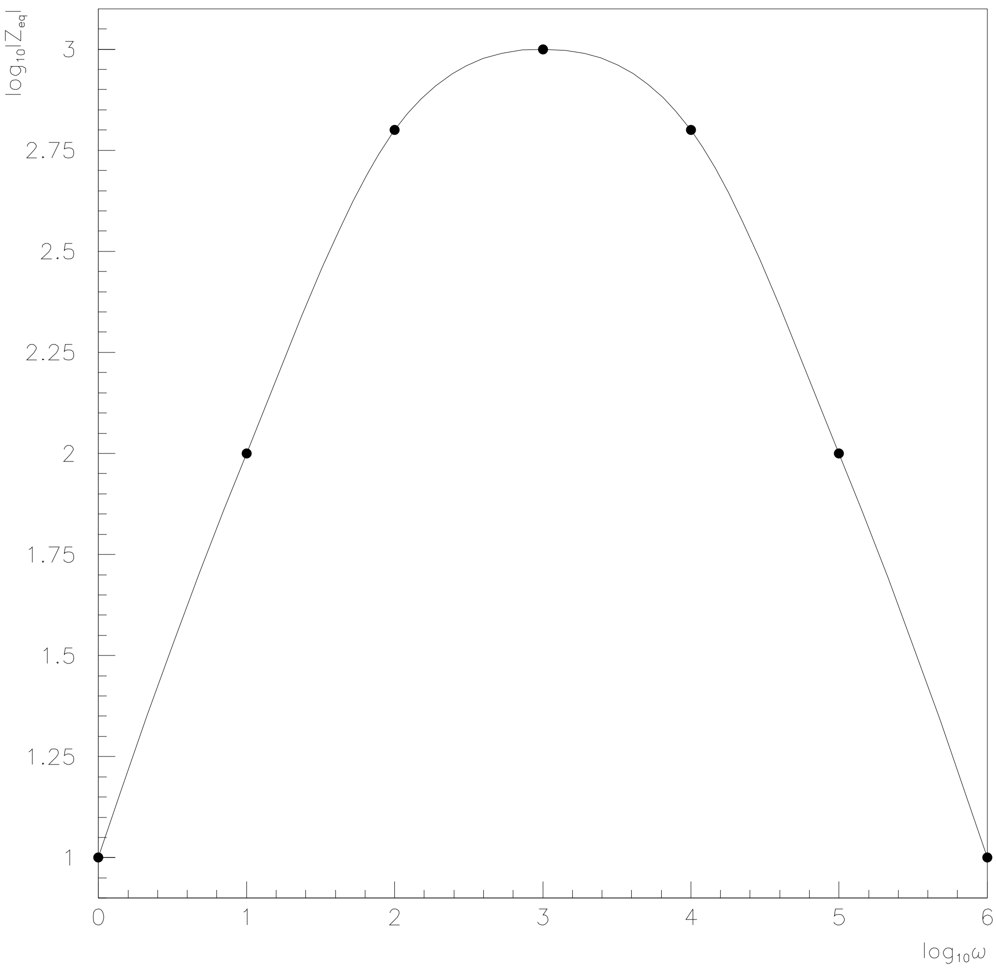


Figure 2.16: Plot of $|\mathbf{Z}_e q|$ for example circuit.

$$\mathbf{H}(j\omega) = \frac{P_n(j\omega)^n}{Q_m(j\omega)^m} = \frac{P_n}{Q_m}(j\omega)^{(n-m)} = \frac{P_n}{Q_m}\omega^{(n-m)}e^{j(n-m)\pi/2} \quad \text{and} \tag{2.116}$$

$$|\mathbf{H}(j\omega)| = \left|\frac{P_n}{Q_m}\right|\omega^{(n-m)}. \tag{2.117}$$

We define $\log \equiv \log_{10}$ and plot

$$\log|\mathbf{H}(j\omega)| = \log\left|\frac{P_n}{Q_m}\right| + (n-m)\log\omega, \tag{2.118}$$

which is a straight line on a log-log plot with integer slope.

As an example, consider our RCL circuit:

$$\mathbf{H}(j\omega) \quad = \quad \frac{R}{R + j(\omega L - 1/(\omega C))} \tag{2.119}$$

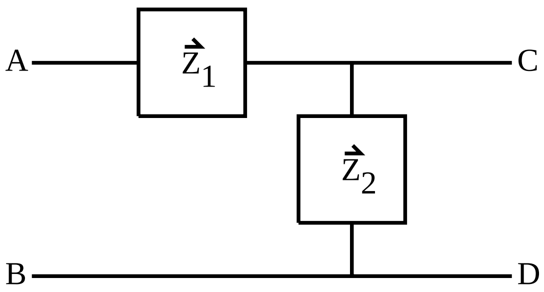


Figure 2.17: Generic four-terminal network.

$$= \frac{1}{1 + j(\omega L/R - 1/(\omega RC))} \tag{2.120}$$

$$= \frac{1}{1 + j(\omega Q/\omega_r - \omega_r Q/\omega)} \tag{2.121}$$

$$= \frac{1}{1 + jQ(\omega/\omega_r)(1 - (\omega_r/\omega)^2)}, \tag{2.122}$$

where $\omega_r = \frac{1}{\sqrt{LC}}$ and $Q = \frac{\omega_r L}{R}$.
At low frequencies $\omega/\omega_r \to 0$ and

$$\mathbf{H}_{\rm low}(j\omega) = \frac{1}{1 - jQ\omega_r/\omega} \approx \frac{j\omega}{Q\omega_r} \tag{2.123}$$

$$|\mathbf{H}_{\rm low}(j\omega)| = \frac{\omega}{Q\omega_r}. \tag{2.124}$$

On a log-log plot

$$\log|\mathbf{H}_{\rm low}(j\omega)| = \log 1/(Q\omega_r) + \log\omega, \tag{2.125}$$

which has a slope of +1. At high frequencies $\omega_r/\omega \to 0$ and

$$\mathbf{H}_{\rm high}(j\omega) = \frac{1}{1 + jQ\omega/\omega_r} \approx \frac{-j\omega_r}{Q\omega} \tag{2.126}$$

$$|\mathbf{H}_{\rm high}(j\omega)| = \frac{\omega_r}{Q\omega}. \tag{2.127}$$

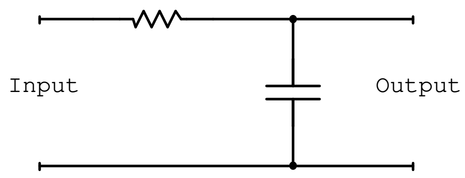
On a log-log plot

$$\log|\mathbf{H}_{\rm high}(j\omega)| = \log\omega_r/Q - \log\omega, \tag{2.128}$$

which has a slope of -1.

2.7 Problems

1. Consider the following circuit:



   (a) What is the impedance of the circuit?

   (b) For the input $\vec{v}(t) = \vec{v}\exp(j\omega t)$, what current flows through the capacitor?

   (c) What is the phase difference between the voltage across the capacitor (V_C) and the applied voltage? Be sure to specify whether V_C leads or follows the applied voltage.

2. Consider a circuit consisting of an inductor (L), a capacitor (C) and a resistor (R) in series with a voltage source $v(t) = v_0 e^{j\omega t}$. Let $\omega = 1$ krad/s, $R = 1$ kΩ, $L = 1$ H and $C = 10$ μF.

   (a) What is the magnitude of the current through the circuit?

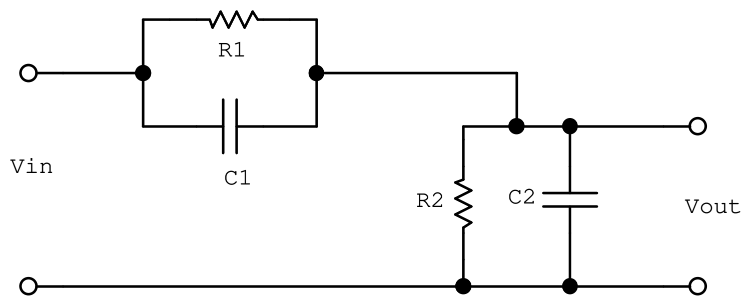
   (b) What is the phase of the current relative to the source voltage?

   (c) What is the magnitude of the voltage drop across the inductor?

   (d) What is the phase of the voltage across the inductor relative to the source voltage?

   (e) At what frequency is the amplitude of the voltage across the resistor largest?

3. Derive the transfer function for the four-terminal network shown below.



Chapter 3

Filter Circuits

Lets now apply our knowledge of AC circuits to some practical applications. We will first look at some simple passive filters (skipping active filters) and then an amplifier model. Again we will rely on complex variables.

3.1 Filters and Amplifiers

Simplistically, filters and amplifiers can be considered as four-terminal networks described by a transfer function as follows:

$$\vec{v}_{out}(j\omega) = \mathbf{H}(j\omega)\vec{v}_{in}(j\omega). \tag{3.1}$$

Figure 3.1 shows some ideal transfer functions. If $\mathbf{H}(j\omega) = \mathbf{H} \equiv A$ is a real constant than we call the network an ideal amplifier. If $\mathbf{H}(j\omega) = \Theta(j(\omega - \omega_0))$ is a heavyside step function we refer to the circuit as an ideal low-pass filter, and if $\mathbf{H}(j\omega) = 1 - \Theta(j(\omega - \omega_0))$ an ideal high-pass filter.

3.2 Log-Log Plots and Decibels

A log-log plot of a circuit's transfer function can be a useful qualitative tool to allow us to understand most of the important features of filter and amplifier circuits. The commonly used decibel unit will be defined. Although unappealing to the physicist this unit is still in wide spread use in electronics. Lets start.

If P_1 and P_2 are two powers, we define the decibel as

$$\text{dB} \equiv 10\log\frac{P_2}{P_1} = 10\log\frac{V_2^2}{V_1^2} = 20\log\left|\frac{V_2}{V_1}\right|. \tag{3.2}$$

where we have used $P \propto V^2$.

The decibel is a property of the network and not the signals. Hence we can make use of any convenient signals in defining decibel. If two constant equal amplitude sources, $|\vec{v}_{in}(j\omega_1)| = |\vec{v}_{in}(j\omega_2)|$, are applied to a four-terminal network we may write

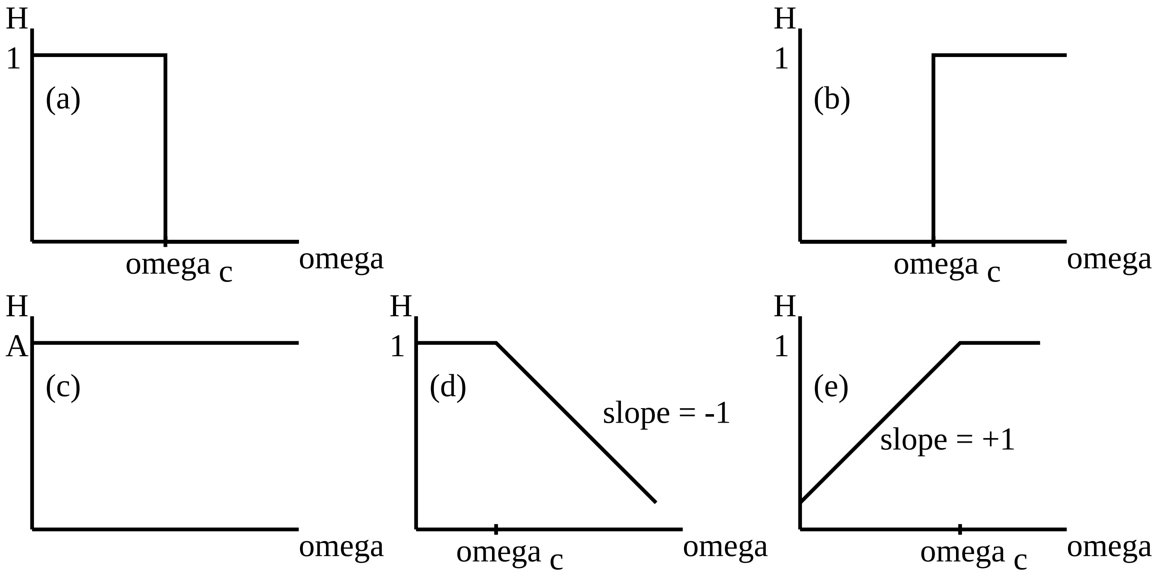


Figure 3.1: a) Ideal low-pass filter, b) ideal high-pass filter, c) Ideal amplifier, d) low-pass filter and e) high-pass filter.

$$|\vec{v}_{out}(j\omega_1)| = |\mathbf{H}(j\omega_1)||v_{in}(j\omega_1)|, \tag{3.3}$$

$$|\vec{v}_{out}(j\omega_2)| = |\mathbf{H}(j\omega_2)||v_{in}(j\omega_2)| \quad \text{and} \tag{3.4}$$

$$\left|\frac{\vec{v}_2}{\vec{v}_1}\right|_{out} = \frac{\mathbf{H}(j\omega_2)}{\mathbf{H}(j\omega_1)}. \tag{3.5}$$

Therefore

$$\mathrm{dB} = 20\log\left|\frac{\mathbf{H}(j\omega_2)}{\mathbf{H}(j\omega_1)}\right|. \tag{3.6}$$

Using the approximation procedure of a previous lecture

$$|\mathbf{H}(j\omega)| \propto |(j\omega)^n| = \omega^n, \tag{3.7}$$

and if ω_1 and ω_2 are not too different

$$\mathrm{dB} = 20\log\left(\frac{\omega_2^n}{\omega_1^n}\right) = n20\log\left(\frac{\omega_2}{\omega_1}\right). \tag{3.8}$$

By definition an octave interval is when $\omega_2 = 2\omega_1$ and hence

$$\mathrm{dB/octave} = 20n\log_{10}(2) = 6.02n \approx 6n. \tag{3.9}$$

Likewise for a decade interval $\omega_2 = 10\omega_1$ and

$$\text{dB/decade} = 20n\log_{10}(10) = 20n. \tag{3.10}$$

3.3 Passive RC Filters

We will now use our passive circuit elements to design some filter circuits. Inductors are not very good devices and hence we will concentrate on the use of resistors and capacitors.

3.3.1 Low-Pass Filter

Figure 3.2 shows one possible low-pass filter. The circuit is essentially a frequency-sensitive voltage divider. At high frequencies the output behaves as if it is shorted while at low frequencies the output appears as an open circuit.

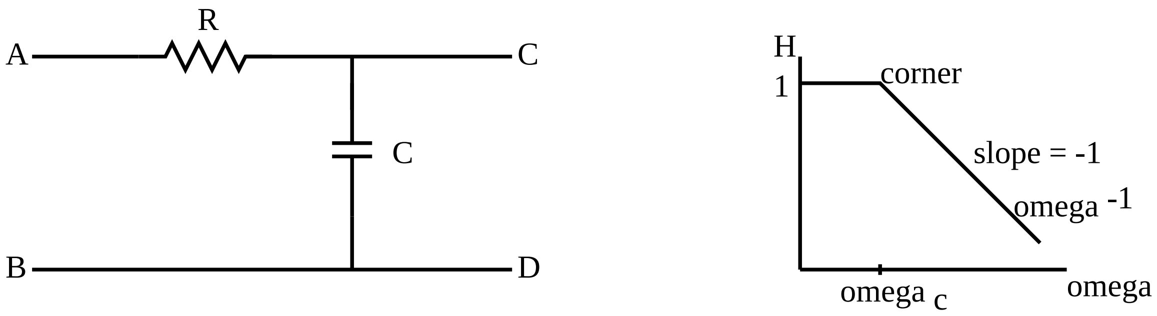


Figure 3.2: RC low-pass filter

Mathematically we have

$$\vec{v}_{out} = \frac{1/(j\omega C)}{R + 1/(j\omega C)}\vec{v}_{in}. \tag{3.11}$$

$$\mathbf{H}(j\omega) \equiv \frac{\vec{v}_{out}}{\vec{v}_{in}} = \frac{1}{1 + j\omega RC}. \tag{3.12}$$

The approximations are

$$\omega \to 0 \Rightarrow \mathbf{H}(j\omega) \to \mathbf{H}_{\text{low}} = 1. \tag{3.13}$$

$$\omega \to \infty \Rightarrow \mathbf{H}(j\omega) \to \mathbf{H}_{\text{high}} = \frac{1}{j\omega RC}, \tag{3.14}$$

$$|\mathbf{H}_{\text{high}}| = \frac{1}{RC}\omega^{-1}. \tag{3.15}$$

At the corner

$$|\mathbf{H}_{\rm high}| = |\mathbf{H}_{\rm low}| \Rightarrow \frac{1}{RC\omega_c} = 1. \tag{3.16}$$

Therefore

$$\omega_c = \frac{1}{RC} \tag{3.17}$$

is the *corner frequency* of the filter. At the corner frequency

$$\mathbf{H}(j\omega_c) = \frac{1}{1 + j\omega_c RC} = \frac{1}{1+j} = \frac{1-j}{2}, \tag{3.18}$$

$$|\mathbf{H}(j\omega_c)| = \frac{1}{\sqrt{2}}. \tag{3.19}$$

We say that the output is down by $1/\sqrt{2}$ at the corner frequency.

3.3.2 Approximate integrater

The low-pass filter acts as an approximate integrater at high frequencies. Assume

$$\vec{v}_{\rm in}(t) = \vec{v}e^{j\omega t} \tag{3.20}$$

and integrate to obtain

$$\vec{v}_{out} = \vec{v}\int e^{j\omega t}dt = \frac{\vec{v}}{j\omega}e^{j\omega t} + \vec{v}_{out}(t=0). \tag{3.21}$$

The DC term is unimportant and may be dropped to obtain

$$\vec{v}_{\rm out} = \frac{1}{j\omega}\vec{v}_{\rm in}. \tag{3.22}$$

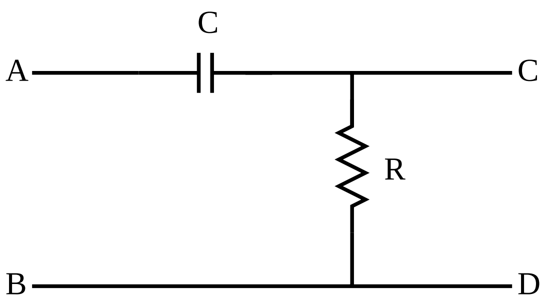
We define

$$\mathbf{H}_{\rm integrate} \equiv \frac{\vec{v}_{out}}{\vec{v}_{in}} = \frac{1}{j\omega}. \tag{3.23}$$

For a low-pass filter at high frequencies $\omega \gg \omega_c$ and

$$\mathbf{H}_{\rm high} = \frac{1}{j\omega RC} = \frac{1}{RC}\mathbf{H}_{\rm integrate}. \tag{3.24}$$

Thus the low-pass filter integrates at high frequencies but also attenuates the signal by $1/(RC)$.



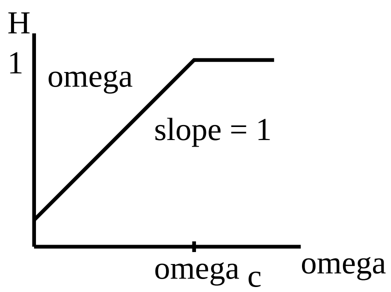


Figure 3.3: RC high-pass filter.

3.3.3 High-Pass Filter

Figure 3.3 shows one possible high-pass filter. Mathematically we can write

$$\mathbf{H}(j\omega) = \frac{R}{R + 1/(j\omega C)} = \frac{j\omega RC}{1 + j\omega RC}. \tag{3.25}$$

At low and high frequencies

$$\mathbf{H}_{\text{low}} = j\omega RC \quad \text{and} \quad \mathbf{H}_{\text{high}} = 1. \tag{3.26}$$

At the corner frequency $\omega = \omega_c$ we have

$$|\mathbf{H}_{\text{low}}| = |\mathbf{H}_{\text{high}}| \tag{3.27}$$

and therefore

$$\omega_c = \frac{1}{RC}. \tag{3.28}$$

3.3.4 Approximate Differentiator

A high-pass filter acts as an approximate differentiator at low frequencies. Consider

$$\vec{v}_{\text{in}} = \vec{v} e^{j\omega t} \tag{3.29}$$

and differentiate to obtain

$$\vec{v}_{\text{out}} = \frac{d\vec{v}_{\text{in}}}{dt} = j\omega \vec{v} e^{j\omega t} = j\omega \vec{v}_{\text{in}}. \tag{3.30}$$

We define

$$\mathbf{H}_{\text{differentiate}} = j\omega = \frac{1}{RC}\mathbf{H}_{\text{low}}. \tag{3.31}$$

Again the filter attenuates the signal by $1/(RC)$.

Example: *Write the transfer function* $\mathbf{H}(j\omega)$ *for the network in figure 3.4 and from it find:*

1. *the corner frequency,*

   Treating the circuit like a voltage divider, the transfer function is

$$\mathbf{H}(j\omega) = \frac{1/(j\omega C)}{1/(j\omega C) + j\omega L} = \frac{1}{1 - \omega^2 LC}. \tag{3.32}$$

   For $\omega \approx 0 \Rightarrow \mathbf{H}(j\omega) \rightarrow 1$.
   For ω *large* $\Rightarrow \mathbf{H}(j\omega) \rightarrow \frac{-1}{\omega^2 LC}$.
   For the corner frequency $1 = \frac{-1}{\omega_C^2 LC} \Rightarrow \omega_C^2 = \frac{-1}{LC}$.
   Therefore

$$\omega_C = \frac{j}{\sqrt{LC}} = \frac{j}{(1 \times 10^{-6})^{1/2}} = j \times 10^3 rad/s. \tag{3.33}$$

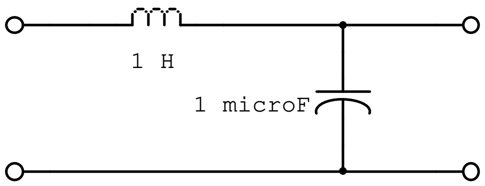


Figure 3.4: Four-terminal network without resistance.

2. *the value of* $|\mathbf{H}|$ *at the corner frequency.*

   At the corner frequency

$$\mathbf{H}(j\omega_C) = \frac{1}{1+1} = \frac{1}{2}. \tag{3.34}$$

3. *How many degrees of phase shift are introduced by this network just below and just above the corner frequency?*

   Since $\mathbf{H}(j\omega)$ *is always real there is no phase shift.*

3.4 Complex Frequencies and the s-Plane

We will now consider s-plane techniques. Not because we will use them, but more to understand some of the common electronics terminology.

We can enhance the usefulness of the transfer function $\mathbf{H}(j\omega)$ by transforming to a complex frequency. Define the complex variable $\vec{s}$ such that

$$\vec{s} = \sigma + j\omega, \tag{3.35}$$

where σ is an inverse time constant.

Our exponential function now becomes

$$f(t) = \mathbf{A}e^{\vec{s}t} = \mathbf{A}e^{\sigma t}e^{j\omega t} \tag{3.36}$$

and we have a rich set of cases

$$\begin{array}{llll}
\omega = 0, & \sigma > 0, & e^{\sigma t} & \text{exponential growth,} \\
\omega = 0, & \sigma < 0, & e^{-|\sigma| t} & \text{decay,} \\
\omega \neq 0, & \sigma = 0, & e^{j\omega t} & \text{oscillation,} \\
\omega \neq 0, & \sigma > 0, & e^{\sigma}e^{j\omega t} & \text{growing oscillations} \quad \text{and} \\
\omega \neq 0, & \sigma < 0, & e^{-|\sigma|}e^{j\omega t} & \text{decaying oscillations.}
\end{array}$$

So we can not only describe oscillatory behavior but transient responses as well.

3.4.1 Poles and Zeros of H

As before, consider expanding the transfer function as the ratio of two polynomials

$$\mathbf{H}(\vec{s}) = \frac{\mathbf{P}(\vec{s})}{\mathbf{Q}(\vec{s})}. \tag{3.37}$$

If $\vec{a}_n$ are the roots of $\mathbf{P}(\vec{s})$ and $\vec{b}_m$ are the roots of $\mathbf{Q}(\vec{s})$ we can write

$$\mathbf{H}(\vec{s}) = A\frac{(\vec{s} - \vec{a}_1)(\vec{s}_1 - \vec{a}_2)\ldots(\vec{s} - \vec{a}_n)}{(\vec{s} - \vec{b}_1)(\vec{s} - \vec{b}_2)\ldots(\vec{s} - \vec{b}_m)}, \tag{3.38}$$

where A is a real constant, $\vec{a}_n$ are zeros of $\mathbf{H}$ and $\vec{b}_m$ are poles (infinity) of $\mathbf{H}$. Knowledge of $\vec{a}_n$ and $\vec{b}_m$ determine $\mathbf{H}(\vec{s})$ everywhere.

Lets now look at our two filter circuits. For a low-pass filter

$$\mathbf{H}(\vec{s}) = \frac{1}{1 + \vec{s}RC} = \frac{1/(RC)}{\vec{s} + 1/(RC)} \tag{3.39}$$

and the filter has one pole at $-1/(RC)$. For a high-pass filter

$$\mathbf{H}(\vec{s}) = \frac{\vec{s}RC}{1 + \vec{s}RC} = \frac{\vec{s}}{\vec{s} + 1/(RC)} \tag{3.40}$$

and it has one pole at $-1/(RC)$ and one zero at 0. We refer to these two types of filters as single-pole filters.

There is a general rule that there must be at least as many reactive elements as poles. Based on the location of the poles we are able to deduce the general response properties of the filter. We will not do this here.

Example: *If a transfer function has poles at (-1,2) and (-1,-2) and a zero at (0,0),*

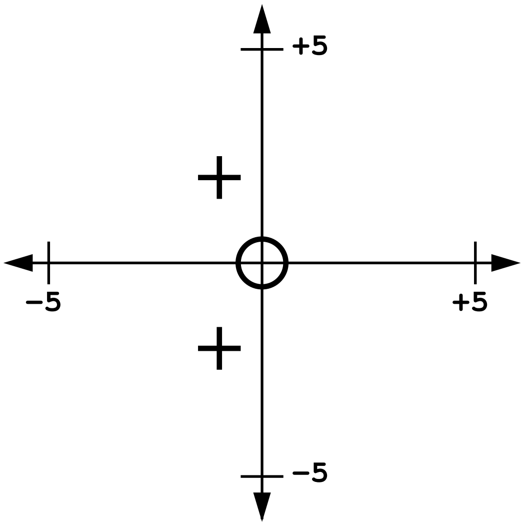


Figure 3.5: Poles and zeros in the complex plane.

1. *sketch* $|\mathbf{H}(j\omega)|$ *on the interval* $0 \leq \omega < 10$.
   The transfer function is given by

$$\mathbf{H}(\vec{s}) = \frac{|\vec{s} - (0,0)|}{|\vec{s} - (-1,2)||\vec{s} - (-1,-2)|} = \frac{\omega}{|\vec{s} - \vec{p}_1||\vec{s} - \vec{p}_2|} \tag{3.41}$$

   Plugging in values for ω *gives the table 3.1.*

Table 3.1: Numerical values of the transfer function.

ω	$\lvert\vec{s} - (-1,2)\rvert$	$\lvert\vec{s} - (-1,-2)\rvert$	$\mathbf{H}(\vec{s})$
0	2.24	2.24	0
1	1.41	3.16	0.224
2	1.00	4.12	0.485
3	1.41	5.10	0.416
4	2.24	6.08	0.294
5	3.16	7.07	0.224
6	4.12	8.06	0.180
7	5.10	9.06	0.152
8	6.08	10.05	0.131
9	7.07	11.05	0.115
10	8.06	12.04	0.103

2. *If* $|\mathbf{H}(j10)| = 1$, *what is the approximate value of* $|\mathbf{H}|$ *at its highest point?*
   If $|\mathbf{H}(j10)| = 1$ *then* H_{max} *at* $\omega = 2$ *is* $H_{max} = 0.485$. *Therefore*

$$\frac{0.485}{0.103} \times 1 = 4.7. \tag{3.42}$$

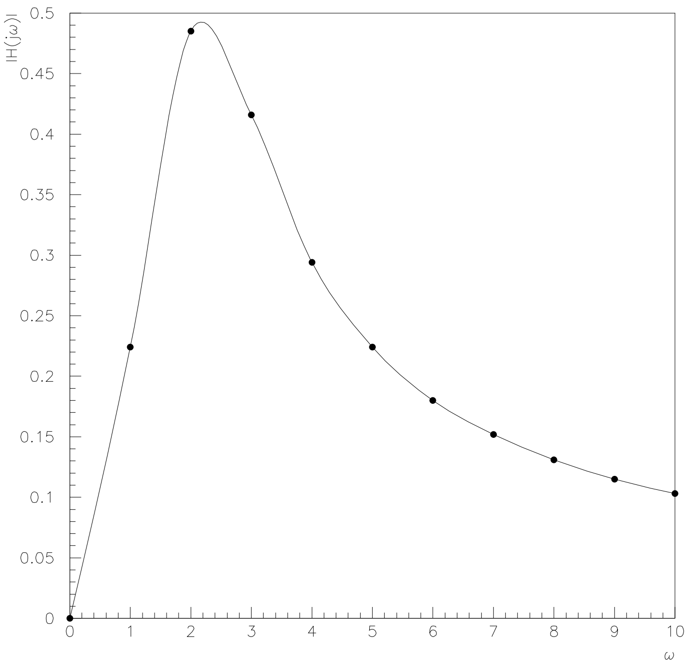


Figure 3.6: The transfer function from the table above.

3.5 Sequential RC Filters

Single-pole filters are rather limited (6 dB/octave slope). For better band-pass and band-reject filters we require more poles and zeros and thus more reactive circuit elements. A simple solution is to connect two or more single-pole RC filters in sequence. If filter $\mathbf{H}_2$ draws no current from filter $\mathbf{H}_1$, the transfer function for the combined filter is

$$\mathbf{H} = \mathbf{H}_1\mathbf{H}_2 (= \mathbf{H}_2\mathbf{H}_1). \tag{3.43}$$

One way to do this is to choose a large impedance for $\mathbf{H}_2$. Hence $\mathbf{H}$ has more poles and zeros than $\mathbf{H}_1$ or $\mathbf{H}_2$.

The corner frequency for a high-pass filter is $\omega_H = 1/(RC)$ and the transfer function may be write as

$$\mathbf{H}_{\text{high}} = \frac{j\omega RC}{1 + j\omega RC} = \frac{j\omega/\omega_H}{1 + j\omega/\omega_H}. \tag{3.44}$$

For a low-pass filter the corner frequency is $\omega_L = 1/(RC)$ and

$$\mathbf{H}_{\text{low}} = \frac{1}{1 + j\omega RC} = \frac{1}{1 + j\omega/\omega_L}. \tag{3.45}$$

We may build a two-section low-pass filter by requiring $R_2 > R_1$ and $1/C_2 > 1/C_1$, as shown in figure 3.7, so that

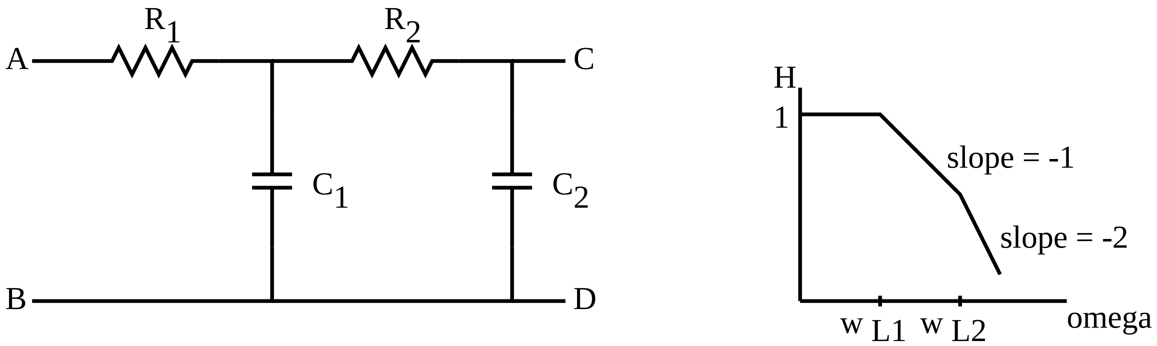


Figure 3.7: Two-section low-pass filter.

$$\mathbf{H}_{\text{low}} = \frac{1}{(1+j\omega/\omega_{L_1})(1+j\omega/\omega_{L_2})}. \tag{3.46}$$

A special case occurs when $R_1C_1 = R_2C_2 \Rightarrow \omega_{L_1} = \omega_{L_2}$ and we obtain one corner frequency but the slope of the filter is ω^{-2}.

Similarly for a two-section high-pass filter. A band-pass filter can be built from one low-pass filter and one high-pass filter, as shown in figure 3.8. The order of the filter sections does not matter as long as the impedance rule is obeyed.

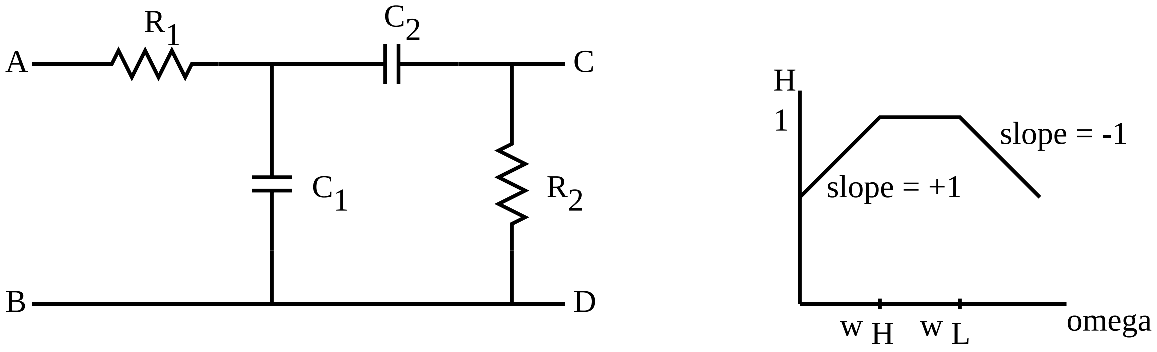


Figure 3.8: Band-pass filter.

$$\mathbf{H}_{\text{pass}} = \frac{j\omega/\omega_H}{(1+j\omega/\omega_H)(1+j\omega/\omega_L)}. \tag{3.47}$$

If $\omega_L \leq \omega_H$ we have only two straight regions and the band-pass frequency range degenerated to zero.

Example: *Show that the magnitude of the transfer function*

$$\mathbf{H}_{\text{pass}} = \frac{j\omega/\omega_H}{(1+j\omega/\omega_H)(1+j\omega/\omega_L)} \tag{3.48}$$

falls off −6 dB/octave at both the low- and high-frequency extremes.
For small ω *(ie.* $\omega \ll \omega_H$ *and* $\omega \ll \omega_L$*)* $\mathbf{H} \approx j\omega/\omega_H$; $|\mathbf{H}(j\omega)| = \omega/\omega_H$;
$\log_{10} H = \log_{10}\omega + C$.
Thus

$$\frac{d(\log_{10}|\mathbf{H}|)}{d(\log_{10}\omega)} = 1 \Rightarrow 6db/octave. \tag{3.49}$$

For large ω *(ie.* $\omega \gg \omega_H$ *and* $\omega \gg \omega_L$*)* $\mathbf{H} \approx -j\omega_L/\omega$; $|\mathbf{H}(j\omega)| = \omega_L/\omega$;
$|\mathbf{H}(j\omega)| = -\log_{10}\omega + C$.
And thus

$$\frac{d(\log_{10}|\mathbf{H}|)}{d(\log_{10}\omega)} = -1 \Rightarrow -6dB/octave. \tag{3.50}$$

3.6 Passive RCL Filters

Sequential RC filters always have real poles and hence smooth rounded corners. To improve these filters we introduce an inductor (which is good for high frequencies).

3.6.1 Series RCL Circuit

Consider the previous RCL circuits as shown in figure 3.9. Each has a low-frequency and high-frequency approximation. Considering the band-reject filter (figure 3.6d) we obtain for the transfer function

$$\mathbf{H} = \frac{1/(j\omega C) + j\omega L}{R + 1/(j\omega C) + j\omega L} \tag{3.51}$$

$$= \frac{1-\omega^2 LC}{(1-\omega^2 LC) + j\omega RC}. \tag{3.52}$$

The approximations are:

$$\omega \to 0; \quad \mathbf{H} \to \mathbf{H}_{\mathrm{L}} = 1 \quad \text{and} \tag{3.53}$$

$$\omega \to \infty; \quad \mathbf{H} \to \mathbf{H}_{\mathrm{H}} = 1. \tag{3.54}$$

We notice a zero in the transfer function at $\omega_0 = 1/\sqrt{LC}$. In the low-medium frequency range

$$\omega < \omega_0; \quad \mathbf{H} \to \mathbf{H}_{\mathrm{LM}} = \frac{1}{j\omega RC} \propto \omega^{-1}, \tag{3.55}$$

for high-medium frequencies

$$\omega > \omega_0; \quad \mathbf{H} \to \mathbf{H}_{\mathrm{HM}} = \frac{-\omega^2 LC}{j\omega RC} = \frac{j\omega L}{R} \propto \omega^{+1}. \tag{3.56}$$

Solving for the corner frequencies we have

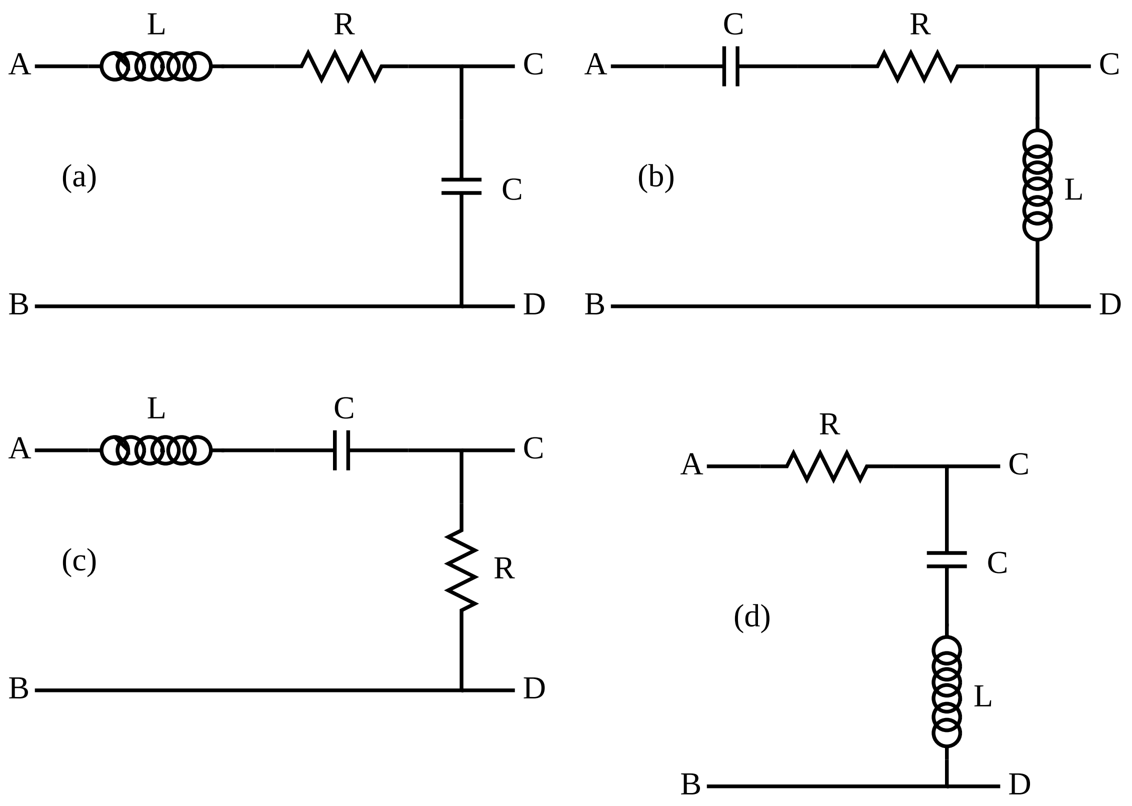


Figure 3.9: LCR filters: a) low-pass, b) high-pass, c) band-pass and d) band-reject.

$$1 = 1/|j\omega RC| \quad \Rightarrow \quad \omega_1 = 1/(RC), \tag{3.57}$$

$$1 = |\omega L/R| \quad \Rightarrow \quad \omega_2 = R/L \quad \text{and} \tag{3.58}$$

$$\omega_0 = 1/\sqrt{LC} = \sqrt{\omega_1\omega_2}. \tag{3.59}$$

Example: *Sketch $|\mathbf{H}(j\omega)|$ for the LCR circuit shown in figure 3.10 for the two conditions $R = 0.5\sqrt{L/C}$ and $R = 2\sqrt{L/C}$. In each case, determine the values of $|\mathbf{H}|$ at $\omega = 0$, ∞, and ω_c, and label these points on the sketches.*
The transfer function is

$$\mathbf{H}(j\omega) = \frac{R + j\omega L}{R + j\omega L + \frac{1}{j\omega C}}. \tag{3.60}$$

For ω small

$$\mathbf{H}(j\omega) \approx \frac{R}{1/(j\omega C)} = -j\omega RC \tag{3.61}$$

$$|\mathbf{H}(j\omega)| = \omega RC. \tag{3.62}$$

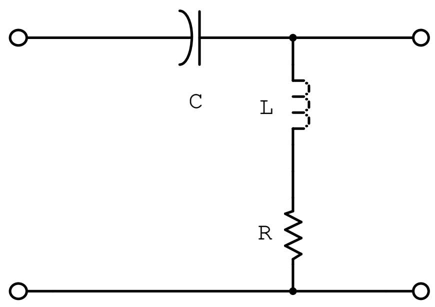


Figure 3.10: LCR circuit with two components across the output.

For ω *large* $\mathbf{H}(j\omega) = 1$.
For the corner frequency $1 = \omega_C RC \rightarrow \omega_C = 1/(RC)$.
For $R = 0.5\sqrt{L/C} = \frac{1}{2}\sqrt{\frac{L}{C}}$,
$H_{low} = \frac{\omega}{2}\sqrt{LC}; \omega_C = \frac{2}{\sqrt{LC}}$.

$$\begin{aligned}
\mathbf{H}(j\omega_C) &= \frac{R + 2j\sqrt{L/C}}{R + 2j\sqrt{L/C} - j/2\sqrt{L/C}} = \frac{R + 4jR}{R + 4jR - jR} && (3.63)\\
&= \frac{1 + 4j}{1 + 3j} = \frac{(1 + 4j)(1 - 3j)}{1 + 9} = \frac{13 + j}{10} && (3.64)\\
&= \sqrt{\frac{13^2 + 1^2}{10^2}} = \sqrt{\frac{170}{10}} = 1.30. && (3.65)
\end{aligned}$$

For $R = 2\sqrt{L/C}$,
$H_{low} = 2\omega\sqrt{LC}; \omega_C = \frac{1}{2\sqrt{LC}}$

$$\begin{aligned}
\mathbf{H}(j\omega_C) &= \frac{R + j/2\sqrt{L/C}}{R + j/2\sqrt{L/C} - 2j\sqrt{L/C}} = \frac{2 + j/2}{2 + j/2 - 2j} && (3.66)\\
&= \frac{4 + j}{4 - 3j} = \frac{(4 + j)(4 + 3j)}{16 + 9} = \frac{13 + 16j}{25} && (3.67)\\
&= \sqrt{\frac{13^2 + 16^2}{25^2}} = \frac{\sqrt{425}}{25} = 0.825. && (3.68)
\end{aligned}$$

Figure 3.11 is a sketch of the transfer functions.

Example:

1. *Write an expression for the transfer function of the circuit shown in figure 3.12.*

$$Z_{CL} = \frac{(1/(j\omega C))(j\omega L)}{1/(j\omega C) + j\omega L} = \frac{j\omega L}{1 - \omega^2 CL} \quad (3.69)$$

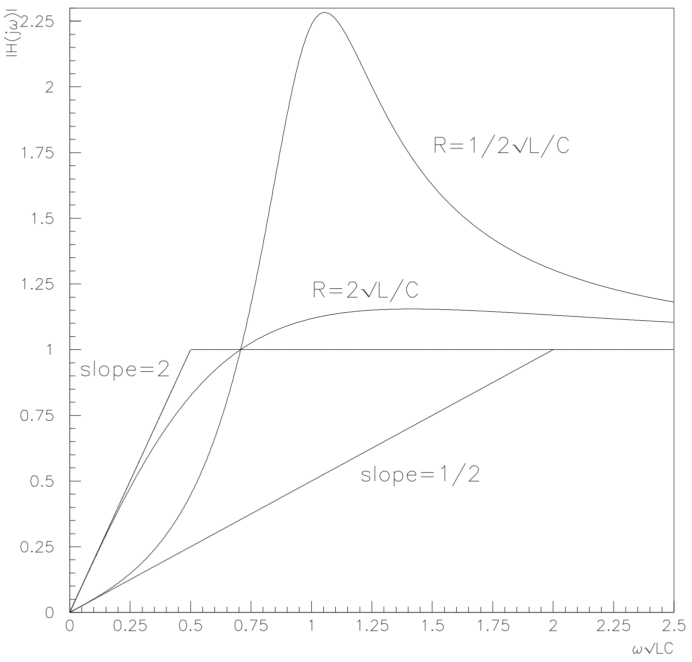


Figure 3.11: Sketch of the transfer functions for the above circuit.

$$\mathbf{H}(j\omega) = \frac{\frac{j\omega L}{1-\omega^2 CL}}{R + \frac{j\omega L}{1-\omega^2 CL}} = \frac{1}{1 - jR/(\omega L)(1-\omega^2 CL)} \tag{3.70}$$

$$= \frac{1}{1 + j(\omega RC - \frac{1}{\omega}\frac{R}{L})}. \tag{3.71}$$

2. *What phase shift is introduced by this filter at very small and very large frequencies?*
   For large ω $\quad \mathbf{H}(j\omega) \approx \frac{1}{j\omega RC} = \frac{-j}{RC}\omega^{-1}$

$$\mathbf{H}_{high} = \frac{1}{RC}\omega^{-1}e^{-j\pi/2} \rightarrow \phi_H = -\frac{\pi}{2}. \tag{3.72}$$

   For small ω $\quad \mathbf{H}(j\omega) \approx \frac{1}{(-j/\omega)(R/L)} = j\omega\frac{L}{R}$

$$\mathbf{H}_{low} = \frac{L}{R}\omega e^{j\pi/2} \rightarrow \phi_L = +\frac{\pi}{2}. \tag{3.73}$$

3. *On a log-log scale, sketch* $|\mathbf{H}(j\omega)|$ *and the phase shift as a function of* ω.
   For the corner frequency $\omega_C^2 RC = \frac{R}{L} \rightarrow \omega_C = \frac{1}{\sqrt{LC}}$.
   $\mathbf{H}(j\omega_C) = 1; \phi_C = 0$.

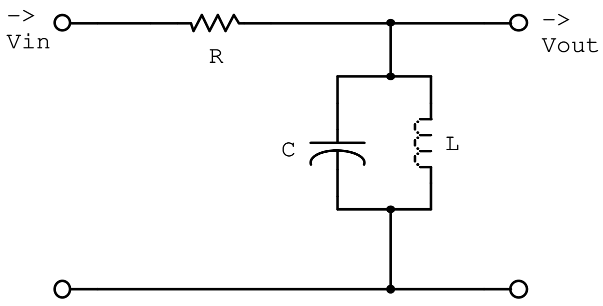


Figure 3.12: Circuit with components in parallel at the output.

3.7 Amplifier Model

Enough for filters. Lets now look at the simple amplifier model in figure 3.14

$$\vec{v}_{\text{out}}(j\omega) = \mathbf{A}(j\omega)\vec{v}_{in}(j\omega), \tag{3.74}$$
$$\vec{v}_{\text{out}}(\vec{s}) = \mathbf{A}(\vec{s})\vec{v}_{in}(\vec{s}). \tag{3.75}$$

Notice that $\vec{v}_{\text{out}}$ is with respect to ground while $\vec{v}_{\text{in}}$ is a voltage difference. For a typical operational amplifier $|\mathbf{H}| \approx 10^6$ at $\omega = 0$. As $\omega \to \infty$, $\mathbf{A}(\omega) < \mathbf{A}(\omega = 0)$ due to internal capacitance, ie. the amplifier behaves like a low-pass filter.

$$\mathbf{A}(\vec{s}) = A_0 \mathbf{H}_{\text{low}}(\vec{s}), \tag{3.76}$$

where $\mathbf{H}_{\text{low}}$ is the transfer function of a low-pass filter.

3.7.1 One-, Two- and Three-Pole Amplifier Models

The simplest amplifier has

$$\mathbf{A}_1(\vec{s}) = \frac{A_0}{1 + \vec{s}/s_a}, \tag{3.77}$$

where s_a is a real positive number (corner frequency). There is a single pole at $-s_a$ on negative real axis. This means that the impulse response will decay exponentially without ringing.

If we cascade multiple (three) single-pole amplifiers together

$$\mathbf{A}_3(\vec{s}) = \frac{A_0}{(1 + \vec{s}/s_a)(1 + \vec{s}/s_b)(1 + \vec{s}/s_c)}. \tag{3.78}$$

There will still be no oscillation to an impulse.

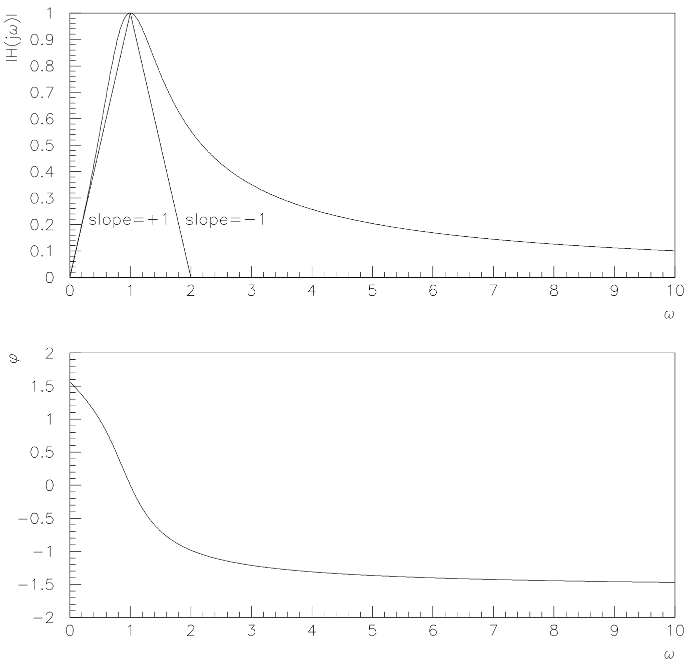


Figure 3.13: Transfer function and phase shift for the above circuit.

3.7.2 Amplifier with Negative Feedback

Feedback is a widely used technique to improve the characteristics of an imperfect amplifier. A generalized amplifier with negative voltage feedback is shown in figure 3.15.

The overall transfer function (closed-loop gain) can be written as

$$\mathbf{H}(\vec{s}) = \frac{\vec{v}_3}{\vec{v}_1}. \tag{3.79}$$

Realizing that

$$\vec{v}_2 = \vec{v}_1 - \vec{v}_4; \quad \vec{v}_2 = \frac{\vec{v}_3}{\mathbf{A}(\vec{s})} \quad \text{and} \quad \vec{v}_4 = \mathbf{F}\vec{v}_3. \tag{3.80}$$

we may write

$$\mathbf{H}(\vec{s}) = \frac{\mathbf{A}}{1 + \mathbf{AF}}. \tag{3.81}$$

If $|\mathbf{AF}| \gg 1 \Rightarrow \mathbf{H}(\vec{s}) = 1/\mathbf{F}$. The transfer function is now independent of the amplifier gain. $\mathbf{F}$ is the transfer function of a stable resistive network which means that $\mathbf{H}$ will also be stable.

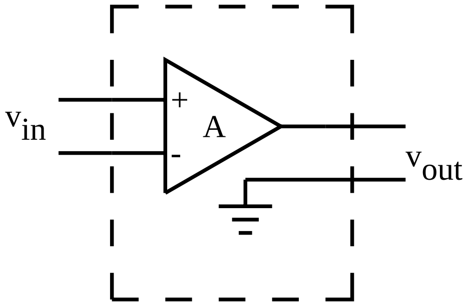


Figure 3.14: A simple amplifier model.

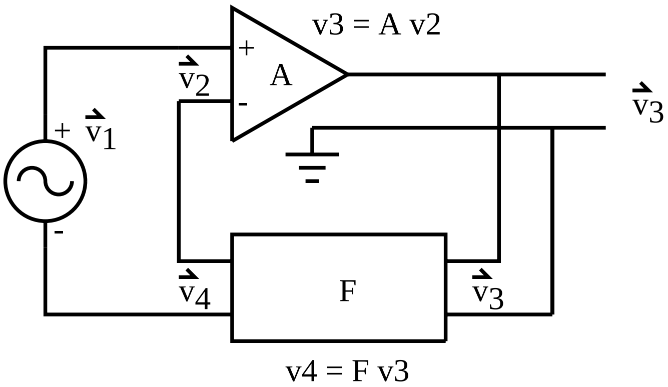
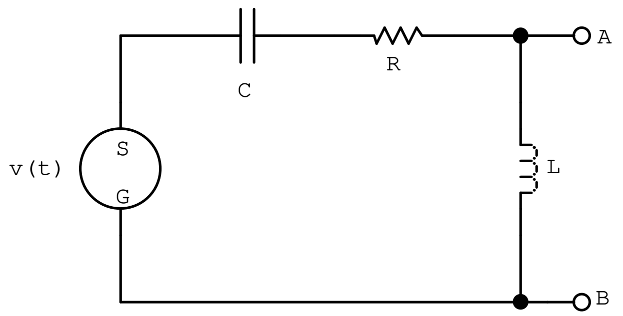


Figure 3.15: Amplifier with negative voltage feedback.

3.8 Problems

1. In the following circuit, the input signal is $\vec{v} = v_0 \exp(j\omega t)$, and the components have been chosen such that $L = R/\omega$ and $C = 3/(\omega R)$. The output is at the terminals AB.



   (a) What is the transfer function $\mathbf{H}(j\omega)$?
   (b) Find the current in the circuit.
   (c) What is the voltage drop across each element of the circuit?
   (d) Show algebraically that at any instant the potential difference around the circuit is zero.
   (e) At time $t = N\pi/\omega$, where $N = 0, 2, 4, ...$ make a sketch showing the voltage across each element in the complex plane and show that the vector sum of the voltage drops is equal to the voltage supplied.
   (f) Write an expression for $|\mathbf{H}(j\omega)|$.
   (g) What is the limit of $|\mathbf{H}(j\omega)|$ as ω goes to zero?
   (h) What is the limit of $|\mathbf{H}(j\omega)|$ as ω goes to infinity?
   (i) What is the corner frequency?
   (j) What is $|\mathbf{H}(j\omega)|$ at the corner frequency?
   (k) Make a sketch showing the characteristics of $|\mathbf{H}(j\omega)|$ on a log-log plot. Label the slope of the curve where possible, the corner frequency, and the value of $|\mathbf{H}(j\omega)|$ at the corner frequency.
   (l) Describe the high and low frequency behavior in dB/octave.

2. (a) Draw a passive LCR low-pass filter and write down the transfer function of your four-terminal network.
   (b) Determine approximations to the transfer function and filter corner frequency(s).
   (c) Write the resonance frequency, $\omega_r = 1/\sqrt{LC}$, in terms of the corner frequency(s).

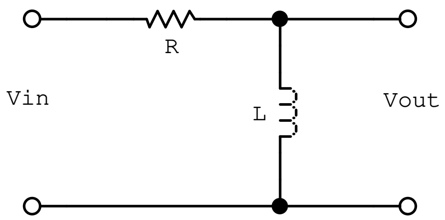
3. Write down the transfer function, $\mathbf{H}(j\omega)$, for the network shown below, and from it find:

(a) the corner frequency(s) and

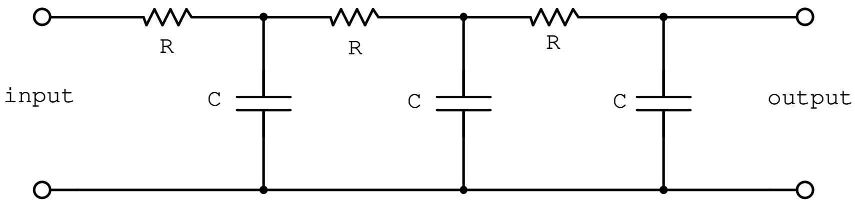
(b) the value(s) of $|\mathbf{H}(j\omega)|$ at the corner frequency(s).

(c) Sketch $|\mathbf{H}(j\omega)|$ and the voltage phase-shift as a function of ω .

(d) What type of filter is this?



4. (a) What is the transfer function for the following circuit?



(b) Describe the frequency response at low and high frequencies?

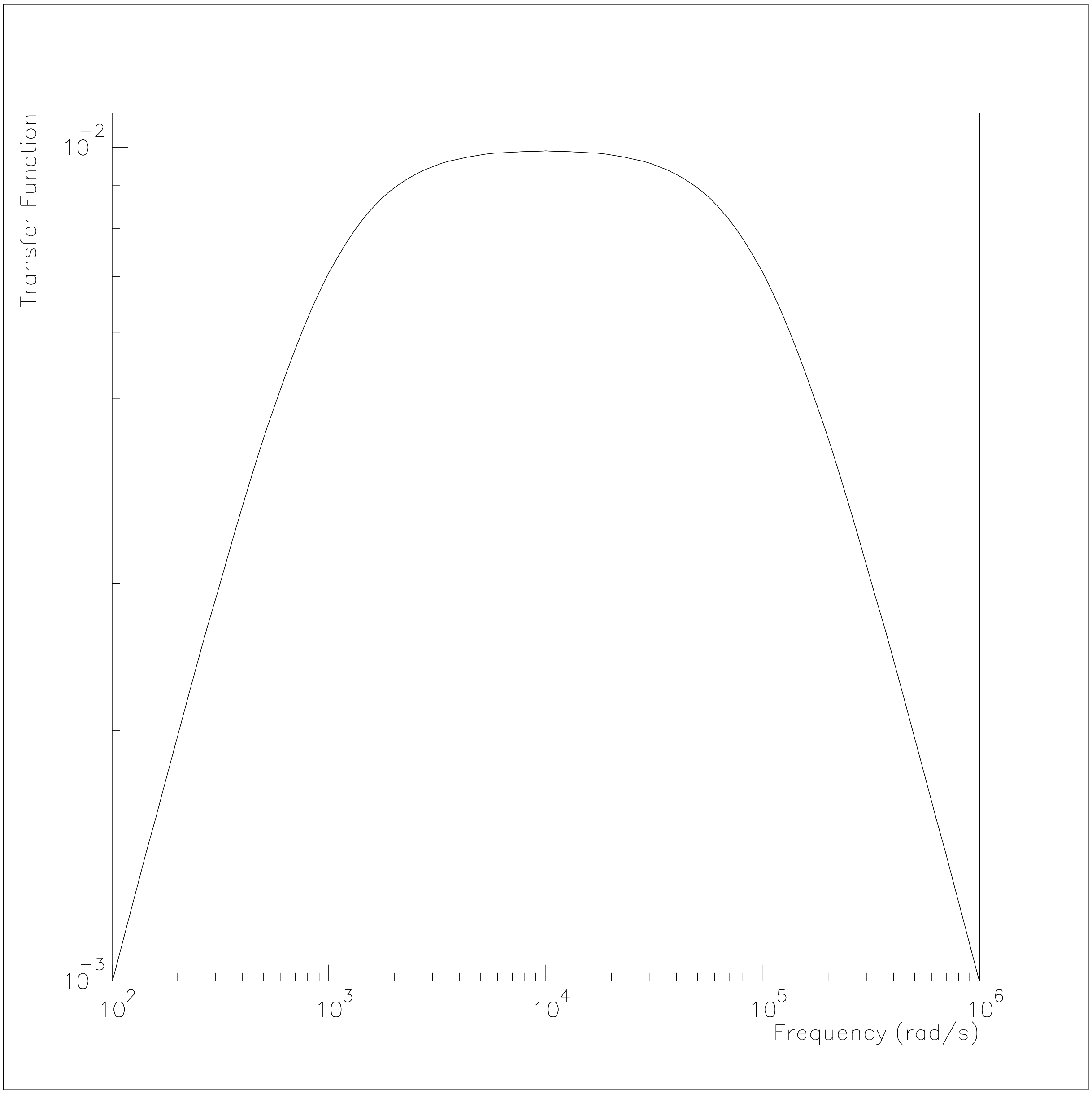
(c) Sketch the magnitude $|\mathbf{H}(j\omega)|$ on a log-log plot. (label slopes, the corner frequency(s), and $|\mathbf{H}(j\omega_C)|$)

(d) What is the signal attenuation for $\omega = 3(RC)^{-1}$.

5. (a) Show that the transfer function of a single-pole RC filter drops by 3 db at the corner frequency. This is often refereed to as the 3 db down-point.

(b) Design a bandpass RC filter with the transfer function shown below. $\omega_1 = 10^3$ rad/s and $\omega_2 = 10^5$ rad/s are the 3 db down-points of the RC filter sections. Choose impedances so that the first section is not much affected by the loading of the second section.

(c) Are ω_1 and ω_2 the 3 db down-points of a bandpass filter?


Transfer Function
10^{-2}
10^{-3}
10^{2}
10^{3}
10^{4}
10^{5}
10^{6}
Frequency (rad/s)

Chapter 4

Diode Circuits

So far we have only considered passive circuit elements. Now we will consider our first reactive circuit element, the diode. Hopefully things will start to get a little more interesting.

Along with the diode there is the transistor, which will be discussed in future lectures. These circuit elements are commonly made from a semiconductor basic material. Semiconductors along with the passive circuit elements are often integrated onto a single electronics chip. If a hundred or so transistor are on a chip it is referred to an an *integrated circuit* or IC. Large-scale integrated circuits, LSI, contain thousands of transistors. And today even very-large-scale integrated circuits, VLSI, exist, with hundreds of thousands of transistors.

Now lets talk physics.

4.1 Energy Levels

The physical principles of semiconductor devices can be understood by considering quantum energy levels in the material. I will just give a sketchy view here and define some terminology.

Valance electrons are the electrons outside the closed shells of an atom. In silicon and germanium there are four valence electrons, arsenic has five and gallium three. The large number of valance electrons favour these elements as semiconductors.

To sustain an electric current, a material must have charge carriers that are free to move. There is some probability that an atom may eject a valence electron which is then free to move in the material. The conductivity of a material is thus a function of the number of free charge carriers per unit volume. Based on these probability densities it is common to divide materials into three categories: conductors, semiconductors and insulators.

In crystals atoms interact and bind by sharing valence electrons. The wave function is no longer associated with a single atom but extends over the entire crystal. One effect of the interaction between the atoms is that the otherwise degenerate energy levels split into closely spaced levels. Since the number of atoms is large, it is common to refer to this set of levels as a continuous *energy band*.

In solid materials there usually exist a *valance band* which is an energy region where the states are filled or partially filled by valence electrons. The *conduction band* is defined to be the lowest unfilled energy band. So our three materials can be characterized by their band structure. An insulator has the valence and conduction band well separated. A semiconductor has the valence band close to the conduction band – separated by about a 1 eV gap. Conductors on the other hand have the conduction and valence bands overlapping.

The interesting property of a semiconductor is that thermally excited electrons can move from the valence band to the conduction band and conduct current. Silicon and germanium have thermally excited electrons at room temperature and hence their common use in diodes and transistors.

When an electron has been excited into the conduction band, the hole left behind in the valence band is also free to move through the crystal. A quantum mechanical treatment of this effect puts the hole on an approximately equal footing with the electron. Temperature causes the thermal generation of electron-hole pairs. One of the components of the pair will add a little to the *majority charge carriers*. The other component of the electron-hole pair will become the *minority charge carrier*. Minority charge carriers limit ideal performance and increase with increasing temperature.

A common method for generating even more charge carriers in a semiconductor is by *doping*. That is, replacing a few atoms of the base material with atoms of a different element. These impurities will contribute an excess electron or hole which is loosely bound and hence can be excited into the conduction band by thermal energy. In N-type semiconductors the majority of free charge carriers are negative, while a P-type semiconductor has majority positive charge carriers.

4.2 The PN Junction and the Diode Effect

By joining a P-type and N-type semiconductor together we can make a diode (figure 4.1)

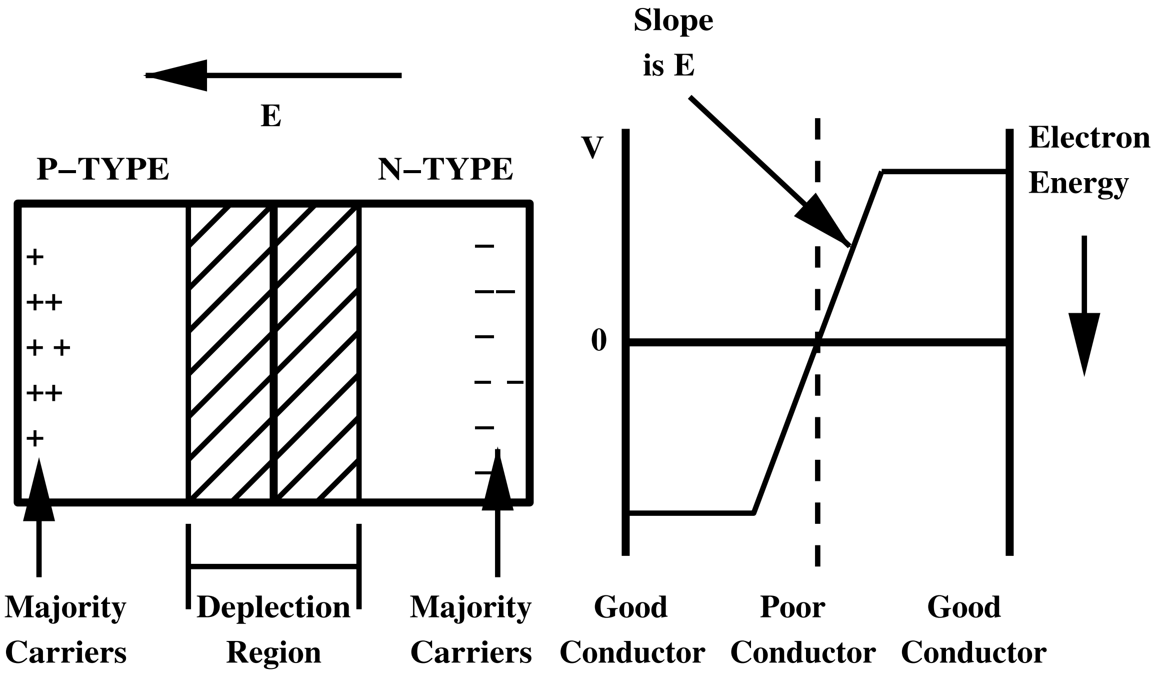


Figure 4.1: PN junction diode.

Initially both semiconductors are totally neutral. The concentration of positive and negative carriers are quite different on opposite sides of the junction and the thermal energy-powered diffusion of positive carriers into the N-type material and negative carriers into the P-type material occurs. The N-type material acquires an excess of positive charge near the junction and the P-type material acquires an excess of negative charge. Eventually diffuse charges build up and an electric field is created which drives the minority charges and eventually equilibrium is reached. A region develops at the junction called the *depletion region*. This region is essentially un-doped or just intrinsic silicon.

To complete the diode conductor, leads are placed at the ends of the PN junction.

4.2.1 Current in the Diode

The behaviour of a diode depends on its polarity in the circuit (figure 4.2). If the diode is *reversed biased* (positive potential on N-type material) the depletion region increases. The only charge carriers able to support a net current across the PN junction are the minority carriers and hence the reverse current is very small. A *forward-biased* diode (positive potential on P-type material) has a decreased depletion region; the majority carriers can diffuse across the junction. The voltage may become high enough to eliminate the depletion region entirely.

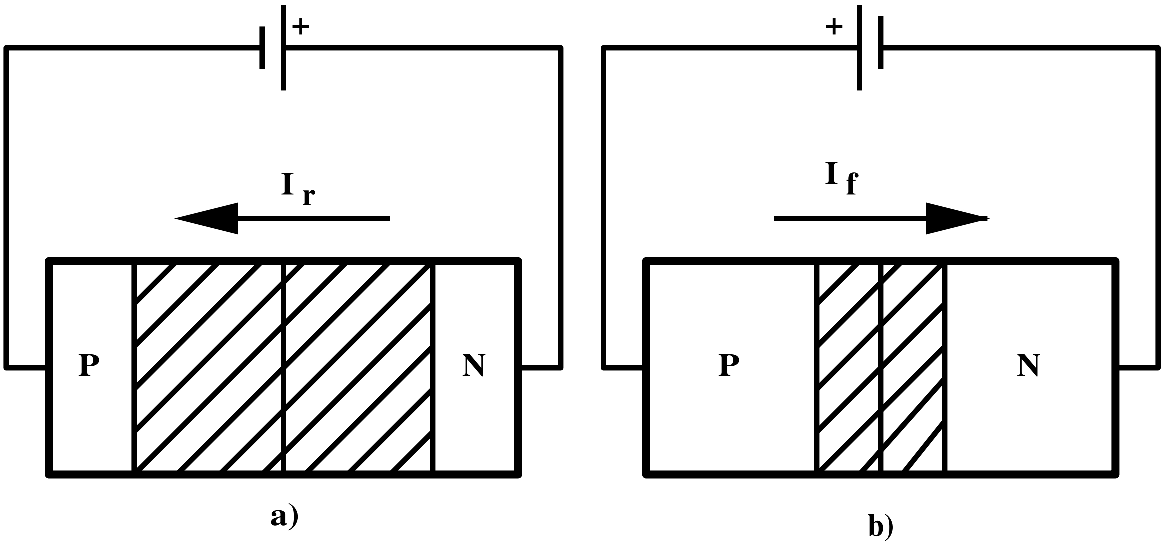


Figure 4.2: Diode circuit connections: a) reversed biased and b) forward biased.

An approximation to the current in the PN junction region is given by (shown in figure 4.3a)

$$I = I_0(e^{V/V_T} - 1), \tag{4.1}$$

where both I_0 and V_T are temperature dependent. This equation gives a reasonably accurate prediction of the current-voltage relationship of the PN junction itself – especially the temperature variation – and can be improved somewhat by choosing I_0 and V_T empirically to fit a particular diode. However, for a real diode, other factors are also important: in particular, edge effects around the boarder of the junction cause the actual reverse current to increase slightly with reverse voltage, and the finite conductivity of the doped semi-conductor ultimately restricts the forward current to a linear increase with increasing applied voltage. A better current-voltage curve for the real diode is shown in the figure 4.3b.

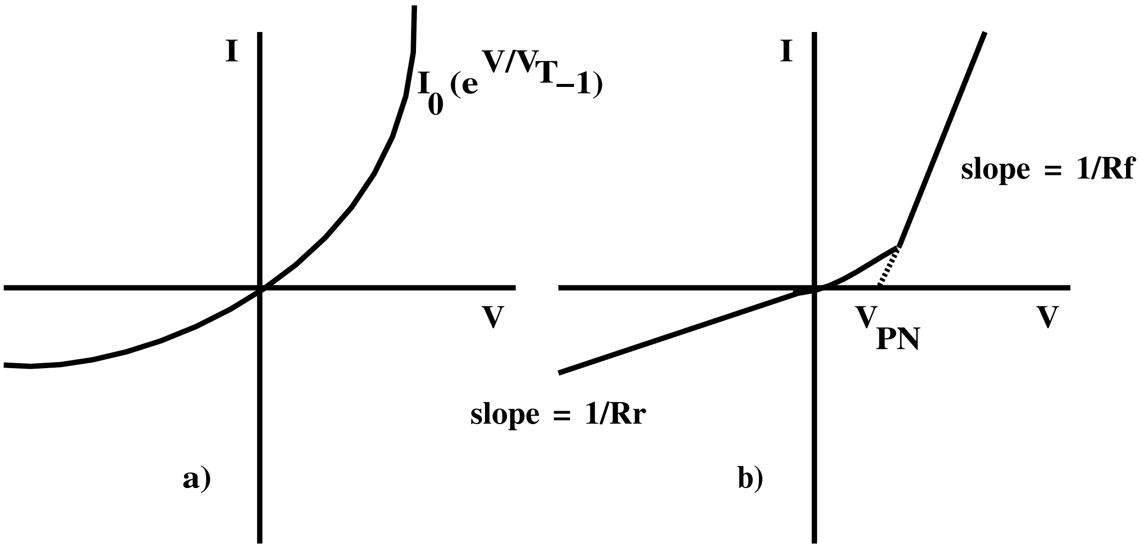


Figure 4.3: Current versus voltage a) in the PN junction region and b) for an actual PN diode.

Various regions of the curve can be identified. The linear region of forward-biasing. A non-linear transition region, a turn-on voltage (V_{PN}) and a reverse-biased region. We can assign a dynamic resistance to the diode in each of the linear regions: R_f in the forward-biased region and R_r in the reverse-biased region. These resistances are defined as the inverse slope of the curve: $1/R = \Delta I/\Delta V$. The voltage V_{PN}, represents the effective voltage drop across a forward-biased PN junction (the turn-on voltage). For a germanium diode, V_{PN} is approximately 0.3 V, while for a silicon diode it is close to 0.6 V.

4.2.2 The PN Diode as a Circuit Element

Diodes are refereed to as non-linear circuit elements because of the above characteristic curve. For most applications the non-linear region can be avoided and the device can be modeled by piece-wise linear circuit elements. Qualitatively we can just think of an ideal diode has having two regions: a conduction region of zero resistance and an infinite resistance non-conduction region. For many circuit applications, this ideal diode model is an adequate representation of an actual diode and simply requires that the circuit analysis be separated into two parts: forward current and reverse current. Figure 4.4 show a schematic symbol for a diode and the current-voltage curve for an ideal diode.

A diode can more accurately be described using the equivalent circuit model shown in figure 4.5. If a diode is forward biased with a high voltage it acts like a resistor (R_f) in series with a voltage source (V_{PN}). For reverse biasing it acts simply as a resistor (R_r). These

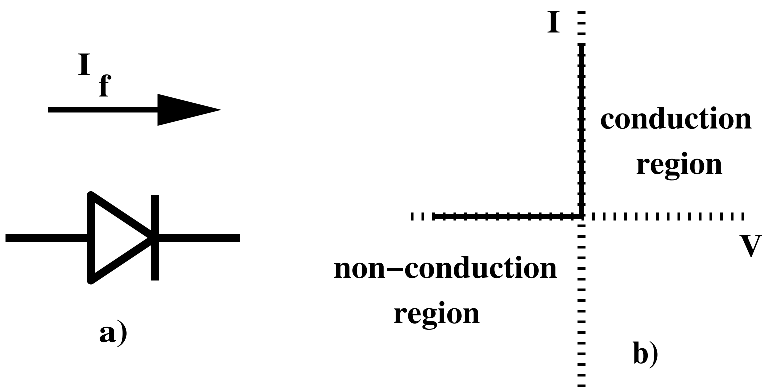


Figure 4.4: a) Schematic symbol for a diode and b) current versus voltage for an ideal diode.

approximations are referred to as the linear element model of a diode.

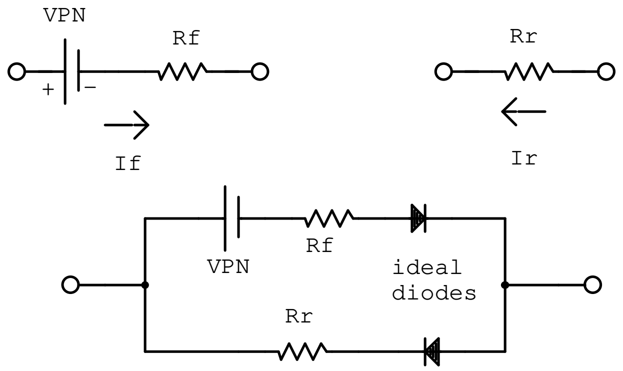


Figure 4.5: Equivalent circuit model of a junction diode.

4.2.3 The Zener Diode

There are several other types of diodes beside the junction diode. As the reverse voltage increases the diode can avalanche-breakdown (zener breakdown). This causes an increase in current in the reverse direction. *Zener breakdown* is when the electric field near the junction becomes large enough to excite valence electrons directly into the conduction band. *Avalanche breakdown* is when the minority carriers are accelerated in the electric field near the junction to sufficient energies that they can excite valence electrons by collisions. Figure 4.6 show the current-voltage characteristic of a zener diode, its schematic symbol and equivalent circuit model in the reverse-bias direction. The best zener diodes have a breakdown voltage (V_Z) of 6-7 V.

4.2.4 Light-Emitting Diodes

Light-emitting diodes (LED) emits light in proportion to the forward current through the diode. LEDs are low voltage devices that have a longer life than incandescent lamps. They

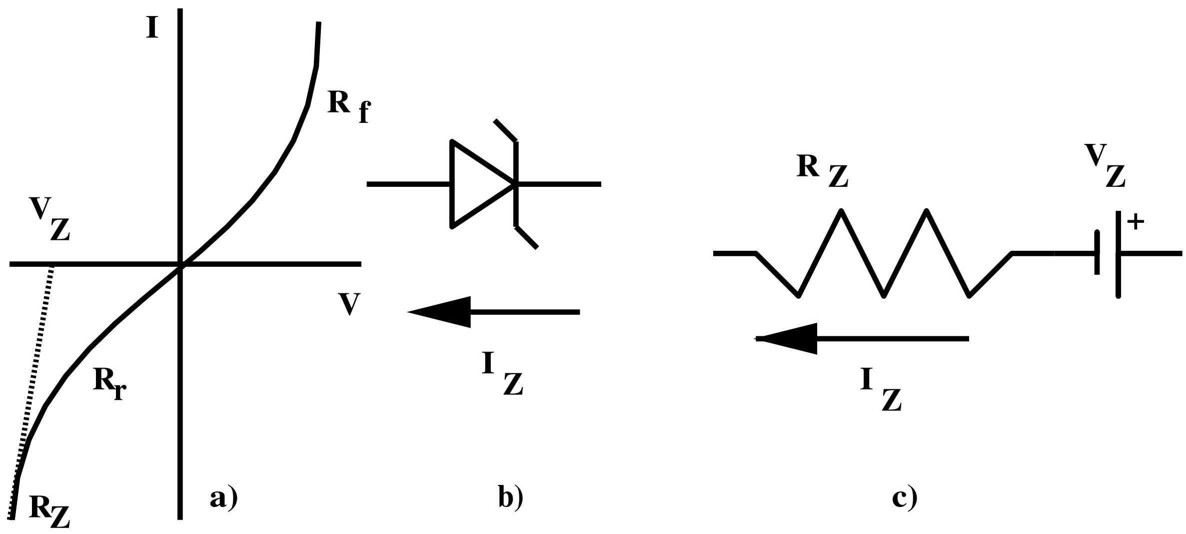


Figure 4.6: a) Current versus voltage of a zener diode, b) schematic symbol for a zener diode and c) equivalent circuit model of a zener diode in the reverse-bias direction.

respond quickly to changes in current (10 MHz). LEDs have application in optical-fiber communication and diode lasers. They produce a narrow spectrum of coherent red or infrared light that can be well collimated.

As an electron in the conduction band recombines with a hole in the valence band, the electron makes a transition to a lower-lying energy state and releases energy in an amount equal to the band-gap energy. Normally the energy heats the material. In an LED this energy goes into emitted infrared or visible light.

4.2.5 Light-Sensitive Diodes

If light of the proper wavelength is incident on the depletion region of a diode while a reverse voltage is applied, the absorbed photons can produce additional electron-hole pairs. Photodiodes or photocells can receive frequency-modulated light signals. LEDs and photodiodes are often used in optical communication as receiver and transmitter respectively.

4.3 Circuit Applications of Ordinary Diodes

Lets briefly discuss some applications of ordinary diodes. For many circuits only the basic diode effect is of any significance and these circuits can be analyzed under the assumption that the diode is an ideal device.

4.3.1 Power Supplies

Batteries are often shown on a schematic diagram as the source of DC voltage but usually the actual DC voltage source is a power supply. A more reliable method of obtaining DC power is to transform, rectify, filter and regulate an AC line voltage. Power supplies make use of simple circuits which we will discuss presently.

DC power supplies are often constructed using a common inexpensive three-terminal regulator. These regulators are integrated circuits consisting of several solid state devices and are designed to provide the desirable attributes of temperature stability, output current limiting and thermal overload protection.

In power supply applications it is common to use a transformer to isolate the power supply from the 110 V AC line. A rectifier can be connected to the transformer secondary to generate a DC voltage with little AC ripple. The object of any power supply is to reduce the *ripple* which is the periodic variations in voltage about the steady value.

4.3.2 Rectification

Figure 4.7 show a half-wave rectifier circuit. The signal is exactly the top half of the input voltage signal, and for an ideal diode does not depend at all on the size of the load resistor.

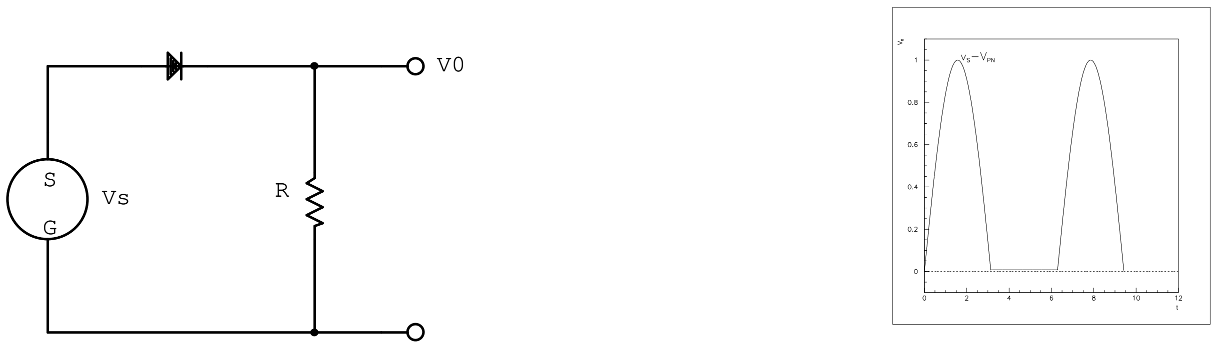


Figure 4.7: Half-wave rectifier and its output waveform.

The rectified signal is now a combination of an AC signal and a DC component. Generally, it is the DC part of a rectified signal that is of interest, and the un-welcomed AC component is described as ripple. It is desirable to move the ripple to high frequencies where it is easier to remove by a low-pass filter.

When diodes are used in small-signal applications – a few volts – their behaviour is not closely approximated by the ideal model because of the PN turn-on voltage. The equivalent circuit model can be used to evaluate the detailed action of the rectifier under these conditions. During the part of the wave when the input is positive but less than the PN turn-on voltage, the model predicts no loop current and the output signal voltage is therefore zero. When the input exceeds this voltage, the output signal becomes proportional to $v_s - V_{PN}$, or about 0.6 V lower than the source voltage.

The diode bridge circuit shown in figure 4.8 is a full-wave rectifier. The diodes act to route the current from both halves of the AC wave through the load resistor in the same direction, and the voltage developed across the load resistor becomes the rectified output signal. The diode bridge is a commonly used circuit and is available as a four-terminal component in a number of different power and voltage ratings.

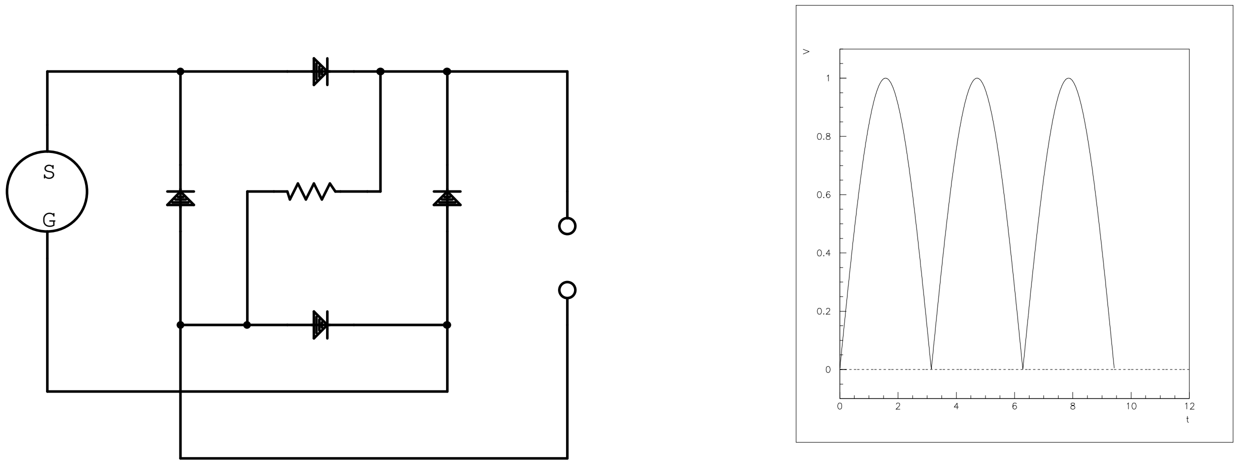


Figure 4.8: Full-wave rectifier and its output waveform.

4.3.3 Power Supply Filtering

The rectified waveforms still have a lot of ripple that has to be smoothed out in order to generate a genuine DC voltage. This we do by tacking on a low-pass filter. The capacitor value is chosen in order to ensure small ripple, by making the time constant for discharging much longer than the time between re-charging.

4.3.4 Split Power Supply

Often a circuit requires a power supply that provides negative voltage as well as positive voltage. By reversing the direction of the diode and the capacitor (if it is polarized), the half-wave rectification circuit with low-pass filter provide a negative voltage. Similarly, reversing the direction of the diodes and capacitor in the full-wave rectified supply produces a negative voltage supply. A split power supply is shown in figure 4.9.

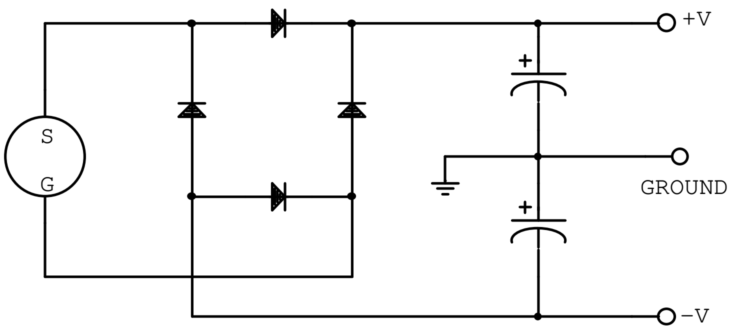


Figure 4.9: Split power supplies.

4.3.5 Voltage Multiplier

A voltage multiplier circuit is shown in figure 4.10. We can think of it as two half-wave rectifier circuits in series. During the positive half-cycle one of the diodes conducts and charges a capacitor. During the negative half-cycle the other diode conducts negatively to charge the other capacitor. The voltage across the combination is therefore equal to twice the peak voltage. In this type of circuit we have to assume that the load does not draw a significant charge from the capacitors.

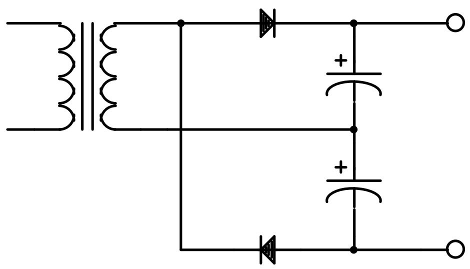


Figure 4.10: Voltage doubler circuit.

4.3.6 Clamping

When a signal drives an open-ended capacitor the average voltage level on the output terminal of the capacitor is determined by the initial charge on that terminal and my therefore be quite unpredictable. Thus it is necessary to connect the output to ground or some other reference voltage via a large resistor. This action drains any excess charge and results in an average or DC output voltage of zero.

A simple alternative method of establishing a DC reference for the output voltage is by using a diode clamp as shown in figure 4.11. By conducting whenever the voltage at the output terminal of the capacitor goes negative, this circuit builds up an average charge on the terminal that is sufficient to prevent the output from ever going negative. Positive charge on this terminal is effectively trapped.

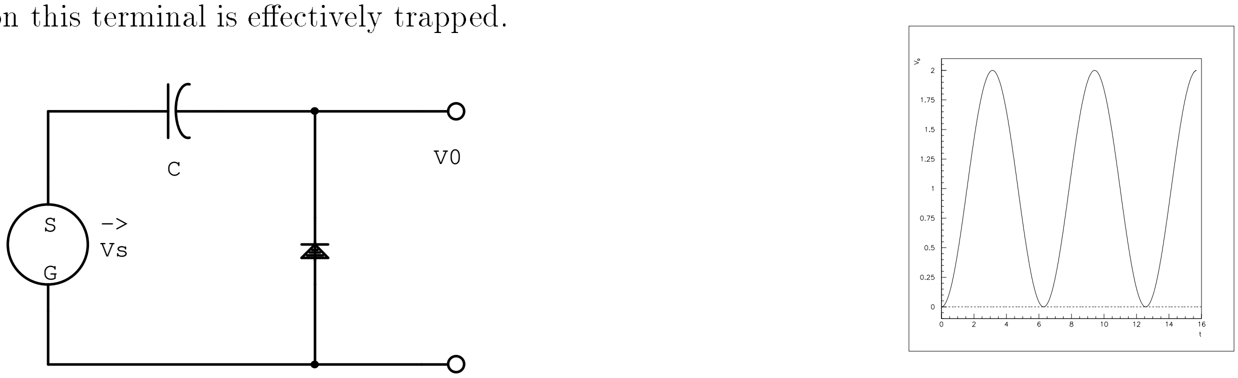


Figure 4.11: Diode clamp circuit and its output waveform.

4.3.7 Clipping

A diode clipping circuit can be used to limit the voltage swing of a signal. Figure 4.12 show a diode circuit that clips both the positive and negative voltage swings to references voltages.

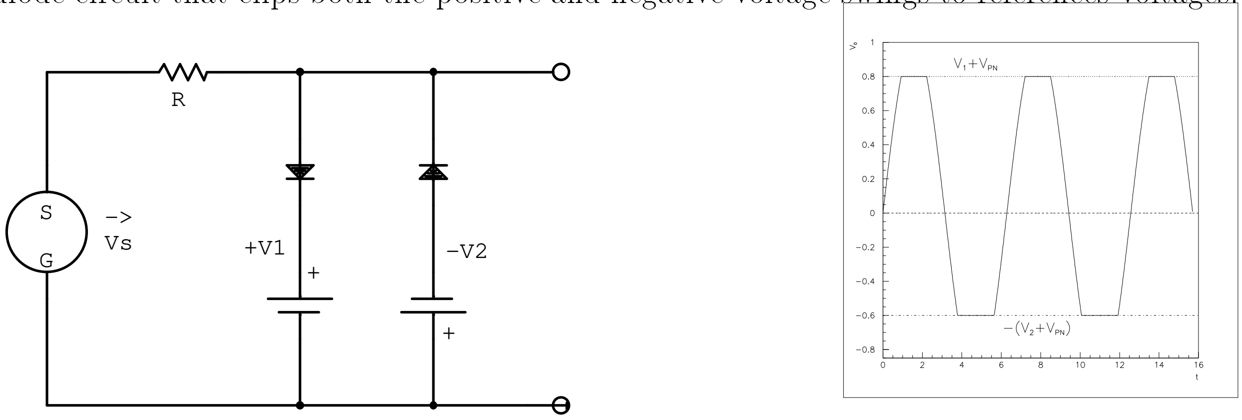


Figure 4.12: Diode clipping circuit and its output waveform.

4.3.8 Diode Gate

Diodes can also be used to pass the higher of two voltages without affecting the lower. A nifty example is shown in figure 4.13 The battery does nothing until the power fails; then it takes over without interruption.

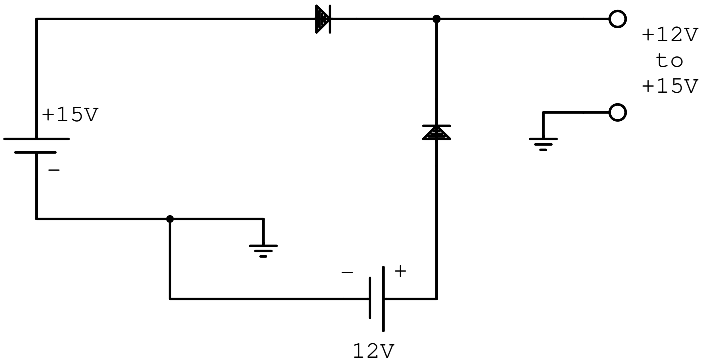


Figure 4.13: Diode OR gate.

4.3.9 Diode Protection

An important use of diodes is to suppress the voltage surge present when an inductive load is switched out of a circuit – inductive serge suppression. With inductors it is not possible to turn off the current suddenly since the inductor will try to keep the current flowing when the switch is opened. A diode in a DC circuit or back-to-back zener diodes in an AC circuit can be used to shunt the inductor and prevent it from conducting.

Example: *For each circuit in figure 4.14 sketch the output voltage as a function of time if $\vec{v}_s(t) = 10\cos(2000\pi t)$ V. Assume that the circuit elements are ideal.*

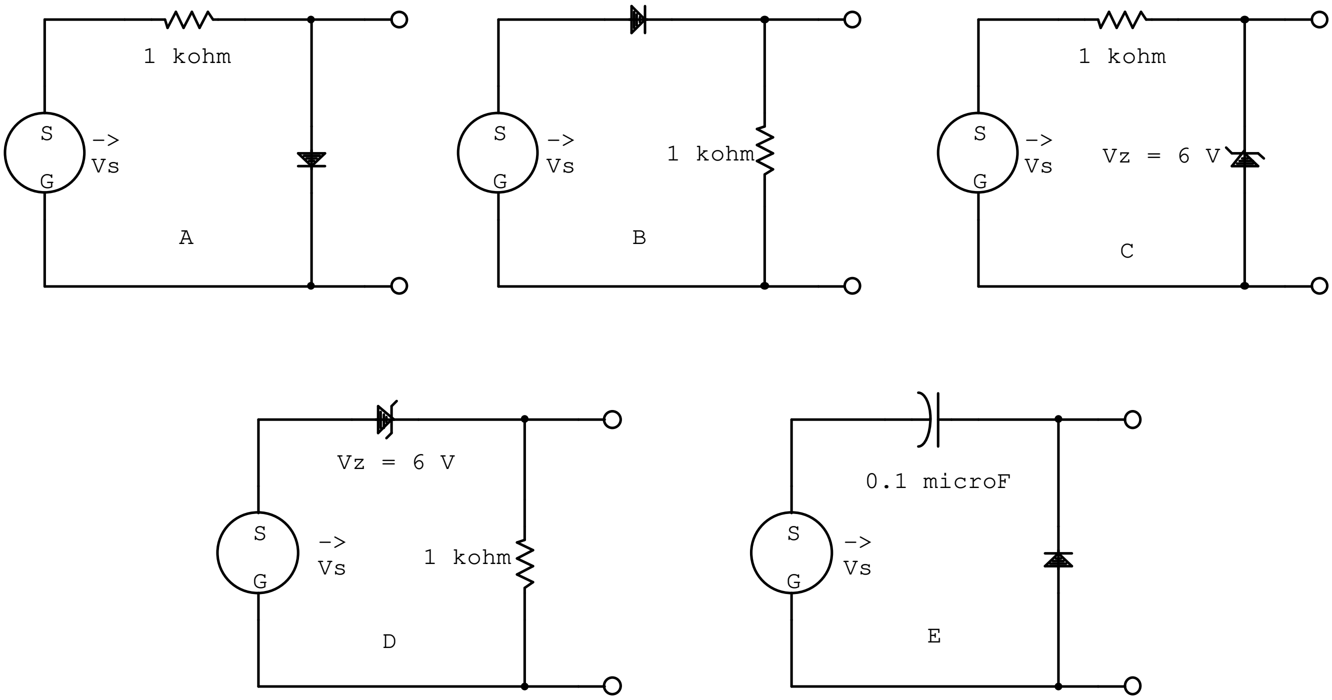


Figure 4.14: Circuits with a single ideal diode.

The forward and reverse biased approximations for the circuit in figure 4.14a are shown in figure 4.15 and the output voltage is sketched in figure 4.19a.

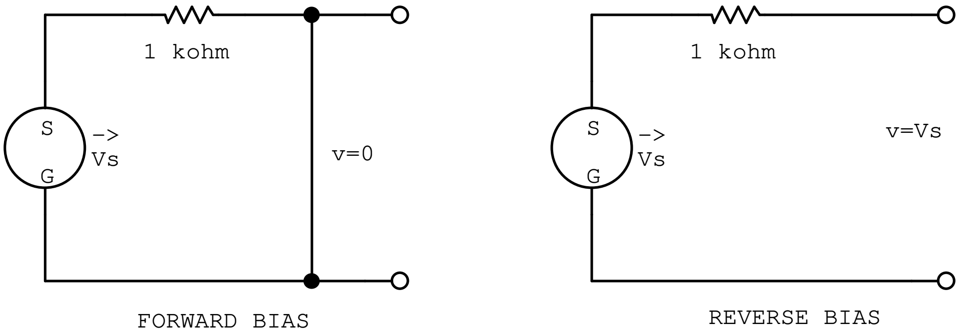


Figure 4.15: Single diode circuit a).

The forward and reverse biased approximations for the circuit in figure 4.14b are shown in figure 4.16 and the output voltage is sketched in figure 4.19b.
The forward and reverse biased approximations for the circuit in figure 4.14c are shown in figure 4.17 and the output voltage is sketched in figure 4.19c.

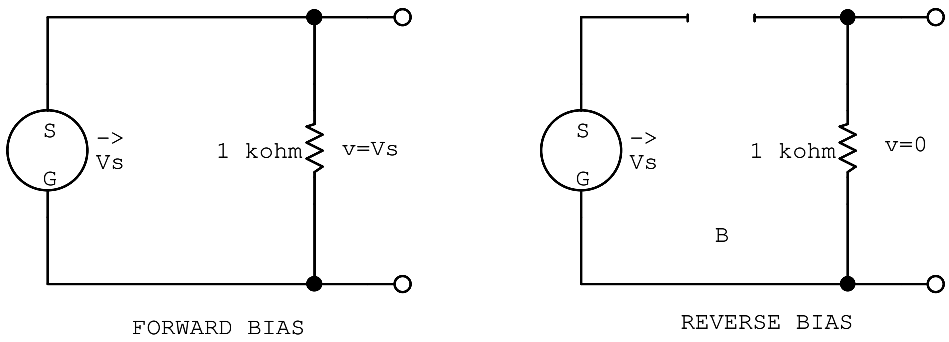


Figure 4.16: Single diode circuit b).

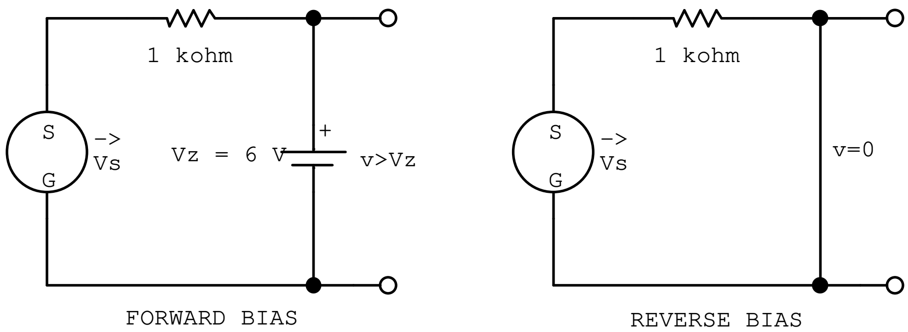


Figure 4.17: Single diode circuit c).

The forward and reverse biased approximations for the circuit in figure 4.14d are shown in figure 4.18 and the output voltage is sketched in figure 4.19d.
The forward and reverse biased approximations for the circuit in figure 4.14e are shown in figure 4.19 and the output voltage is sketched in figure 4.19e.

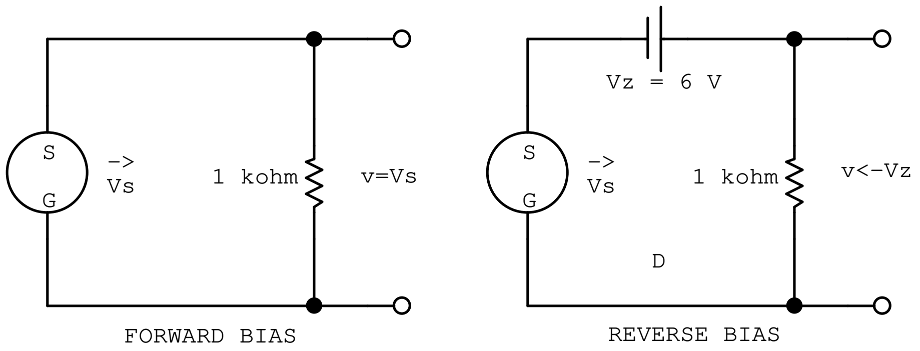


Figure 4.18: Single diode circuit d).

Example: *Assuming that the diodes in the circuit below are ideal, write expressions for the voltage at points A and B.*
Consider when the current flows in the clockwise direction (figure 4.22). $V_A = V_B = V_0$ *in the steady state because the charge just builds (it has nowhere to "drain" to).*
Consider when the current flows in the anti-clockwise direction (figure 4.23). $V_A = V_0 \cos \omega t$, *since this is just the output terminal of the voltage source.* $V_B = V_0$ *in the steady state, again since the charge cannot go anywhere.*
Thus by superposition

$$V_A = V_0 + V_0 \cos \omega t \quad (4.2)$$
$$V_B = V_0 + V_0 = 2V_0. \quad (4.3)$$

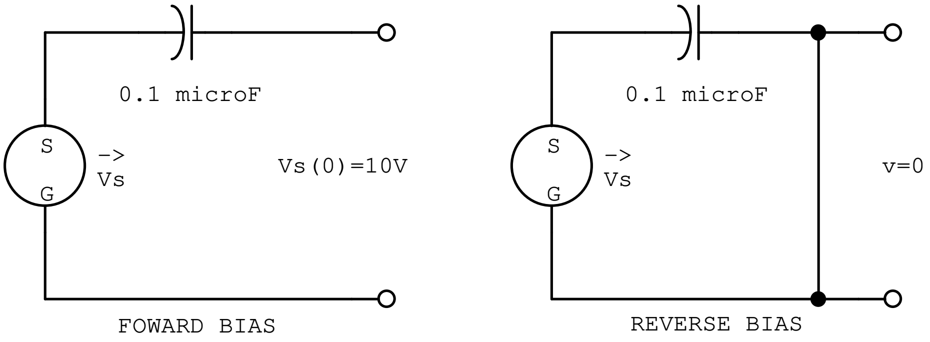


Figure 4.19: Single diode circuit e).

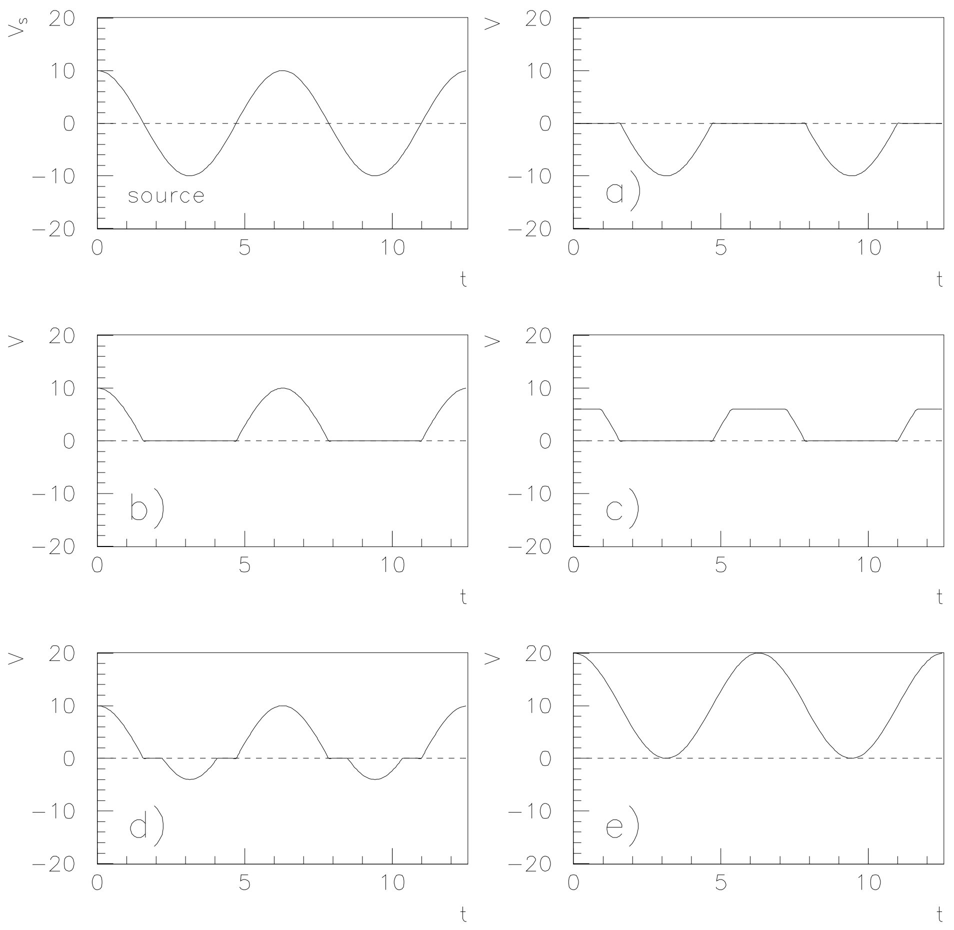


Figure 4.20: Sketch of the output voltage as a function of time.

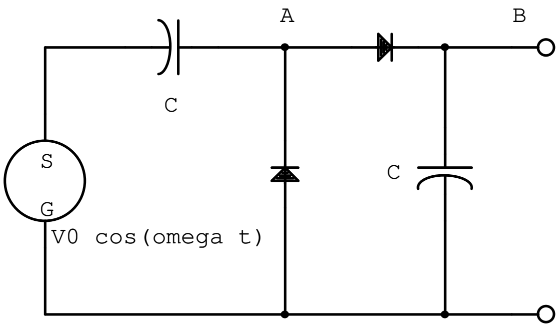


Figure 4.21: A circuit with two ideal diodes.

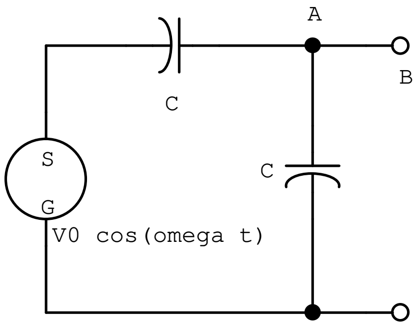


Figure 4.22: Current clockwise.

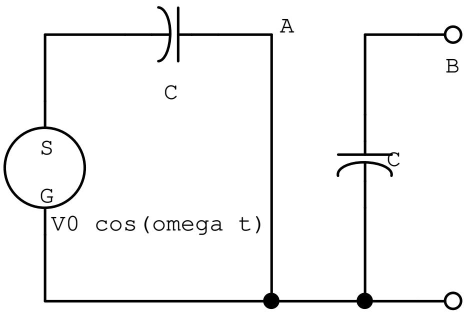


Figure 4.23: Current anti-clockwise.

4.4 Problems

1. (a) Make a sketch showing the current through an ideal diode as a function of the applied voltage. Also sketch the current through a real signal diode as a function of voltage.

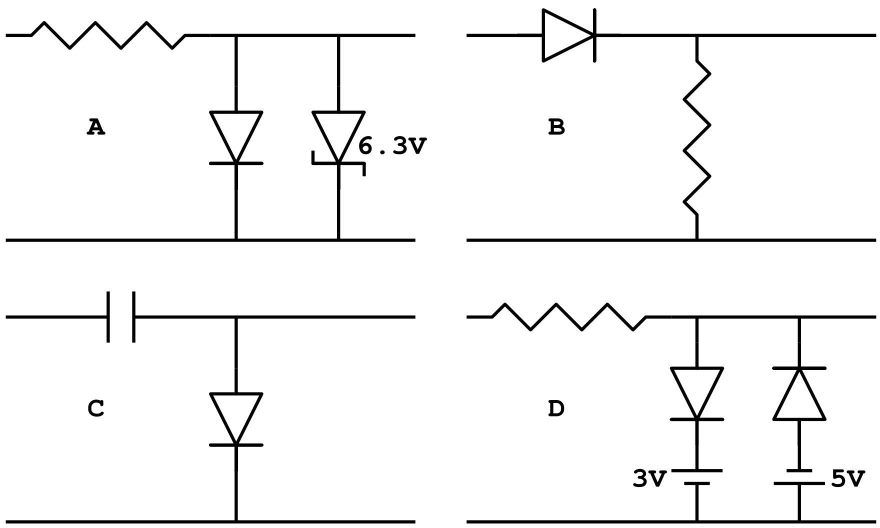
   (b) Make a sketch showing the current drawn through a Zener diode as a function of the applied voltage. Show how to determine the forward resistance (R_f), the reverse resistance (R_r) and the Zener resistance (R_Z) from your sketch. Label the voltages V_{PN} and V_Z.

2. Sketch the expected output waveforms when

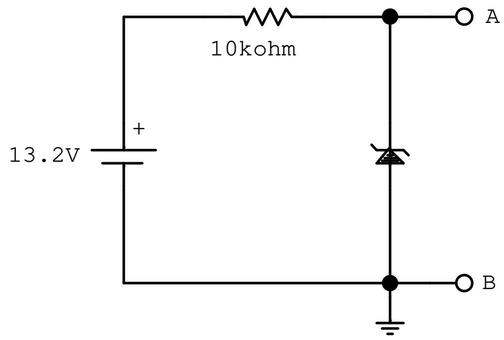
   (a) a 100 Hz sine wave with a peak voltage of 5 V, and

   (b) a 100 Hz square wave with a peak-to-peak voltage of 10 V

   are applied separately to each of the circuits below.



3. The Zener diode in the following circuit is characterized by $V_{PN} = 0.6$ V and $|V_Z| =$ 4.8 V. Terminal B is at ground and there is no external load resistor.



(a) What is the voltage at terminal A in the above circuit?

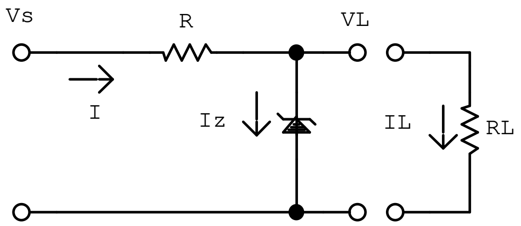
(b) What is the current through the Zener? (What reasonable approximation makes this straightforward?).

(c) If the Zener is dissipating 1.0 μW (in heat), what can we conclude to be the effective impedance of the diode for this situation?

4. The effects of a Zener diode in a circuit can be treated analytically by using an equivalent circuit model of the reverse-biased condition. In the low voltage region, before breakdown, the Zener diode can be treated like any other reverse-biased diode. However, the Zener diode is normally operated in the breakdown region.

   (a) Write down an equivalent linear-circuit model in the breakdown voltage region.

   (b) Replace the Zener diode in the following voltage reference circuit by your equivalent circuit model.



   (c) Determine the contribution of the of Zener diode to this voltage reference circuit by calculating the elements of a Thevenin equivalent circuit representation.

   (d) Show that for small Zener diode effective resistance the Thevenin equivalent voltage is close to the Zener breakdown voltage and thus is insensitive to changes in the source voltage.

   (e) Show that for small Zener diode effective resistance, the Thevenin equivalent resistor gives the voltage source a reasonably small output impedance.

   (f) The combined results show a voltage reference that is insensitive to voltage changes in the original EMF and to changes in the load current. State the assumptions under which this result is valid.

Chapter 5

Transistor Circuits

The circuits we have encounter so far are passive and dissipate power. Even a transformer that is capable of giving a voltage gain to a circuit is not an active element. *Active* elements in a circuit increase the power by controlling or modulating the flow of energy or power from an additional power supply into the circuit.

Transistors are active circuit elements and are typically made from silicon or germanium and come in two types. The bipolar transistor controls the current by varying the number of charge carriers. The field effect transistor (FET) varies the current by varying the shape of the conducting volume.

Before starting we define some notation. The voltages that are with respect to ground are indicated by a single subscript. Voltages with repeated letters are power supply voltages. And voltages between two terminals are indicated by a double subscript.

5.1 Bipolar Junction Transistors

By placing two PN junctions together we can create a bipolar transistor. In a PNP transistor the majority charge carriers are holes and germanium is favoured for these devices. Silicon is best for NPN transistors where the majority charge carriers are electrons.

The thin and lightly doped central region is known as the *base* (B) and has majority charge carriers of opposite polarity to those in the surrounding material. The two outer regions are known as the *emitter* (E) and the *collector* (C). Under the proper operating conditions the emitter will emit or inject majority charge carriers into the base region, and because the base is very thin, most will ultimately reach the collector. The emitter is highly doped to reduce resistance. The collector is lightly doped to reduce the junction capacitance of the collector-base junction.

The schematic circuit symbols for bipolar transistors are shown in figure 5.1. The arrows on the schematic symbols indicate the direction of both I_B and I_C. The collector is usually at a higher voltage than the emitter. The emitter-base junction is forward biased while the collector-base junction is reversed biased.

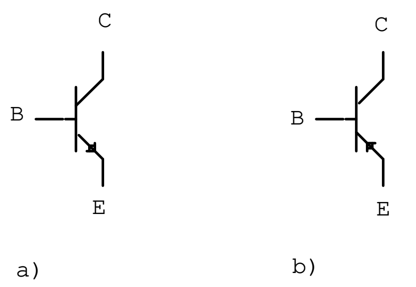


Figure 5.1: a) NPN bipolar transistor and b) PNP bipolar transistor.

5.1.1 Transistor Operation (NPN)

If the collector, emitter, and base of an NPN transistor are shorted together as shown in figure 5.2a, the diffusion process described earlier for diodes results in the formation of two depletion regions that surround the base as shown. The diffusion of negative carriers into the base and positive carriers out of the base results in a relative electric potential as shown in figure 5.2b.

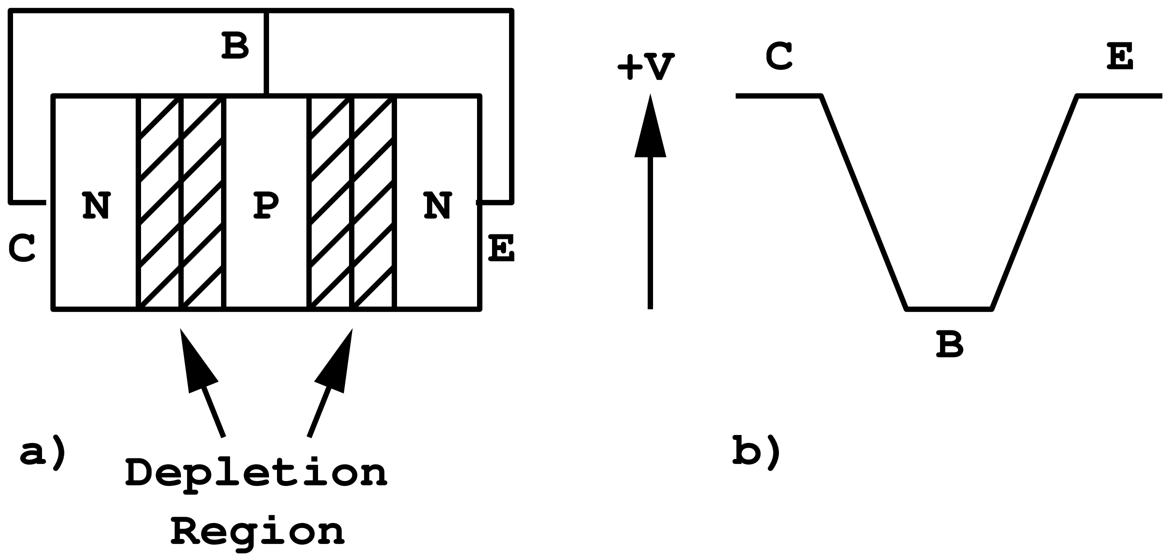


Figure 5.2: a) NPN transistor with collector, base and emitter shorted together, and b) voltage levels developed within the shorted semiconductor.

When the transistor is biased for normal operation as in figure 5.3a, the base terminal is slightly positive with respect to the emitter (about 0.6 V for silicon), and the collector is positive by several volts. When properly biased, the transistor acts to make $I_C \gg I_B$. The depletion region at the reverse-biased base-collector junction grows and is able to support the increased electric potential change indicated in the figure 5.3b.

For a typical transistor, 95% to 99% of the charge carriers from the emitter make it to

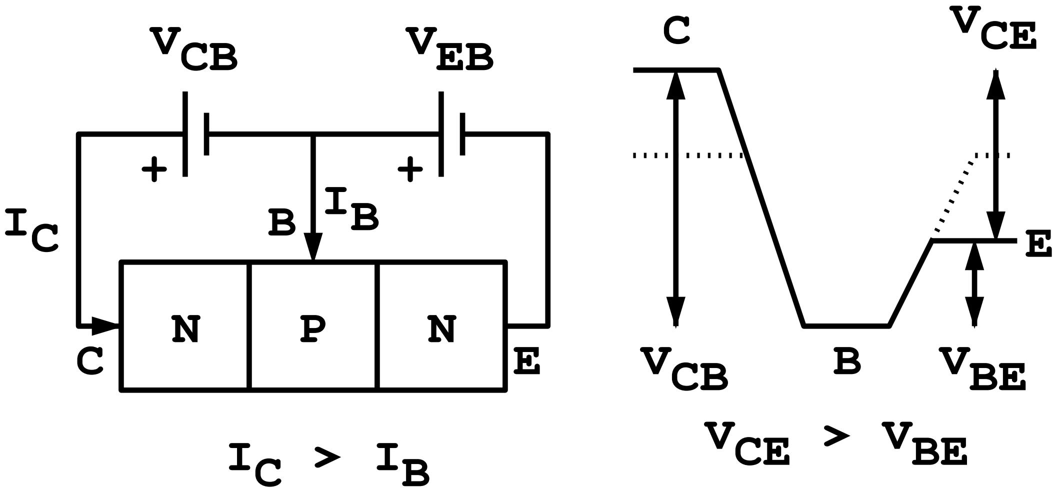


Figure 5.3: a) NPN transistor biased for operation and b) voltage levels developed within the biased semiconductor.

the collector and constitute almost all the collector current I_C. I_C is slightly less than I_E and we may write $\alpha = I_C/I_E$, where from above $\alpha = 0.95$ to 0.99.

The behaviour of a transistor can be summarized by the characteristic curves shown in figure 5.4. Each curve starts from zero in a nonlinear fashion, rises smoothly, then rounds a knee to enter a region of essentially constant I_C. This flat region corresponds to the condition where the depletion region at the base-emitter junction has essential disappeared. To be useful as a linear amplifier, the transistor must be operated exclusively in the flat region, where the collector current is determined by the base current.

A small current flow into the base controls a much larger current flow into the collector. We can write

$$I_C = \beta I_B = h_{FE} I_B, \tag{5.1}$$

where β is the DC current gain and h_{FE} is called the static forward-current transfer ratio. From the previous definition of α and the conservation of charge, $I_E = I_C + I_B$, we have

$$\beta = \frac{\alpha}{1-\alpha}. \tag{5.2}$$

For $\alpha = 0.99$ we have $\beta = 99$ and the transistor is a current amplifying device.

5.1.2 Basic Circuit Configurations

In any transistor circuit design you must supply a DC bias current and voltage to operate in the linear region of the characteristic curve. The DC *operating point* is defined by the values of I_B, I_C, V_{BE} and V_{CE}. You must also obtain the proper AC operation.

The transistor is a three-terminal device that we will use to form a four-terminal circuit. Small voltage changes in the base-emitter junction will produce large current changes in

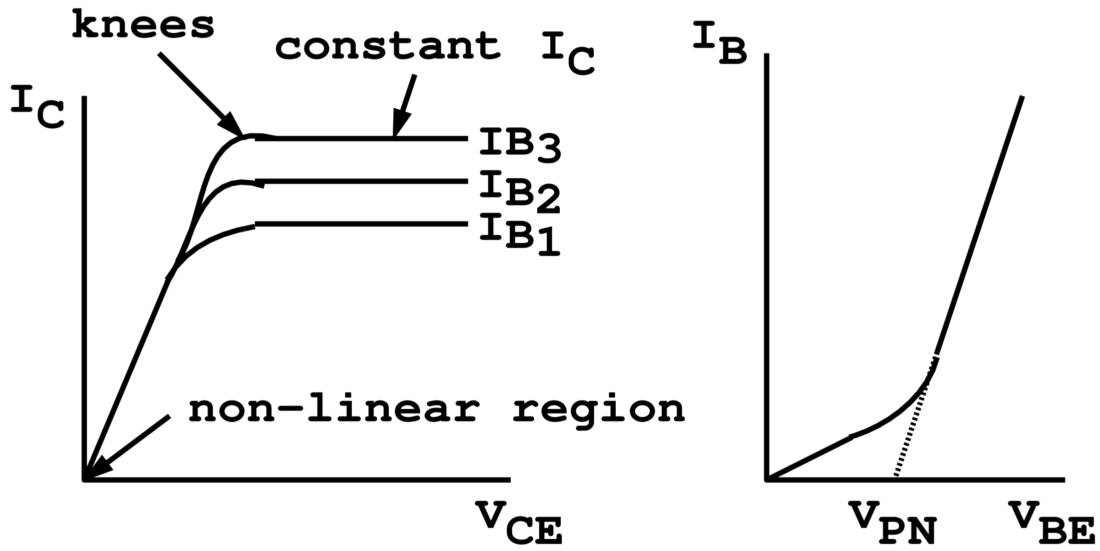


Figure 5.4: Characteristic curves of an NPN transistor.

the collector and emitter, whereas small changes in the collector-emitter voltage have little effect on the base. The result is that the base is always part of the input to a four-terminal network. There are three common configurations: common emitter (CE), common collector (CC) and common base (CB), as shown in figure 5.5.

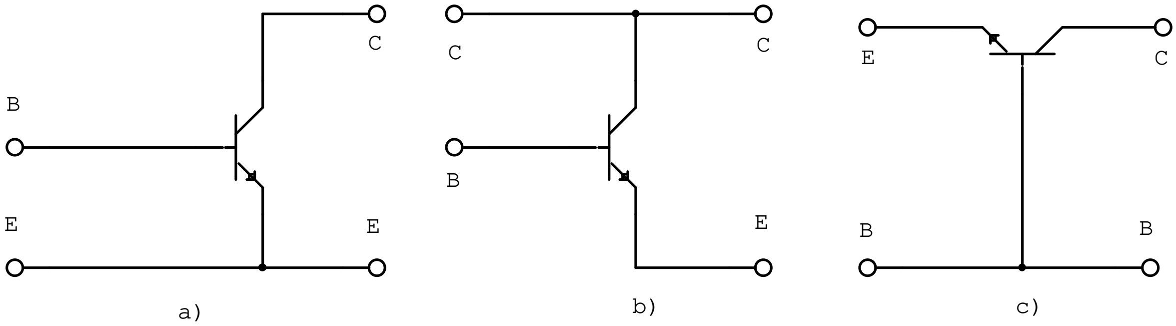


Figure 5.5: Transistor basic circuit configurations: a) common emitter (CE), b) common collector (CC) and c) common base (CB).

The operating characteristics of the different circuit configurations are shown in table 5.1.

5.1.3 Small-Signal Models

A simple transistor model is given by $I_C = h_{FE} I_B$. A more general model capable of describing the family of characteristic curves is given by

$$I_C = I_C(I_B, V_{CE}), \tag{5.3}$$

Characteristic	*CE*	*CC*	*CB*
power gain	yes	yes	yes
voltage gain	yes	no	yes
current gain	yes	yes	no
input resistance	3.5 kΩ	580 kΩ	30 Ω
output resistance	200 kΩ	3 5 Ω	3.1 MΩ
voltage phase change	yes	no	no

Table 5.1: Operating characteristics of different transistor circuit configurations.

where I_C is a transistor-dependent function.

For AC analysis only time changes are important and we may write

$$\frac{dI_C}{dt} = \frac{\partial I_C}{\partial I_B}\frac{dI_B}{dt} + \frac{\partial I_C}{\partial V_{CE}}\frac{dV_{CE}}{dt}, \tag{5.4}$$

where the partial derivatives are evaluated at a particular I_B and V_{CE} – the operating point. $h_{fe} \equiv \partial I_C/\partial I_B|_{I_B,V_{CE}}$ is the forward current transfer ratio and describes the vertical spacing $\Delta I_C/\Delta I_B$ between the curves. $h_{oe} \equiv \partial I_C/\partial V_{CE}|_{I_B,V_{CE}}$ is the output admittance (inverse resistance) and describes the slope $\Delta I_C/\Delta V_{CE}$ of one of the curves as it passes through the operating point.

Using these definitions we may write

$$\frac{dI_C}{dt} = h_{fe}\frac{dI_B}{dt} + h_{oe}\frac{dV_{CE}}{dt}. \tag{5.5}$$

The input signal V_{BE} is also related to I_B and V_{CE}, and a similar argument to the above gives

$$\frac{dV_{BE}}{dt} = h_{ie}\frac{dI_B}{dt} + h_{re}\frac{dV_{CE}}{dt}, \tag{5.6}$$

where h_{ie} is the input impedance and h_{re} is the reverse voltage ratio.

The differential equations are linear only in the limit of small AC signals, where the h parameters are effectively constant. The h parameters are in general functions of the variables I_B and V_{CE}. We arbitrarily picked I_B and V_{CE} as our independent variables. We could have picked any two of V_{BE}, V_{CE}, I_B and I_C. Because the current and voltage variables are mixed the h parameters are known as *hybrid* parameters.

In general the current and voltage signals will have both DC and AC components. The time derivatives involve only the AC component and if we restrict ourselves to sinusoidal AC signals, we may replace the time derivatives by the signals themselves (using complex notation). Our hybrid equations become

$$i_C = h_{fe}i_B + h_{oe}v_{CE} \quad \text{and} \tag{5.7}$$

$$v_{BE} = h_{ie}i_B + h_{re}v_{CE}. \tag{5.8}$$

The hybrid parameters are often used as the manufacturer's specification of a transistor, but there are large variations between samples. Thus one should use the actual measured parameters in any detailed calculation based on this model. Table 5.2 shows typical values for the hybrid parameters.

Symbol	*Name*	*Typical Value*
h_{fe}	forward current ratio	10^2
h_{ie}	input impedance	$2 \times 10^3\ \Omega$
h_{oe}	output admittance	$2 \times 10^{-5}\ \Omega^{-1}$
h_{re}	reverse voltage ratio	10^{-4}

Table 5.2: Hybrid parameters.

The relationship between the voltages and currents for a transistor in the common emitter configuration is shown in figure 5.6.

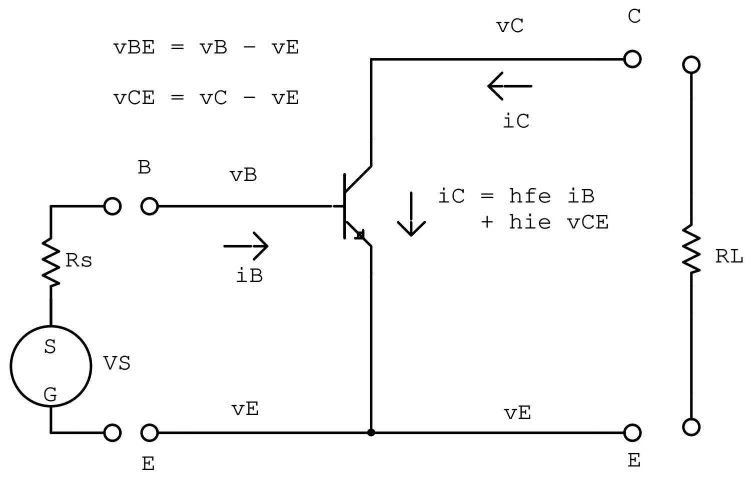


Figure 5.6: Transistor in the common emitter configuration.

We now make a few approximations to our hybrid parameter model to get an intuitive feel for how transistors behave in circuits. The voltage across the load resistor is

$$v_E - v_C = i_C R_L, \tag{5.9}$$
$$v_C - v_E = -i_C R_L \quad \text{and} \tag{5.10}$$
$$v_{CE} = -i_C R_L. \tag{5.11}$$

Substituting this into our first hybrid equation gives

$$i_C = \frac{h_{fe} i_B}{1 + h_{oe} R_L}. \tag{5.12}$$

If $h_{oe}R_L \ll 1$ (good to about 10%) we can write

$$i_C = h_{fe} i_B, \tag{5.13}$$

which is the AC equivalent of $i_C = \beta I_B = h_{FE} I_B$. Similarly, using the second hybrid equation gives

$$\frac{v_{CE}}{v_{BE}} = -\frac{R_L h_{fe}}{h_{ie} - R_L h_{fe} h_{ie}}. \tag{5.14}$$

If $R_L h_{fe} h_{re} \ll 1$ (good to about 10%) we have

$$\frac{v_{CE}}{v_{BE}} = -\frac{h_{fe}}{h_{ie}} R_L, \tag{5.15}$$

which is the AC voltage gain.

5.1.4 Ideal and Perfect Bipolar Transistor Models

By ignoring h_{oe} and h_{re} we can define a simplified AC model for the transistor (*perfect* transistor) that is independent of the circuit configuration:

$$\begin{aligned} i_C &= h_{fe} i_B \quad \text{and} && (5.16) \\ v_{BE} &= h_{ie} i_B. && (5.17) \end{aligned}$$

There is no PN voltage drop in these equations since it is a DC effect.

Since i_C is typically 100 times larger than i_B we can make the approximation $i_E \approx i_C$. An *ideal* transistor is defined such that $h_{ie} = 0$ and hence $v_B = v_E$. When the effects of h_{ie} cannot be ignored, we can use the perfect transistor model as described by the two equations above. On a circuit diagram h_{ie} can be added directly to the ideal transistor symbol.

The ideal transistor model has the following two working rules:

1. The base and emitter are at the same AC voltage ($v_B = v_E$). They differ only by a constant DC potential V_{PN}.

2. The collector current is equal to emitter current and proportional to the base current ($i_E = i_C, I_E = I_C, i_C = h_{fe} i_B$ and $I_C = h_{FE} i_B$).

5.1.5 Transconductance Model

The transconductance model provides an alternative description of transistor operation. The forward transconductance, which has units of inverse resistance, is defined as $g_m = h_{fe}/h_{ie}$. Using the perfect transistor model we can write

$$i_C = g_m(v_B - v_E) = g_m v_{BE}. \tag{5.18}$$

Since the transconductance is used to describe field effect transistors, it is sometimes convenient to apply the same parameter to bipolar transistors.

We now turn to the description of some simple amplifiers that use a single bipolar transistor. Our goal will be to estimate the voltage gains, current gains, input impedances, output impedances and corner frequencies of the amplifiers. The characteristics of a perfect amplifier are as follows:

- infinite input impedance (the amplifier draws no current),
- zero output impedance,
- infinite voltage and current gain, and
- stable, linear, etc.

5.2 The Common Emitter Amplifier

The common emitter configuration is the most versatile of the three. It has low input impedance, moderate output impedance, voltage gain and current gain. The input and output are often capacitively coupled. Before performing an AC analysis we will discuss DC biasing.

5.2.1 DC Biasing

DC biasing is setting up a circuit to operate a transistor at a desired operating point on its characteristic curve. Three bias networks for the common emitter amplifier are shown in figure 5.7.

In figure 5.7a the only path for DC bias current into the base is through R_B. V_{CC} is a power supply voltage which is generally greater than 10 V such that V_{PN} can be ignored. The DC voltage at the collector should be large enough to provide at least a 2 V drop between collector and emitter and clearly must be less than V_{CC}. In the absence of other circuit requirements, a convenient algebraic choice for V_C is $V_{CC}/2$. DC circuit analysis results in the following relative sizes of the two resistors:

$$R_B = 2h_{FE}R_C. \tag{5.19}$$

Although the circuit works reasonably well, the fact that h_{FE} is quite variable among samples leads to a bad design. A well-designed circuit should have an operating point that is less dependent on this parameter.

Figure 5.7b shows a network with the base-biasing resistor connected to the collector instead of V_{CC}. R_F acts as a negative feedback resistor since it feeds the collector current back into the base. Analysis give

$$R_F = h_{FE}R_C. \tag{5.20}$$

Therefore a change in h_{FE} has only half the effect of the previous design.

A more common bias stabilization technique employs a series resistor between the emitter and ground. This circuit has about the same sensitivity to changes in h_{FE} as the previous circuit.

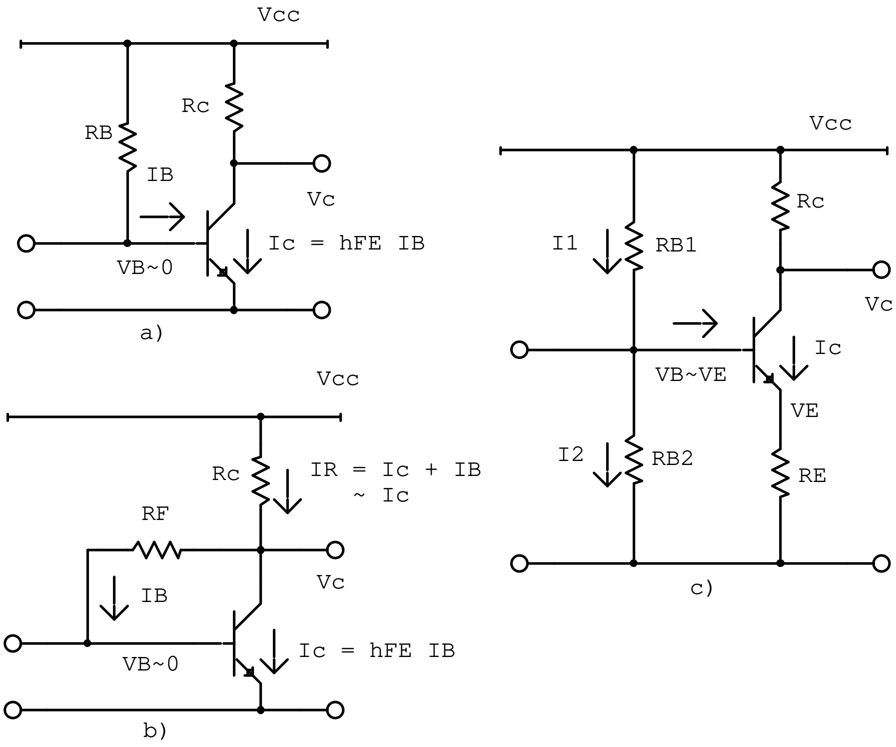


Figure 5.7: Bias circuits for the common emitter amplifier.

A further improvement can be made by introducing a second base-bias resistor as shown in figure 5.7c. The bias voltage is determined almost entirely by the two bias resistors. These biasing methods can also be used for the common collector and common base configurations.

5.2.2 Approximate AC Model

The circuit shown in figure 5.8a is the basic common emitter amplifier using the simplest biasing method. Because it is constant, the power supply voltage V_{CC} is an AC ground indistinguishable from the normal ground of the circuit. We can therefore relocate the upper end of R_B and R_C to the common ground line as shown in figure 5.8b. The transistor symbol is ideal and h_{ie} is shown explicitly as the input impedance and hence $i_S \neq i_B$.

5.2.3 The Basic CE Amplifier

We can now use the AC equivalent circuit to calculate the AC voltage gain between the base and collector. The base voltage is developed across the input resistor h_{ie} and $v_B = h_{ie} i_B$. The collector voltage can be similarity expressed as the voltage drop across the resistor R_C: $0 - v_C = R_C h_{fe} i_B$. Eliminating i_B, we can write the amplifier voltage transfer function between the base and collector as

$$\frac{v_C}{v_B} = -\frac{h_{fe} R_C}{h_{ie}}. \tag{5.21}$$

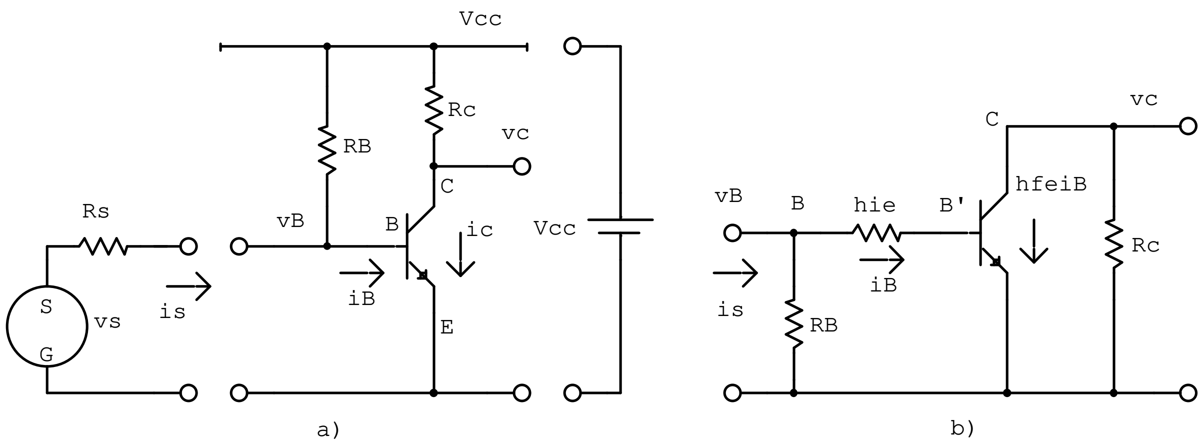


Figure 5.8: a) Basic CE amplifier and b) AC equivalent circuit drawn using an ideal transistor symbol with h_{ie} shown explicitly.

The minus sign indicates that the voltage signal at the collector is 180^o out of phase with the signal at the base.

The input impedance to this amplifier circuit is just the parallel combination of R_B and h_{ie}, and since h_{ie} is usually much smaller than R_B, the input impedance generally reduces to just the input impedance of the transistor itself, namely, h_{ie}. The circuit output impedance is the collector resistor R_C.

The high-frequency operation of the common emitter amplifier is limited by the parasitic capacitance between the collector and base. This capacitance provides a path by which the large and inverted signal at the collector drives a feedback current into the base. The base-to-collector voltage gain of this amplifier looks like a low-pass filter.

5.2.4 CE Amplifier with Emitter Resistor

The CE amplifier is often constructed with an emitter resistor R_E as shown in figure 5.9. This resistor provides a form of negative feedback that can be used to stabilize both the DC operating point and the AC gain. It can be shown that the voltage transfer function across the transistor is

$$\frac{v_C}{v_B} = -A = -\frac{h_{fe}R_C}{h_{ie} + h_{fe}R_E}. \tag{5.22}$$

If $h_{fe}R_E \gg h_{ie}$, the gain becomes independent of the hybrid parameters:

$$\frac{v_C}{v_B} = -A = -\frac{R_C}{R_E}. \tag{5.23}$$

Because it is unaffected by variations in the hybrid parameters, this result is valid even for a large-amplitude signal.

The input resistance can be shown to be $R_{in} = h_{fe}R_E$. Since h_{ie} is small, it can usually be neglected whenever the emitter impedance is more than a few hundred ohms.

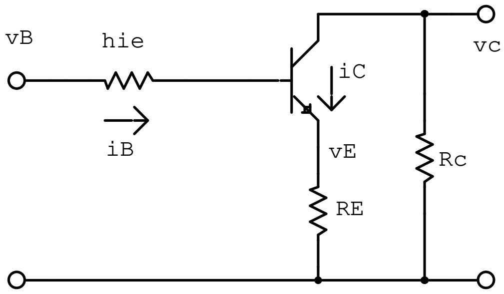


Figure 5.9: CE amplifier with emitter resistor.

For small input signals it is often desirable to retain the large voltage gain of the basic CE amplifier even though an emitter resistor is used for DC stability. This can be done if a large capacitor C_E is used to bypass the AC signal around the emitter resistor. C_E shorts out the emitter bias resistor R_E for AC signals. The magnitude of the resulting transfer function is similar to a high-pass filter, with R_E setting the gain ($A = R_C/R_E$) at low frequencies and the capacitor maximizing the gain ($A = h_{fe}R_C/h_{ie}$) at high frequencies.

Example: *Determine values for R_B and R_C that will yield the operating point shown in the circuit in figure 5.10 ($V_{CC} = +20\ V$) under the assumption that:*

1. $V_{BE} = 0$.
   $V_{BE} = 0 \Rightarrow V_B = 0$.
   $I_B = \frac{V_{CC}}{R_B} = \frac{I_C}{h_{FE}}$.
   Therefore

$$R_B = h_{FE}\frac{V_{CC}}{I_C} = \frac{100 \times 20}{1 \times 10^{-3}} = 2 \times 10^6 \Omega \qquad (5.24)$$
$$= 2M\Omega. \qquad (5.25)$$

$$R_C = \frac{V_{CC} - V_C}{I_C} = \frac{20 - 10}{10^{-3}} = 10^4 \Omega \qquad (5.26)$$
$$= 10k\Omega. \qquad (5.27)$$

2. $V_{BE} = 0.6\ V$.
   $V_{BE} = 0.6V \Rightarrow V_B = 0.6V$.
   $I_B = \frac{V_{CC} - V_B}{R_B} = \frac{I_C}{h_{FE}}$.
   Therefore

$$R_B = h_{FE}\frac{V_{CC} - V_B}{I_C} = \frac{100 \times (20 - 0.6)}{1 \times 10^{-3}} \qquad (5.28)$$
$$= 1.94M\Omega. \qquad (5.29)$$

$$R_C = \frac{V_{CC} - V_C}{I_C} \tag{5.30}$$
$$= 10k\Omega. \tag{5.31}$$

3. *Repeat both calculations for $h_{FE} = 80$.*
   For $h_{FE} = 80$, $R_C = 10k\Omega$ remains unchanged.
   $V_{BE} = 0 \Rightarrow R_B = \frac{80\times 20}{1\times 10^{-3}} = 1.6M\Omega$.
   $V_{BE} = 0.6V \Rightarrow = \frac{80(20-0.6)}{1\times 10^{-3}} = 1.55M\Omega$.

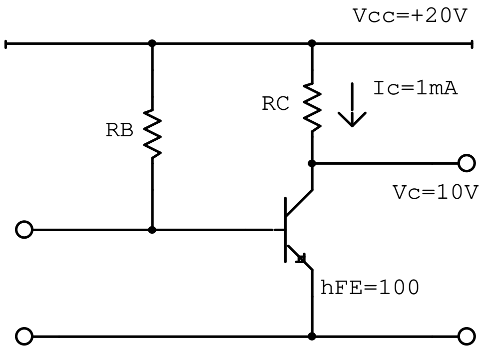


Figure 5.10: Example transistor circuit with a single bias transistor.

Example:

1. *If $h_{FE} = 100$, determine an expression for the base-biasing resistor R_B that will result in a DC operating point $V_C = V_{CC}/2$ for the circuit in figure 5.11.*
   Now $h_{FE} = 100$. The voltage drop across the bias resistor is $V_{CC} = R_B I_1 + 100RI_2$. Charge conservation ($I_1 = I_2 + I_B$) gives

$$V_{CC} = R_B(I_2 + I_B) + 100RI_2 \tag{5.32}$$
$$= R_B I_B + (R_B + 100R)I_2. \tag{5.33}$$

The voltage at the base is $V_B = 100RI_2$. Neglecting the V_{PN} voltage drop gives

$$V_B \approx V_E = R(I_C + I_C). \tag{5.34}$$

Eliminating V_B gives $I_2 = \frac{I_C + I_B}{100}$. Using $I_C = h_{FE} I_B \Rightarrow I_B = \frac{I_C}{h_{FE}}$ gives

$$I_2 = \frac{1 + 1/h_{FE}}{100} I_C. \tag{5.35}$$

Substituting equation 5.35 into equation 5.33 gives

$$V_{CC} = \left(\frac{R_B}{h_{FE}} + (R_B + 100R)\frac{1 + 1/h_{FE}}{100}\right) I_C. \tag{5.36}$$

The voltage drop across the collector resistor is

$$V_{CC} - V_C = 5RI_C \tag{5.37}$$
$$V_{CC} - V_{CC}/2 = V_{CC}/2 = 5RI_C. \tag{5.38}$$

Therefore

$$10R = \frac{R_B}{h_{FE}} + (R_B + 100R)\frac{1 + 1/h_{FE}}{100} \tag{5.39}$$
$$= 0.01R_B + 0.0101R_B + 1.01R \tag{5.40}$$
$$R_B = \frac{8.99}{0.0201}R = 447R \tag{5.41}$$
$$= 447R. \tag{5.42}$$

2. *If the circuit is built with the R_B just found, what will be the operating point if $h_{FE} = 50$?*
   If $R_B = 447R$ and $h_{FE} = 50$, $V_{CC} - V_C = 5RI_C \Rightarrow I_C = \frac{V_{CC}-V_C}{5R}$.
   Substitution into equation 5.36 gives

$$\frac{5RV_{CC}}{V_{CC} - V_C} = \frac{R_B}{h_{FE}} + (R_B + 100R)\frac{1 + 1/h_{FE}}{100} \tag{5.43}$$
$$\frac{5}{1 - V_C/V_{CC}} = \frac{447}{50} + (447 + 100)\frac{1 + 1/50}{100} \tag{5.44}$$
$$= 14.5194 \tag{5.45}$$
$$V_C = \left(1 - \frac{5}{14.5194}\right)V_{CC} \tag{5.46}$$
$$= 0.66V_{CC}. \tag{5.47}$$

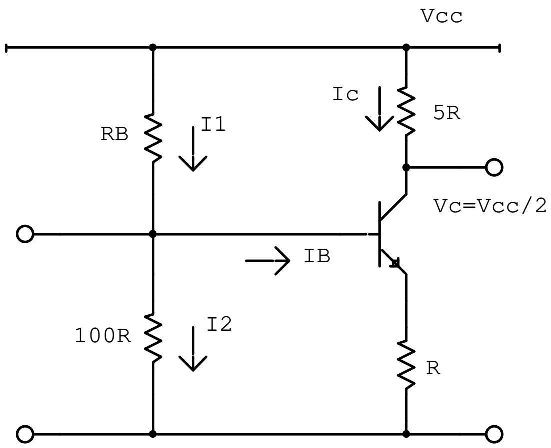


Figure 5.11: Example transistor circuit with two bias resistors.

5.3 The Common Collector Amplifier

The common collector amplifier is also called the *emitter follower* amplifier because the output voltage signal at the emitter is approximately equal to the voltage signal input on the base. The amplifier's voltage gain is always less than unity, but it has a large current gain and is normally used to match a high-impedance source to a low-impedance load: the amplifier has a large input impedance and a small output impedance.

A typical common collector amplifier is shown in figure 5.12.

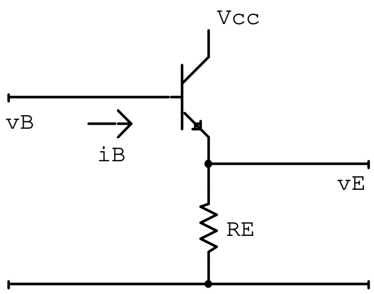


Figure 5.12: Basic common collector amplifier.

The voltage gain can be written as

$$\frac{v_E}{v_B} = \frac{h_{fe}R_E}{h_{ie} + h_{fe}R_E}. \tag{5.48}$$

The gain is thus in phase and slightly less than unity. The output impedance of the CC amplifier can be substantially less than the output impedance of the driving signal source.

5.4 The Common Base Amplifier

The common base amplifier is also known as the grounded base amplifier. This amplifier can produce a voltage gain but generates no current gain between the input and the output signals. It is normally characterized by a very small input impedance and an output impedance like the common emitter amplifier. Because the input and output currents are of similar size, the stray capacitance of the transistor is of less significance than for the common emitter amplifier. The common base amplifier is often used at high frequencies where it provides more voltage amplification than the other one-transistor circuits.

A common base circuit is shown in figure 5.13. Above the corner frequency the capacitor between base and ground on the circuit provides an effective AC ground at the transistor's base.

The voltage gain is given by

$$\frac{v_C}{v_E} = \frac{h_{fe}R_C}{h_{ie}}, \tag{5.49}$$

which is the same as the CE amplifier except for the lack of voltage inversion.

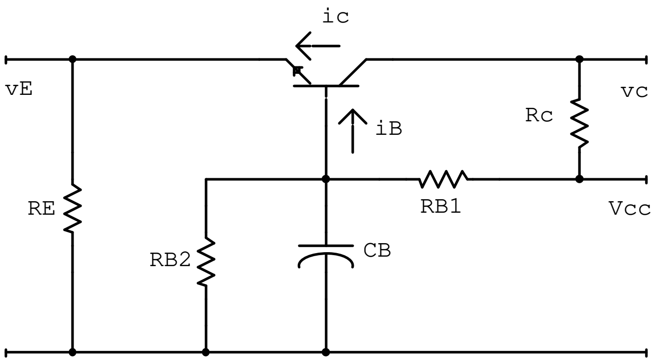


Figure 5.13: Basic common base amplifier.

The input impedance looking into the emitter ($R_{in} = h_{ie}/h_{fe}$) is quite small. The output impedance of this circuit is never greater than R_C.

Because of its high-frequency response and small input impedance, this circuit is often used to receive high-frequency signals transmitted via a coaxial cable. For this purpose the input impedance of the amplifier is adjusted to match the distributed impedance of the coaxial cable – usually 50 to 75 Ω.

5.5 The Junction Field Effect Transistor (JFET)

Bipolar junction transistors have low input impedance, small high-frequency gain and are non-linear when $|V_{CE}| < 2$ V. The input impedance is naturally restricted by the forward-biased base-emitter junction. There are always problems due to the main charge carriers passing through the region where the majority carriers are of opposite polarity.

The junction field effect transistor (JFET) overcomes some of the problems of the bipolar junction transistor. JFETs come in two types: N-channel and P-channel, and are shown in figure 5.14.

The designation refers to the polarity of the majority charge carriers in the bar of semiconductor that connects the drain terminal D to the source terminal S. Since the channel is formed from a single-polarity (*unipolar*) material, its resistance is a function only of the geometry of the conducting volume and the conductivity of the material. The JFET operates with all PN junctions reverse-biased so as to obtain a high input impedance into the gate.

5.5.1 Principles of Operation

Figure 5.15 shows an N-channel JFET with DC bias voltage applied. Just as for a simple diode, the depletion region grows as the reverse bias across the PN junction is increased, thereby constricting the cross section of the conducting N-channel material and increasing the resistance of the channel. The major current I_D in the channel is caused by the applied voltage between the drain and source, V_{DS}, and is controlled by the applied voltage between the gate and source, V_{GS}.

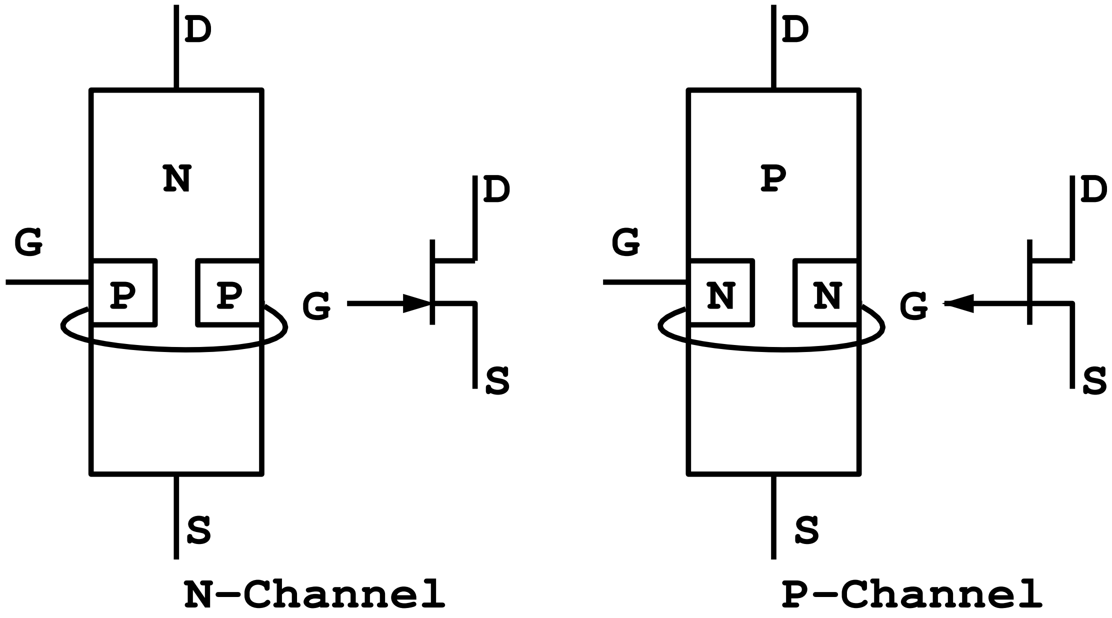


Figure 5.14: Basic geometry and circuit symbols of JFETS.

The JFET has two distinct modes of operation: the variable-resistance mode, and the *pinch-off* mode. In the variable-resistance mode the JFET behaves like a resistor whose value is controlled by V_{GS}. In the pinch-off mode, the channel has been heavily constricted with most of the drain-source voltage drop occuring along the narrow and therefore high-resistance part of the channel near the depletion regions.

The characteristic curves of a typical JFET are shown in figure 5.16. At small values of V_{DS} (in the range of a few tenths of a volt), the curves of constant V_{GS} show a linear relationship between V_{DS} and I_D. This is the variable-resistance region of the graph. As V_{DS} increases, each of the curves of constant V_{GS} enters a region of nearly constant I_D. This is the pinch-off region, where the JFET can be used as a linear voltage and current amplifier. At $V_{GS} = 0$ the current through the JFET reaches a maximum known as I_{DSS}, the current from Drain to Source with the gate Shorted to the source. If V_{GS} goes positive for this N-channel JFET, the PN junction becomes conducting and the JFET becomes just a forward-biased diode.

5.5.2 Small-Signal AC Model

The JFET characteristic curves can be described by an equation of the form

$$I_D = I_D(V_{GS}, V_{DS}), \tag{5.50}$$

where the function varies with the particular transistor. This expression yields the AC relationship

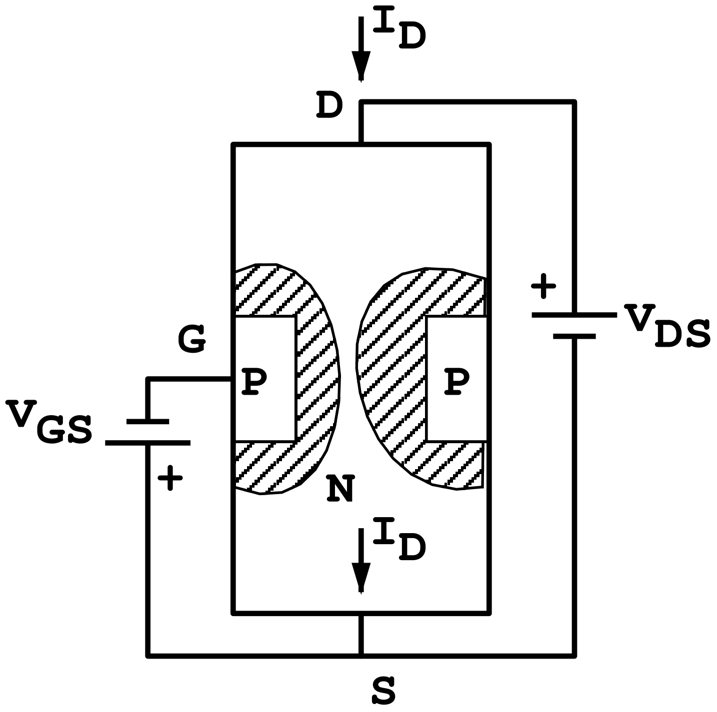


Figure 5.15: An N-channel JFET with DC bias voltages applied.

$$\vec{i}_D = \frac{\partial I_D}{\partial V_{GS}}\vec{v}_{GS} + \frac{\partial I_D}{\partial V_{DS}}\vec{v}_{DS}, \tag{5.51}$$

where the AC currents and voltages are complex but the partial derivatives evaluate to real numbers. In the pinch-off region the curves of constant V_{GS} are essential flat ($\partial I_D/\partial V_{DS} = 0$) and allow the equation to be written as

$$\vec{i}_D = g_m \vec{v}_{GS}, \tag{5.52}$$

where $g_m = \partial I_D/\partial V_{GS}$ is the transconductance.

5.6 JFET Common Source Amplifier

The common source configuration for a FET is similar to the common emitter bipolar transistor configuration, and is shown in figure 5.17. The common source amplifier can provide both a voltage and current gain. Since the input resistance looking into the gate is extremely large the current gain available from the FET amplifier can be quite large, but the voltage gain is generally inferior to that available from a bipolar device. Thus FET amplifiers are most useful with high output-impedance signal sources where a large current gain is the primary requirement. The source by-pass capacitor provides a low impedance path to ground

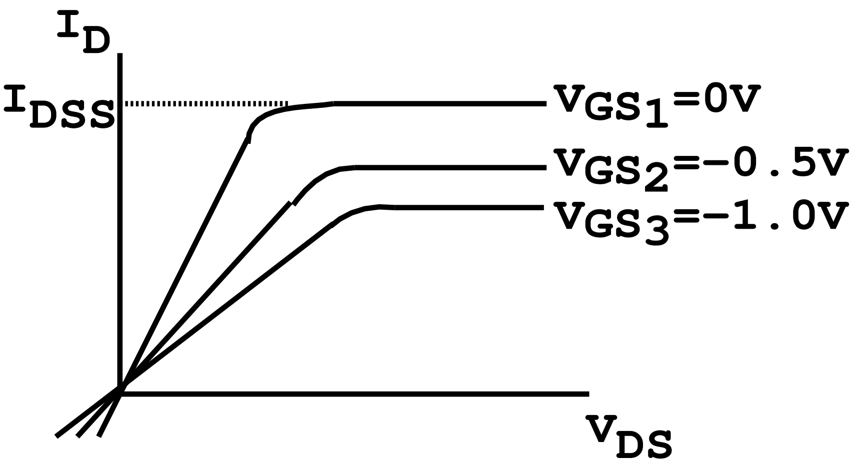


Figure 5.16: Characteristic curves of a typical N-channel JFET.

for high frequency components of v_{DS} and hence AC signals will not cause a swing in the bias voltage.

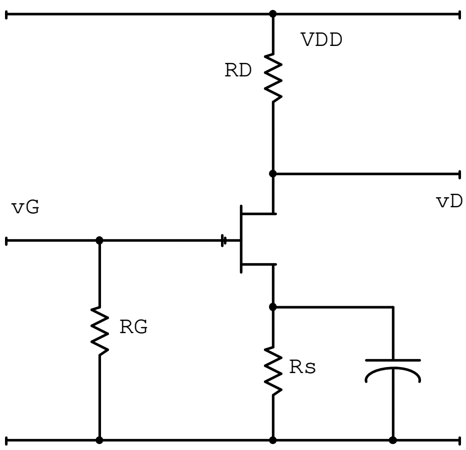


Figure 5.17: JFET common source amplifier.

Since the FET gate current is small we can make the approximations $i_S = i_D$ and $v_S = -v_{GS}$: the source is positive with respect to the gate for reverse-bias. Since at low frequencies we can ignore the capacitor the source voltage is given by

$$v_S = R_S i_S = R_S i_D. \tag{5.53}$$

Using the transconductance equation we can write

$$v_S = \frac{g_m R_S v_G}{1 + g_m R_S}. \tag{5.54}$$

With the approximation $i_S = i_D$ we can write the drain voltage as

$$v_D = -\frac{v_S R_D}{R_S}. \tag{5.55}$$

The voltage gain is thus

$$\frac{v_D}{v_G} = -A = -\frac{g_m R_D}{1 + g_m R_S}. \tag{5.56}$$

If $g_m R_S \gg 1$, this reduces to

$$\frac{v_D}{v_G} = -A = -\frac{R_D}{R_S}. \tag{5.57}$$

5.7 JFET Common Drain Amplifier

The common drain FET amplifier is similar to the common collector configuration of the bipolar transistor. A general common drain JFET amplifier, self-biased, is shown in figure 5.18. This configuration, which is sometimes known as a source follower, is characterized by a voltage gain of less than unity, and features a large current gain as a result of having a very large input impedance and a small output impedance.

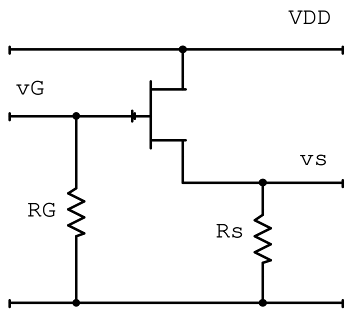


Figure 5.18: JFET common drain amplifier.

Using AC circuit analysis

$$\begin{aligned} i_D &= g_m v_{GS} \quad \text{and} \qquad (5.58)\\ \frac{v_S}{R_S} &= g_m(v_G - v_S). \qquad (5.59)\end{aligned}$$

The voltage gain between the gate and source is

$$\frac{v_S}{v_G} = \frac{g_m R_S}{1 + g_m R_S}. \tag{5.60}$$

If $g_m R_S \gg 1$, $v_S = v_G$ and we have a voltage follower.

5.8 The Insulated-Gate Field Effect Transistor

The insulated-gate FET, also known as a metal oxide semiconductor field effect transistor (MOSFET), is similar to the JFET but exhibits an even larger resistive input impedance due to the thin layer of silicon dioxide that is used to insulate the gate from the semiconductor channel. This insulating layer forms a capacitive coupling between the gate and the body of the transistor. The consequent lack of an internal DC connection to the gate makes the device more versatile than the JFET, but it also means that the insulating material of the capacitor can be easily damaged by the internal discharge of static charge developed during normal handling.

The MOSFET is widely used in large-scale digital integrated circuits where its high input impedance can result in very low power consumption per component. Many of these circuits feature bipolar transistor connections to the external terminals, thereby making the devices less susceptible to damage.

The MOSFET comes in four basic types, N-channel, P-channel, depletion and enhancement. The configuration of an N-channel, depletion MOSFET is shown in figure 5.19a. Its operation is similar to the N-channel JFET discussed previously: a negative voltage placed on the gate generates a charge depleted region in the N-type material next to the gate, thereby reducing the area of the conduction channel between the drain and source. However, the mechanism by which the depletion region is formed is different from the JFET. As the gate is made negative with respect to the source, more positive carriers from the P-type material are drawn into the N-channel, where they combine with and eliminate the free negative charges. This action enlarges the depletion region towards the gate, reducing the area of the N-channel and thereby lowering the conductivity between the drain and source. For negative applied gate-source voltages the observed effect is much like a JFET, and g_m is also about the same size.

However, since the MOSFET gate is insulated from the channel, positive gate-source voltages may also be applied without losing the FET effect. Depending on the construction details, the application of a positive gate-source voltage to a depletion-type MOSFET can repel the minority positive carriers in the depleted portion of the N-channel back into the P-type material as discussed below, thereby enlarging the channel and reducing the resistance. If the device exhibits this behaviour, it is known as an enhancement-depletion MOSFET.

A strictly enhancement MOSFET results from the configuration shown in figure 5.19b. Below some threshold of positive gate-source voltage, the connecting channel of N-type material between the drain and source is completely blocked by the depletion region generated by the PN junction. As the gate-source voltage is made more positive, the minority positive carriers are repelled back into the P-type material, leaving free negative charges behind. The effect is to shrink the depletion region and increase the conductivity between the drain and source.

5.9 Power MOSFET Circuits

Traditionally, MOSFET devices have had the drain-to-source current confined to a thin planar volume of silicon lying parallel to the gate. The limited cross-sectional area of material

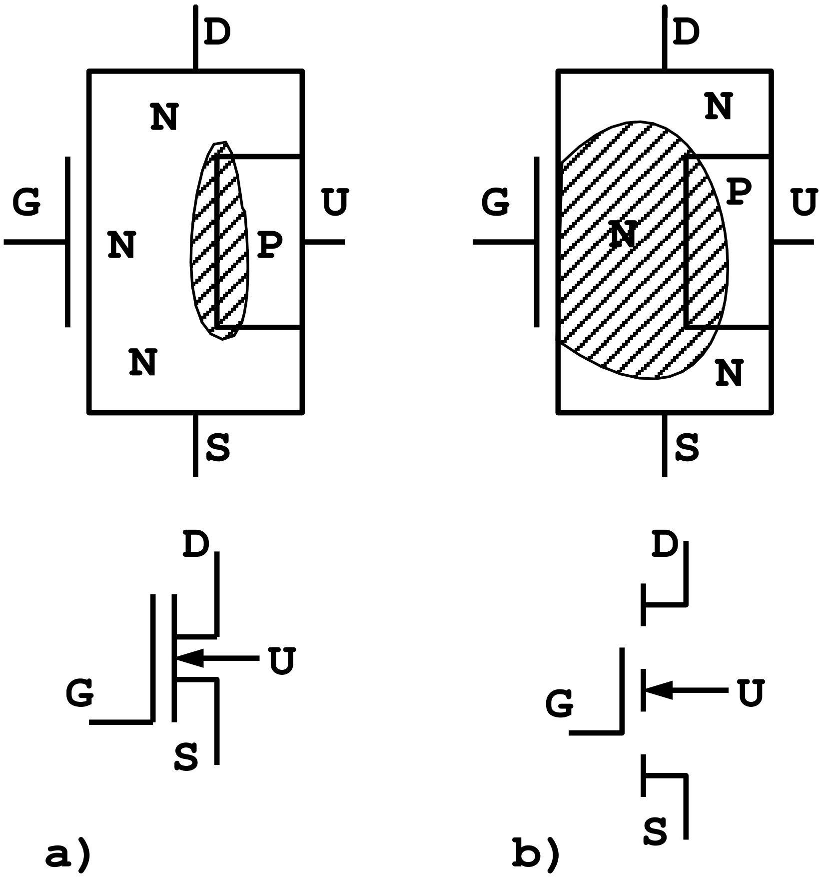


Figure 5.19: a) Depletion or depletion-enhancement type MOSFET and b) enhancement type MOSFET.

thus available for conduction effectively limits the power-handling capability of MOSFET devices to less than 1 W. More recently, new designs and manufacturing techniques have been developed to produce a more complicated, three-dimensional gate structure. These transistors are identified by various manufactures as HEXFET, VMOS, or DMOS, depending on the geometry of the gate structure: respectively hexagonal, V-shaped, or D-shaped. They feature power dissipations exceeding 100 W and excellent high-frequency operation. In contrast to the normal MOSFET, these devices have a much larger forward transconductance. These devices thus feature very high current gain at both high frequency and high power, a combination that is hard to obtain with traditional bipolar power transistors.

5.10 Multiple Transistor Circuits

Integrated circuit technology has largely eliminated the need to fabricate multiple transistor circuits from discrete transistors.

5.10.1 Coupling Between Single Transistor Stages

Quite often the single-transistor amplifier discussed in the previous lectures does not provide enough gain for an application, or more often, it does not combine gain with the desired input and output impedance characteristics. Perhaps the most obvious solution (but generally not the best) is to connect several single-transistor amplifiers, or stages, in tandem one after the other. Because of DC biasing considerations, it is usually not practical to connect the output of one stage directly to the input of another; some kind of coupling device must be used that permits a change in the DC level between two stages.

A possible circuit features capacitor coupling between single-transistor stages. The inter-stage coupling capacitor allows the following transistor to be DC biased without concern for the DC component of the driving signal. Thus the DC analysis of the two transistor stages is separated into two distinct problems.

5.10.2 Darlington and Sziklai Connections

Two bipolar transistors in either the Darlington or Sziklai connection can be used as a single, high gain, transistor. These circuits have AC current gains on the order of h_{fe}^2, providing high amplification in a single stage.

The arrangement of two NPN transistors shown in figure 5.20a is known as the Darlington connection. The three unconnected terminals, the base of Q_1 and the collector and emitter of Q_2, behave like a single transistor with current gain $h_{fe_1}h_{fe_2}$ and an overall base to emitter DC voltage drop of $2V_{PN}$. Two transistors in the Darlington connection can be purchased in a single three-terminal package.

A similar circuit result can be obtained with the Sziklai connection of figure 5.20b. Because it uses one transistor of each polarity (NPN and PNP), this connection is also known as the complementary Darlington. The combination again results in a three-terminal device that behaves like a single high-current-gain transistor. The overall circuit behaves like a transistor of the same polarity as Q_1.

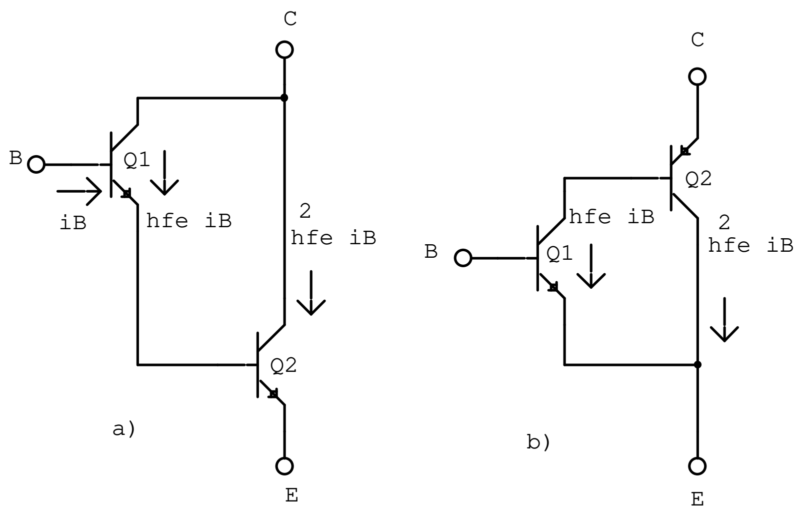
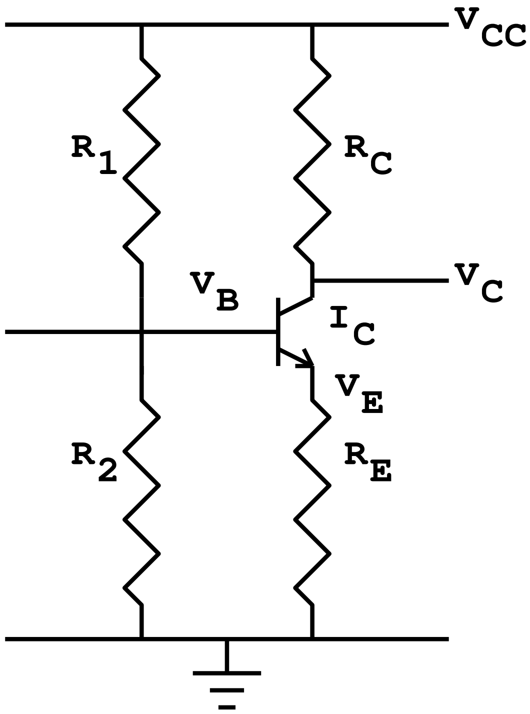


Figure 5.20: a) The Darlington connection of two transistors to obtain higher current gain and b) the Sziklai connection of an NPN and PNP transistor to obtain the equivalent of a high-current-gain NPN.

5.11 Problems

1. Consider the common-emitter amplifier shown below with values $V_{CC} = 12$ V, $R_1 = 47$ kΩ, $R_2 = 12$ kΩ, $R_C = 2.7$ kΩ, $R_E = 1$ kΩ, and a forward-bias voltage drop across the base-emitter junction of 0.7 V. Calculate approximate values for V_B, V_E, I_C, V_C, and the voltage gain. Using the measured h parameters $h_{ie} = 3600$ Ω and $h_{fe} = 150$, calculate the input impedance, base current, and voltage gain. Compare your calculated voltage gain with your approximation.



Chapter 6

Operational Amplifiers

The operational amplifier (op-amp) was designed to perform mathematical operations. Although now superseded by the digital computer, op-amps are a common feature of modern analog electronics.

The op-amp is constructed from several transistor stages, which commonly include a differential-input stage, an intermediate-gain stage and a push-pull output stage. The differential amplifier consists of a matched pair of bipolar transistors or FETs. The push-pull amplifier transmits a large current to the load and hence has a small output impedance.

The op-amp is a linear amplifier with $V_{\rm out} \propto V_{\rm in}$. The DC open-loop voltage gain of a typical op-amp is 10^3 to 10^6. The gain is so large that most often feedback is used to obtain a specific transfer function and control the stability.

Cheap IC versions of operational amplifiers are readily available, making their use popular in any analog circuit. The cheap models operate from DC to about 20 kHz, while the high-performance models operate up to 50 MHz. A popular device is the 741 op-amp which drops off 6 dB/octave above 5 Hz. Op-amps are usually available as an IC in an 8-pin dual, in-line package (DIP). Some op-amp ICs have more than one op-amp on the same chip.

Before proceeding we define a few terms:

linear amplifier – the output is directly proportional to the amplitude of input signal.

open-loop gain, A – the voltage gain without feedback ($\approx 10^5$).

closed-loop gain, G – the voltage gain with negative feedback (approximation to $\mathbf{H}(j\omega)$).

negative feedback – the output is connected to the inverting input forming a feedback loop (usually through a *feedback resistor* R_F).

6.1 Open-Loop Amplifiers

Figure 6.1a show a complete diagram of an operational amplifier. A more common version of the diagram is shown in figure 6.1b, where missing parts are assumed to exist. The inverting input means that the output signal will be 180^0 out of phase with the input applied to this terminal. On the diagram $V_{++} \equiv +V_{CC} = +15$ V (DC) and $V_{--} \equiv -V_{CC} = -15$ V (DC).

V_{CC} is typically, but not necessarily, ± 15 V. The positive and negative voltages are necessary to allow the amplification of both positive and negative signals without special biasing.

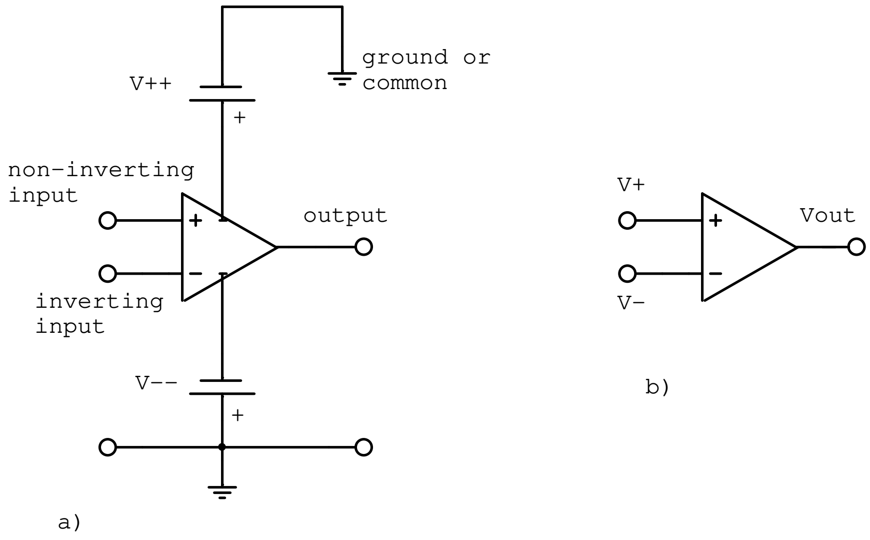


Figure 6.1: a) Complete diagram of an operation amplifier and b) common diagram of an operation amplifier.

For a linear amplifier (cf. a differential amplifier) the open-loop gain is

$$\vec{v}_{\text{out}} = \mathbf{A}(j\omega)(\vec{v}_+ - \vec{v}_-). \tag{6.1}$$

The open-loop gain can be approximated by the transfer function

$$\mathbf{A}(j\omega) = A_0 \mathbf{H}_{\text{low}}(j\omega), \tag{6.2}$$

where A_0 is the DC open-loop gain and $\mathbf{H}_{\text{low}}$ is the transfer function of a passive low-pass filter. We can write

$$\mathbf{A}(j\omega) = \frac{A_0}{1 + j\omega/\omega_c}, \tag{6.3}$$

where $A_0 \approx 2 \times 10^5$ and $f_c \approx 5$ Hz.

Two conditions must be satisfied for linear operation:

1. The input voltage must operate within the bias voltages:
   $-V_{CC}/A_0 \leq (v_+ - v_-) \leq +V_{CC}/A_0$.

2. For no clipping the output voltage swing must be restricted to
   $-V_{CC} \leq v_{\text{out}} \leq +V_{CC}$.

6.2 Ideal Amplifier Approximation

The following are properties of an ideal amplifier, which to a good approximation are obeyed by an operational amplifier:

1. large forward transfer function,
2. virtually nonexistent reverse transfer function,
3. large input impedance, $\mathbf{Z}_{\text{in}} \to \infty$ (any signal can be supplied to the op-amp without loading problems),
4. small output impedance, $\mathbf{Z}_{\text{out}} \to 0$ (the power supplied by the op-amp is not limited),
5. wide bandwidth, and
6. infinite gain, $A \to \infty$.

If these approximations are followed two rules can be used to analyze op-amp circuits:

Rule 1: The input currents $\mathbf{I}_+$ and $\mathbf{I}_-$ are zero, $\mathbf{I}_+ = \mathbf{I}_- = \mathbf{0}$ ($\mathbf{Z}_{\text{in}} = \infty$).

Rule 2: The voltages $\mathbf{V}_+$ and $\mathbf{V}_-$ are equal, $V_+ = V_-$ ($A = \infty$).

To achieve these rules requires negative feedback.

Feedback is used to control and stabilize the amplifier gain. The open-loop gain is too large to be useful since noise will causes the circuit to clip. Stabilization is obtained by feeding the output back into the input (closed negative feedback loop). In this way the closed-loop gain does not depend on the amplifier characteristics.

6.2.1 Non-inverting Amplifiers

Figure 6.2 shows a non-inverting amplifier, sometimes referred to as a *voltage follower*.

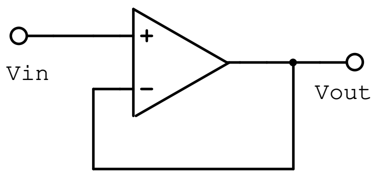


Figure 6.2: Non-inverting, unity-gain amplifier.

Applying our rules to this circuit we have

$$V_+ = V_- \Rightarrow V_{\text{in}} = V_{\text{out}}. \tag{6.4}$$

$$I_+ = I_- = 0 \Rightarrow R_{\text{in}} = \infty. \tag{6.5}$$

The amplifier gives a unit closed-loop gain, $\mathbf{G}(j\omega) = 1$, and does not change the sign of the input signal (no phase change).

This configuration is often used to buffer the input to an amplifier since the input resistance is high, there is unit gain and no inversion. The *buffer amplifier* is also used to isolate a signal source from a load.

Often a feedback resistor is used as shown in figure 6.3.

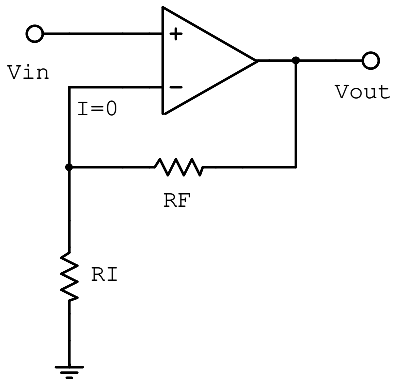


Figure 6.3: Non-inverting amplifier with feedback.

For this circuit

$$V_+ = V_- \Rightarrow V_{\text{in}} = \frac{R_I}{R_I + R_F} V_{\text{out}}. \tag{6.6}$$

The gain is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_I + R_F}{R_I} = 1 + \frac{R_F}{R_I} \quad \text{and} \tag{6.7}$$

$$\mathbf{G}(j\omega) = 1 + \frac{R_F}{R_I}. \tag{6.8}$$

$$\tag{6.9}$$

6.2.2 Inverting Amplifiers

An inverting amplifier is shown in figure 6.4. Analysis of the circuit gives

$$\frac{V_{\text{in}} - V_-}{R_I} = \frac{V_- - V_{\text{out}}}{R_F}. \tag{6.10}$$

Since $V_+ = V_- = 0$ (V_- is at *virtual ground*),

$$\frac{-V_{\text{in}}}{R_I} = \frac{V_{\text{out}}}{R_F}. \tag{6.11}$$

The gain is

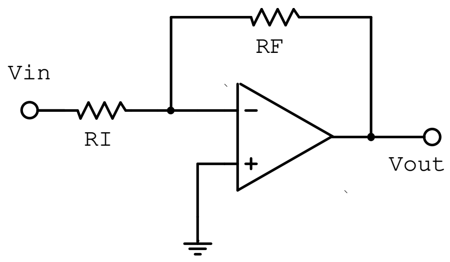


Figure 6.4: Inverting amplifier.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_F}{R_I} \quad \text{and} \tag{6.12}$$

$$\mathbf{G}(j\omega) = -\frac{R_F}{R_I}. \tag{6.13}$$

$$\tag{6.14}$$

The output is inverted with respect to the input signal.

A sketch of the frequency response of the inverting and non-inverting amplifiers are shown in figure 6.5.

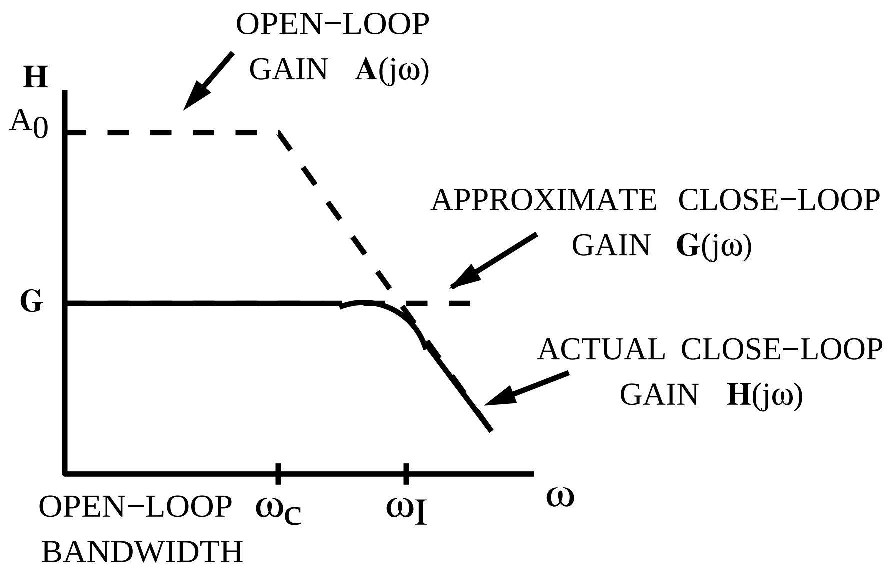


Figure 6.5: Inverting and non-inverting amplifier frequency response.

The input impedance of the inverting amplifier is $R_{\text{in}} = V_{\text{in}}/I$. Since $V_{\text{in}} - IR_I = 0$ we have $R_{\text{in}} = R_I$.

A better circuit for approximating an ideal inverting amplifier is shown in figure 6.6 The extra resistor is a current bias-compensation resistor. It reduces the current bias by eliminating non-zero current at the inputs.

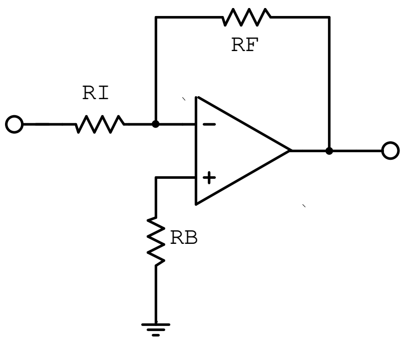


Figure 6.6: Inverting amplifier with bias compensation.

6.2.3 Mathematical Operations

Current Summing Amplifier

Consider the current-to-voltage converter shown in figure 6.7. Applying our ideal amplifier rules gives

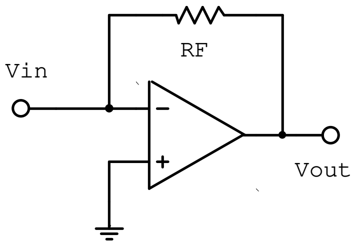


Figure 6.7: Current-to-voltage converter.

$$V_+ = V_- = 0 \Rightarrow 0 - V_{\text{out}} = IR_F. \tag{6.15}$$

Therefore $V_{\text{out}} = -IR_F$ and the circuit acts as a current-to-voltage converter.

Figure 6.8 shows several current sources driving the negative input of an inverting amplifier. Summing the current into the node gives

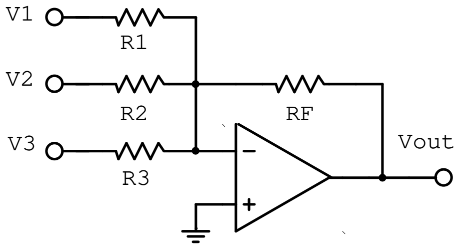


Figure 6.8: Current summing amplifier.

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -\frac{V_{\text{out}}}{R_F}. \tag{6.16}$$

Therefore

$$V_{\text{out}} = -\left(\frac{R_F}{R_1}\right) V_1 - \left(\frac{R_F}{R_2}\right) V_2 - \left(\frac{R_F}{R_3}\right) V_3. \tag{6.17}$$

If $R_1 = R_2 = R_3 (\equiv R)$, we have

$$V_{\text{out}} = -\frac{R_F}{R}(V_1 + V_2 + V_3), \tag{6.18}$$

and the output voltage is proportional to the sum of the input voltages.

For only two inputs and a constant reference voltage

$$V_{\text{out}} = -\frac{R_F}{R_I} V_{\text{in}} - \frac{R_F}{R_R} V_{\text{ref}}, \tag{6.19}$$

where the second term represents an offset voltage. This provides a convenient method for obtaining an output signal with any required voltage offset.

Differentiation Circuit

To obtain a differentiation circuit we replace the input resistor of the inverting amplifier with a capacitor as shown in figure 6.9.

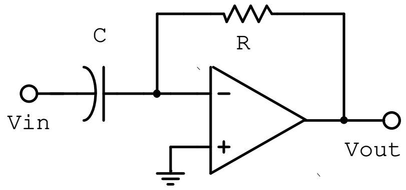


Figure 6.9: Differentiation circuit.

Replacing R_I with $Z_C = 1/j\omega C$ in the voltage gain gives

$$\mathbf{G}(j\omega) = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R}{Z_C} = -j\omega RC, \tag{6.20}$$

or

$$V_{\text{out}} = -j\omega RC V_{\text{in}} = -RC\frac{dV_{\text{in}}}{dt}. \tag{6.21}$$

Using $dV/dt = I/C$ gives

$$\frac{d(V_{\text{in}} - 0)}{dt} = \frac{1}{C}\frac{0 - V_{\text{out}}}{R} \tag{6.22}$$

and thus the same result as above.

The frequency response is shown in figure 6.10.

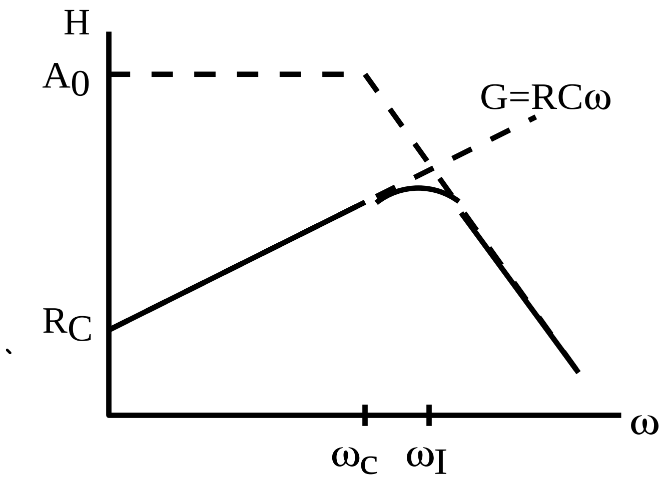


Figure 6.10: Differentiation circuit frequency response.

Integration Circuit

Integration is obtained by reverse the resistor and the capacitor as shown in figure 6.11. The capacitor is now in the feedback loop.

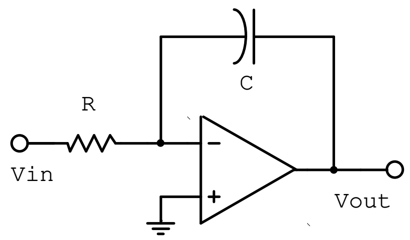


Figure 6.11: Integration circuit.

Analysis gives

$$\mathbf{G}(j\omega) = \frac{V_{\rm out}}{V_{\rm in}} = -\frac{Z_C}{R} = \frac{-1}{j\omega RC} \tag{6.23}$$

or

$$V_{\rm out} = \frac{-V_{\rm in}}{j\omega RC} = \frac{-1}{RC}\int V_{\rm in} dt. \tag{6.24}$$

Using $dV/dt = I/C$ gives

$$\frac{d(0 - V_{\rm out})}{dt} = \frac{1}{C}\frac{V_{\rm in} - 0}{R}. \tag{6.25}$$

and thus the same result as above.

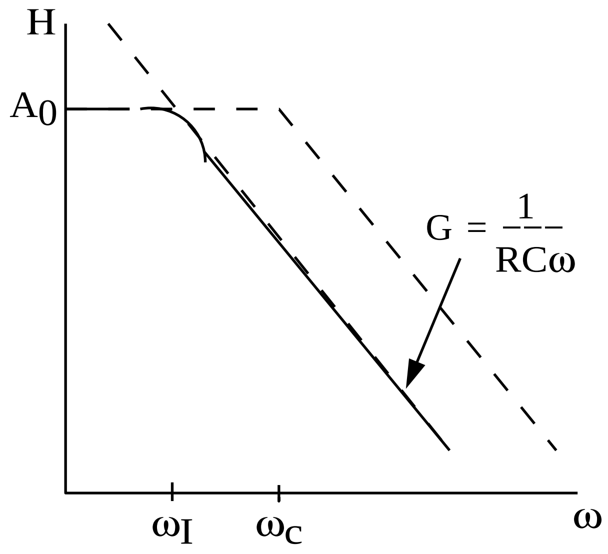


Figure 6.12: Integration circuit frequency response.

The frequency response is shown in figure 6.12.

We can combine the above inverting, summing, offset, differentiation and integration circuits to build an analog computer that can solve differential equations. However, today, the differentiators and integrators are mainly used to condition signals.

6.2.4 Active Filters

Filters often contain embedded amplifiers between passive-filter stages as shown in figure 6.13.

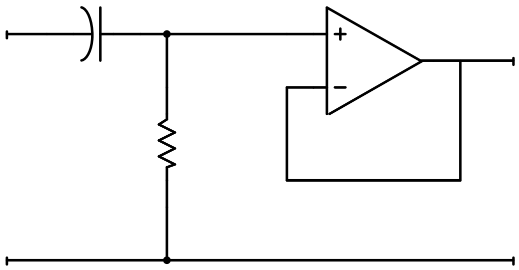


Figure 6.13: Buffer amplifier as part of active filter.

These filters have a limited performance since the poles are still real and hence the knees are not sharp. For example, a three stage high-pass filter with buffer amplifiers has a transfer function

$$\mathbf{G}(j\omega) = \frac{j\omega}{1 + j\omega/\omega_c}\frac{j\omega}{1 + j\omega/\omega_c}\frac{j\omega}{1 + j\omega/\omega_c} = \frac{-j\omega^3}{(1 + j\omega/\omega_c)^3}, \tag{6.26}$$

and only drops 18 db/octave.

For complex poles we must use either integrators or differentiators. Consider figure 6.14.

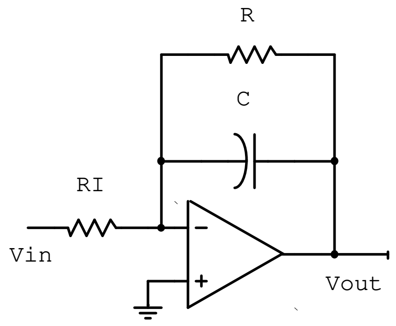


Figure 6.14: Active filter with complex poles.

The closed-loop gain is

$$\mathbf{G} = \frac{-Z_{RC}}{R_I} = -\frac{R/j\omega C}{R_I(R + 1/j\omega C)} = \frac{-R}{R_I(1 + j\omega RC)}. \tag{6.27}$$

By exchanging the input resistor for a capacitor we can change between a low-pass and high-pass filter.

General Feedback Elements

The feedback elements in an operation amplifier design can be more complicated than a simple resistor and capacitor. An interesting feedback element is the analog multiplier as defined in figure 6.15.

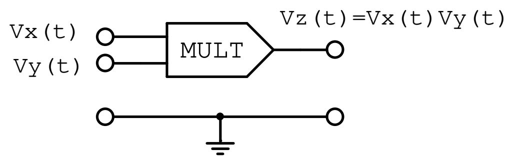


Figure 6.15: Five-terminal network that performs the multiplication operation on two voltage signals.

The multiplier circuit itself can be thought of as another op-amp with a feedback resistor whose value is determined by a second input voltage. Multiplication circuits with the ability to handle input voltages of either sign (four-quadrant multipliers) are available as integrated circuits and have a number of direct uses as multipliers. But when used in a feedback loop around an operational amplifier, other useful functional forms result.

The circuit of figure 6.16 gives an output that is the ratio of two signals, whereas the circuit of figure 6.17 yields the analog square-root of the input voltages.

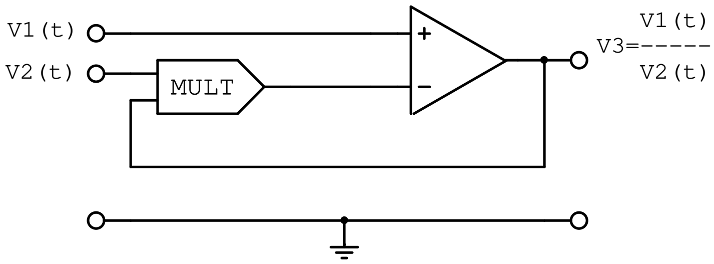


Figure 6.16: A multiplier as part of the feedback loop that results in the division operation.

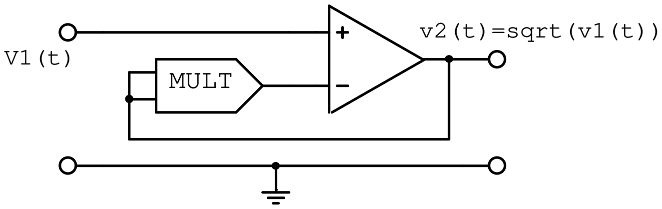


Figure 6.17: A multiplier as part of the feedback loop that results in the square-root operation.

6.2.5 Differential Amplifiers

The differential amplifier amplifies the difference between two input signals (−) and (+). This amplifier is also referred to as a differential-input single-ended output amplifier. It is a precision voltage difference amplifier, and forms the central basis of more sophisticated instrumentation amplifier circuits.

A differential amplifier is shown in figure 6.18. The voltage V_3 is given by (cf. voltage divider)

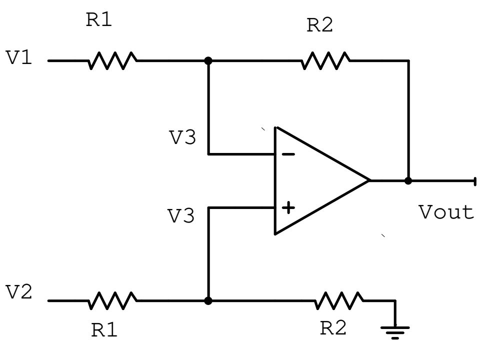


Figure 6.18: Differential amplifier.

$$V_3 = \frac{R_2}{R_1 + R_2} V_2, \tag{6.28}$$

and thus

$$\frac{V_1 - V_3}{R_1} = \frac{V_3 - V_{\rm out}}{R_2} \tag{6.29}$$

leads to

$$V_{\rm out} = \frac{R_2}{R_1}(V_2 - V_1). \tag{6.30}$$

The differential amplifier is usually limited in its performance by the low input impedance of $2R_1$. Two buffer amplifiers are commonly added to remove this limitation and form the simple instrumentation amplifier in figure 6.19.

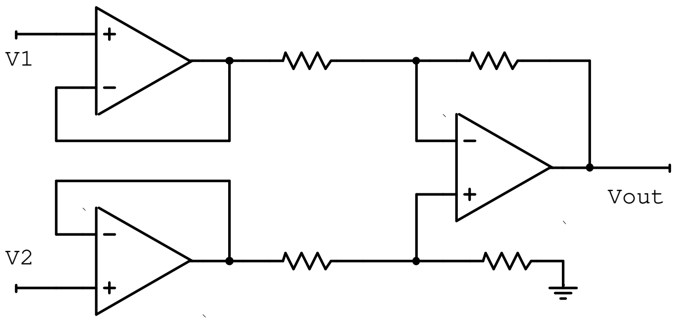


Figure 6.19: Instrumentation amplifier.

Example: *If the open-loop gain curve in figure 6.20 describes the amplifier shown, write an expression for* $\mathbf{V}_{\rm out}$ *when* $\mathbf{V}_{\rm in} = 10\cos(1000t)$ *mV.*
By definition

$$V_{out} = \mathbf{A}(j\omega)(V_+ - V_-). \tag{6.31}$$

Since V_- *is at ground and* $V_+ = V_{in}$*, we have* $V_{out} = \mathbf{A}(j\omega)V_{in}$.

$$\mathbf{A}(j\omega) = \frac{A_0}{1 + j\omega/\omega_C}, \tag{6.32}$$

where $A_0 = 2 \times 10^5$ *and* $\omega_C = 25$ *rad/s (4 Hz).*
Since $V_{in} = 10\cos(1000t)$ *mV* $\Rightarrow \omega = 1000$ rad/s.
Therefore

$$A = \frac{2 \times 10^5}{1 + j1000/25} = \frac{2 \times 10^5}{1 + 40j} = \frac{2 \times 10^5}{1 + 40^2}(1 - 40j), \tag{6.33}$$

$$|A| = \frac{2 \times 10^5}{\sqrt{1 + 40^2}} \approx \frac{2 \times 10^5}{40} = 1/2 \times 10^4, \tag{6.34}$$

$$\phi = \tan^{-1}\left(\frac{-40}{1}\right) = -88.6^o(-1.55rad), \tag{6.35}$$

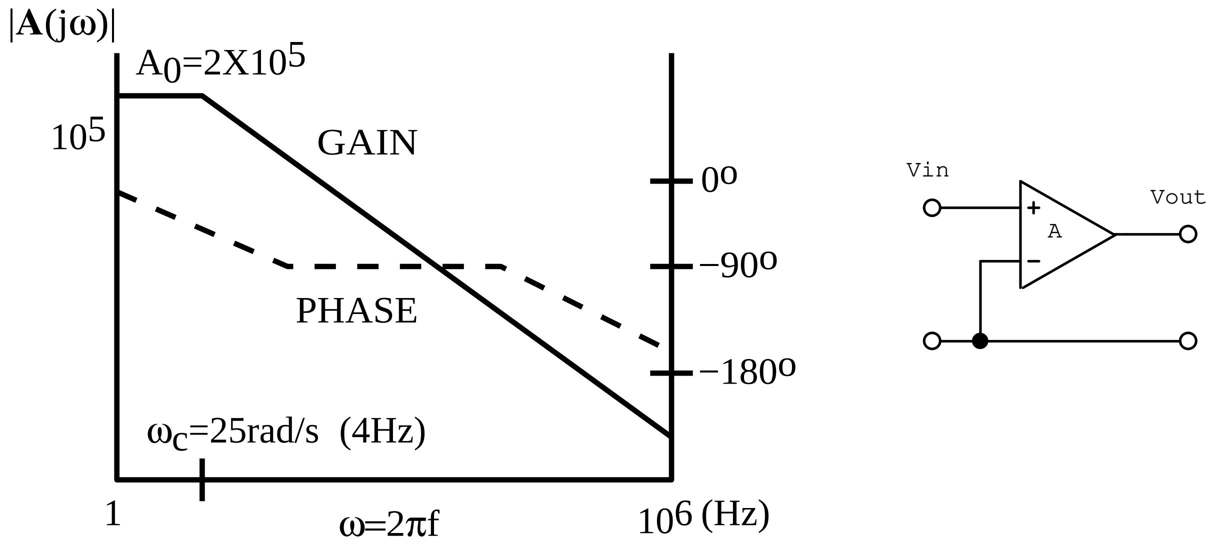


Figure 6.20: Open loop gain curve and amplifier.

and

$$
\begin{aligned}
V_{out} &= (0.5 \times 10^4) \times 10\cos(1000t) \times 10^{-3} e^{-j1.55} && (6.36)\\
&= 50 e^{j1000t} e^{-j1.55} && (6.37)\\
&= 50\cos(1000t - 1.55) && (6.38)\\
&\approx 50\cos(1000t)\ V. && (6.39)
\end{aligned}
$$

Example: *The variable resistor in the circuit in figure 6.21 provides a DC offset to the output voltage; a circuit of this type is often used to provide a zero output for some specific but nonzero input signal. What range of input voltage V_0 can be zeroed out by this circuit?*
The current flowing from the input to the output is

$$I = \frac{V_{in} - V_-}{10\ k\Omega} \quad \text{or} \quad I = \frac{V_- - V_{out}}{10\ k\Omega}. \qquad (6.40)$$

Therefore

$$
\begin{aligned}
V_{in} - V_- &= V_- - V_{out} && (6.41)\\
V_{out} &= 2V_- - V_{in} && (6.42)\\
&\approx 2V_+ - V_{in}. && (6.43)
\end{aligned}
$$

V_+ ranges from 0 to $\frac{10k\Omega}{10k\Omega+1000k\Omega}15\text{V} = \frac{15}{11}$ V.
Therefore V_{out} ranges from $V_{out} = -V_{in}$ to $V_{out} = \frac{30}{11}V - V_{in}$.
For $V_{out} = 0 \Rightarrow V_{in} = 0$ to $0 = 30/11 - V_{in}$ or $V_{in} = 30/11 = 2.7$ V.

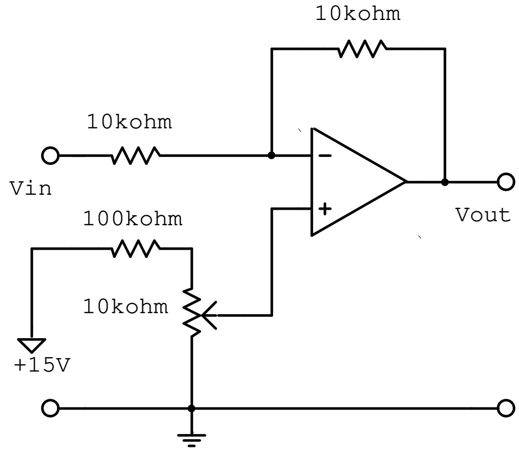


Figure 6.21: Circuit with DC offset.

The range of input singals that can be zeroed is

$$0 \leq V_{in} \leq 2.7\ V. \tag{6.44}$$

Example: *A two-input current summing amplifier can be used to shift the DC level of an AC signal. For the circuit shown below, determine the average value of the output signal if the input is* $V_{\text{in}} = 2\sin(6000t)\ V$.

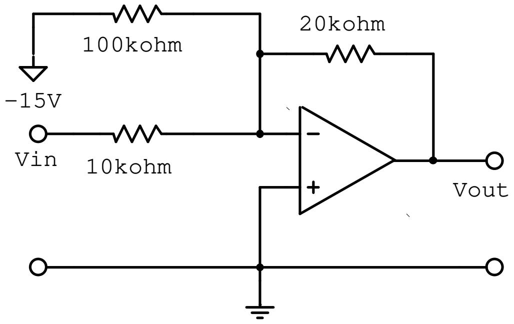


Figure 6.22: Two-input current summing amplifier.

The current sum into the node is

$$\frac{-15V - V_{-}}{100k\Omega} + \frac{V_{in} - V_{-}}{10k\Omega} = \frac{0 - V_{out}}{20k\Omega}. \tag{6.45}$$

since V_{-} *is at virtual ground* ($V_{-} = 0$).

$$V_{out} = 20k\Omega\left(\frac{15V}{100k\Omega} - \frac{V_{in}}{10k\Omega}\right) \tag{6.46}$$

$$= 3V - 2V_{in}. \tag{6.47}$$

$$\langle V_{out}\rangle = 3V - 2\langle V_{in}\rangle. \tag{6.48}$$

since $V_{in} = 2\sin(6000t)V$ $\langle V_{in}\rangle = 0$.
Therefore $\langle V_{out}\rangle = 3V$.

Example: *Assuming ideal operational amplifiers, determine* $\mathbf{G}(j\omega)$ *for each of the circuits below. Then determine the single-term approximations to the transfer function at various frequencies, sketch the resulting straight-line approximation to* $|\mathbf{G}|$, *and label all magnitudes, corners and slopes.*

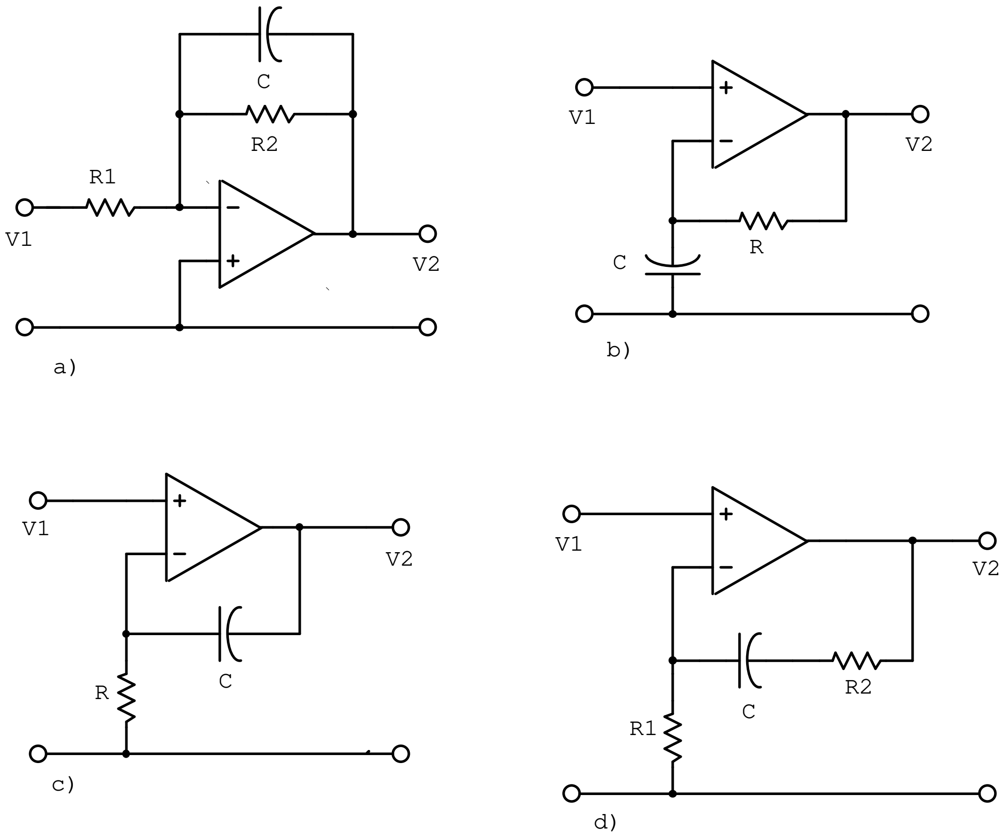


Figure 6.23: Amplifiers with a feedback capacitor.

a) *Since* V_- *is at virtual ground*

$$\frac{V_1 - 0}{R_1} = \frac{0 - V_2}{Z_F}, \tag{6.49}$$

where

$$Z_F = \frac{R_2/j\omega C}{R_2 + 1/j\omega C} = \frac{R_2}{1 + j\omega R_2 C} \tag{6.50}$$

$$\mathbf{G}(j\omega) = \frac{V_2}{V_1} = -\frac{Z_F}{R_1} = -\frac{R_2}{R_1}\frac{1}{1+j\omega R_2 C} \quad (6.51)$$
$$= -\frac{R_2}{R_1}\frac{1}{1+j\omega R_2 C}. \quad (6.52)$$

$\omega \to 0 \Rightarrow \mathbf{G} = -R_2/R_1$; $|\mathbf{G}| = R_2/R_1$.
$\omega \to \infty \Rightarrow \mathbf{G} = -1/jR_1 C\omega$; $|\mathbf{G}| = (1/R_1 C)\omega^{-1}$.
$\frac{R_2}{R_1} = \frac{1}{R_1 C\omega_C} \Rightarrow \omega_C = \frac{1}{R_2 C}$.

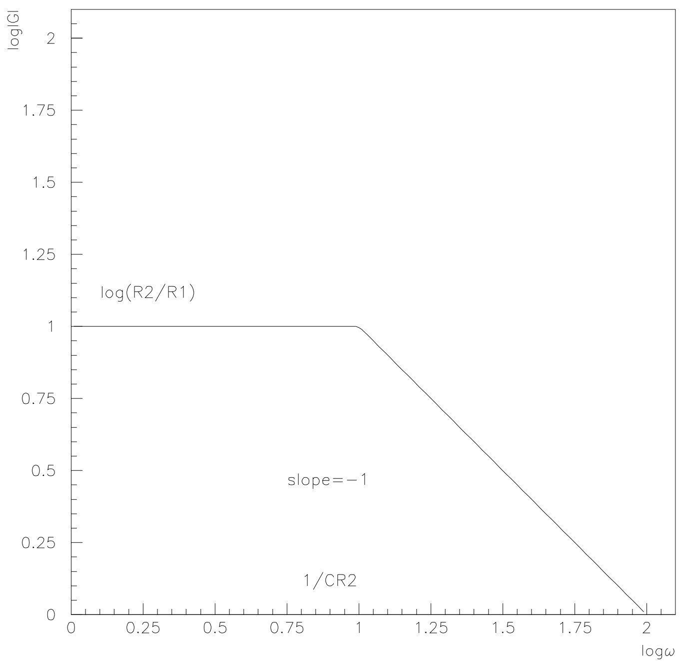


Figure 6.24: Straight-line approximation to $|\mathbf{G}|$ for amplifier a).

b)

$$\frac{V_2 - V_-}{R} = \frac{V_- - 0}{Z_C} \quad (6.53)$$
$$\frac{V_2 - V_+}{R} \approx \frac{V_+}{Z_C} \quad (6.54)$$
$$\frac{V_2 - V_1}{R} = \frac{V_1}{Z_C}. \quad (6.55)$$

Therefore $V_2 = V_1(R/Z_C + 1) = V_1(1 + j\omega CR)$

$$\mathbf{G}(j\omega) = \frac{V_2}{V_1} = 1 + j\omega RC. \quad (6.56)$$

$\omega \to 0 \Rightarrow \mathbf{G} = 1$; $|\mathbf{G}| = 1$.
$\omega \to \infty \Rightarrow \mathbf{G} = j\omega RC$; $|\mathbf{G}| = (RC)\omega^{+1}$.
$RC\omega_C = 1 \Rightarrow \omega_C = 1/RC$.

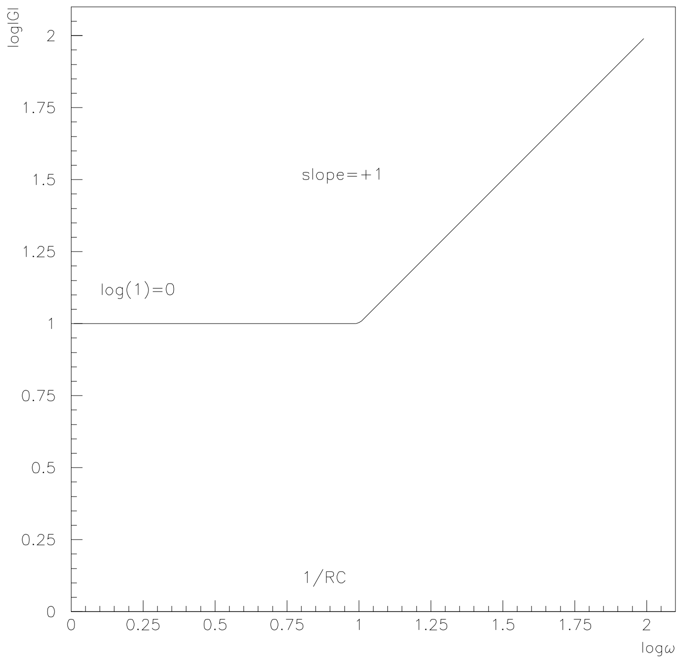


Figure 6.25: Straight-line approximation to $|\mathbf{G}|$ for amplifier b).

c)

$$\frac{V_2 - V_-}{Z_C} = \frac{V_- - 0}{R} \tag{6.57}$$

$$\frac{V_2 - V_+}{Z_C} \approx \frac{V_+}{R} \tag{6.58}$$

$$\frac{V_2 - V_1}{Z_C} = \frac{V_1}{R}. \tag{6.59}$$

Therefore

$$V_2 = \frac{Z_C}{R}V_1 + V_1 = \left(1 + \frac{1}{j\omega RC}\right)V_1 \tag{6.60}$$

$$\mathbf{G}(j\omega) = 1 + \frac{1}{j\omega RC}. \tag{6.61}$$

$\omega \to 0 \Rightarrow \mathbf{G} = 1/j\omega RC$; $|\mathbf{G}| = (1/RC)\omega^{-1}$.
$\omega \to \infty \Rightarrow \mathbf{G} = 1$; $|\mathbf{G}| = 1$.
$1 = 1/\omega_C RC \Rightarrow \omega_C = 1/RC$.

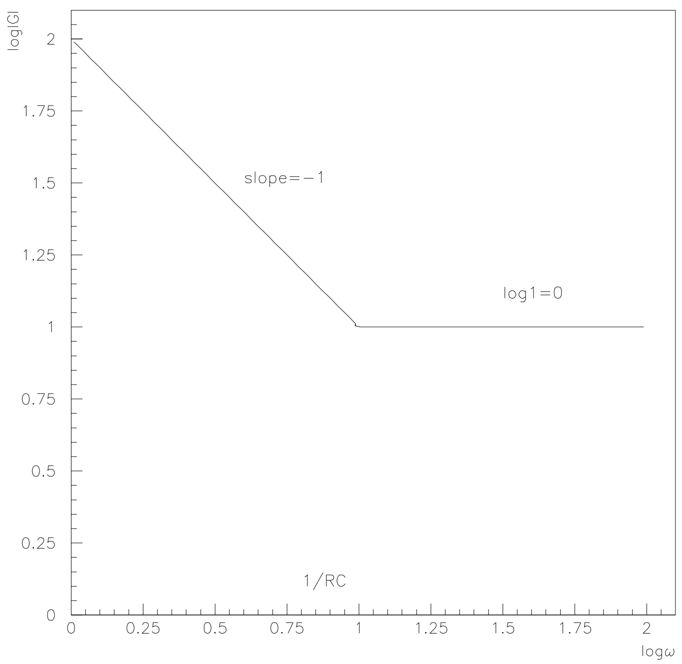


Figure 6.26: Straight-line approximation to $|\mathbf{G}|$ for amplifier c).

d)

$$\frac{V_2 - V_1}{Z_C + R_2} = \frac{V_- - 0}{R_1} \tag{6.62}$$

$$\frac{V_2 - V_1}{1/j\omega_C + R_2} = \frac{V_1}{R_1} \tag{6.63}$$

Therefore

$$V_2 = \frac{1/j\omega C + R_2}{R_1} V_1 + V_1 \tag{6.64}$$

$$\mathbf{G}(j\omega) = 1 + \frac{R_2}{R_1} + \frac{1}{j\omega R_1 C} \tag{6.65}$$

$\omega \to 0 \Rightarrow \mathbf{G} = 1/j\omega R_1 C$; $|\mathbf{G}| = (1/R_1 C)\omega^{-1}$.
$\omega \to \infty \Rightarrow \mathbf{G} = 1 + R_2/R_1$; $|\mathbf{G}| = 1 + R_2/R_1$.
$\frac{1}{R_1 C \omega_C} = 1 + \frac{R_2}{R_1} \to \omega_C = \frac{1}{CR_1 + CR_2}$.

6.3 Analysis Using Finite Open-Loop Gain

The infinite gain approximation is very useful but a more complete description is required if we are to understand the limitations of the op-amp. Real op-amps have a large but finite

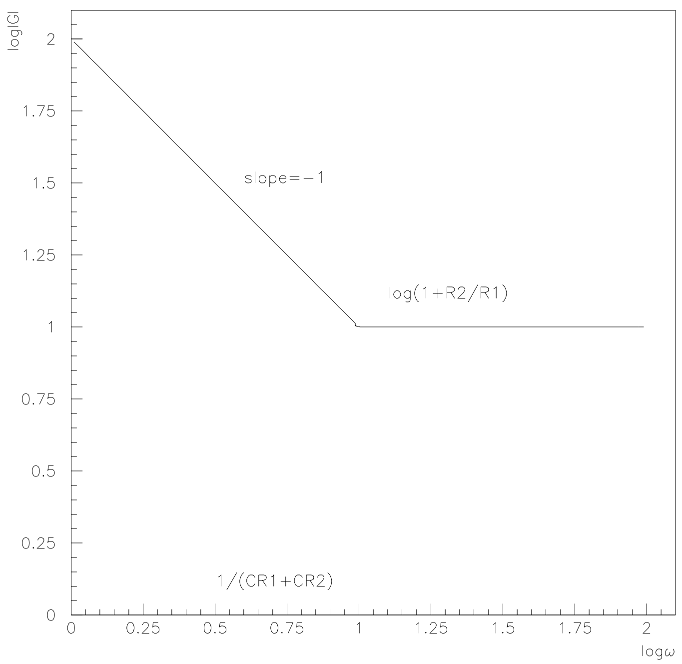


Figure 6.27: Straight-line approximation to $|\mathbf{G}|$ for amplifier d).

input impedance, small but non-zero output impedance and large but finite open-loop gain. They also have voltage and current asymmetries at the inputs. We will analyze some circuits using an finite open-loop gain and consider output impedance, input impedance, and voltage and current offsets.

6.3.1 Output Impedance

An op-amp will in general have a small resistive output impedance from the push-pull output stage. We will model the open-loop output impedance by adding a series resistor R_0 to the output of an ideal op-amp as shown in figure 6.28.

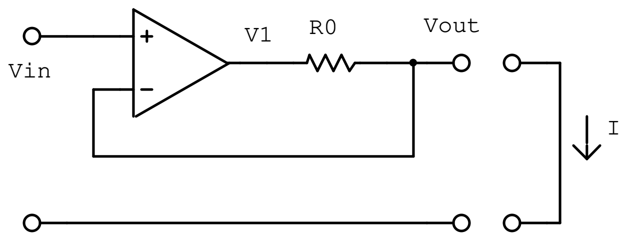


Figure 6.28: Real, current-limiting operational amplifier partially modeled by an ideal amplifier and an output resistor.

Assuming no current into the input terminals (unloaded), and hence no current through

R_0, we have $\mathbf{V}_1 = \mathbf{V}_{\mathrm{out}} = \mathbf{V}(\mathrm{open})$. Using the open-loop transfer function $\mathbf{V}_1 = \mathbf{A}(j\omega)(\mathbf{V}_{\mathrm{in}} - \mathbf{V}_{\mathrm{out}})$ we obtain

$$\mathbf{V}(\mathrm{open}) = \frac{\mathbf{A}(j\omega)}{1+\mathbf{A}(j\omega)}\mathbf{V}_{\mathrm{in}}. \tag{6.66}$$

Shorting a wire across the output gives $\mathbf{V}_{\mathrm{out}} = 0$ and hence

$$\mathbf{I}(\mathrm{short}) = \frac{\mathbf{V}_1}{R_0} \tag{6.67}$$

$$= \frac{\mathbf{A}(j\omega)}{R_0}\mathbf{V}_{\mathrm{in}}. \tag{6.68}$$

Using the standard definition for the impedance give

$$\mathbf{Z}_{\mathrm{out}} = \frac{\mathbf{V}(\mathrm{open})}{\mathbf{I}(\mathrm{short})} = \frac{R_0}{1+\mathbf{A}(j\omega)}. \tag{6.69}$$

If $\mathbf{A} \approx A_0 \gg 1$ than $Z_{\mathrm{out}} \approx R_0/A_0$, which is small as required of our infinite open-loop gain approximation.

We can now draw the impedance outside the feedback loop and use

$$\mathbf{A}(j\omega) = \frac{A_0}{1+j\omega/\omega_c} = \frac{A_0}{1+\vec{s}/\omega_c} \tag{6.70}$$

to obtain

$$\mathbf{Z}_{\mathrm{out}} = \frac{R_0\omega_c + R_0\vec{s}}{\omega_c(1+A_0)+\vec{s}}. \tag{6.71}$$

The circuit can now be modeled by a resistor R_0/A_0 in series with an inductor $R_0/(A_0\omega_c)$ all in parallel with another resistor R_0 (three passive components) as shown in figure 6.29. Students should convince themselves of this.

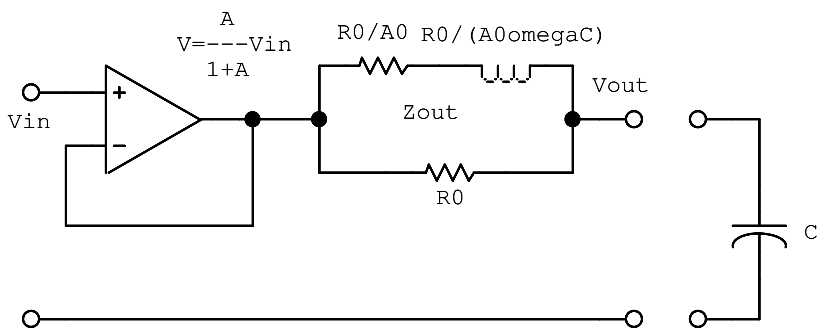


Figure 6.29: An equivalent circuit for a 741-type operational amplifier.

If the op-amp is used to drive a capacitive load, the inductive component in the output impedance could set up an LCR resonant circuit which would result in a slight peaking of transfer function near the corner frequency as shown in figure 6.30

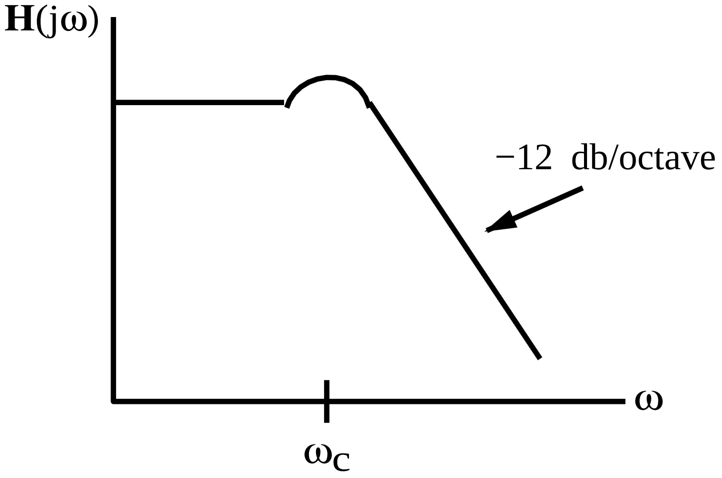


Figure 6.30: The overall transfer function when the amplifier drives a capacitive load.

6.3.2 Input Impedance

When calculating the output impedance we still assumed an infinite input impedance. In this section we will calculate the finite input impedance assuming a zero output impedance. We consider a model that assumes an internal resistor R_T connecting the inverting and non-inverting input terminals of the op-amp as shown in figure 6.31

Consider an inverting amplifier and remove the input resistor so that the input impedance can be calculated directly at the amplifier's input terminals.

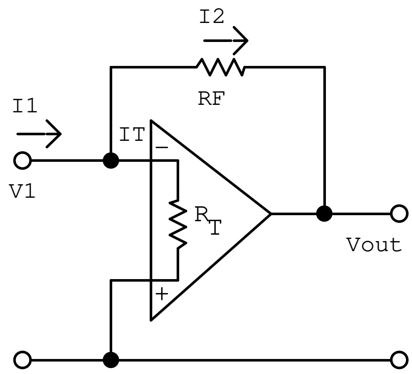


Figure 6.31: Model for calculating the input impedance of the inverting amplifier.

The input impedance is defined by

$$\mathbf{Z}_{\text{in}} = \frac{\mathbf{V}_1}{\mathbf{I}_1} \tag{6.72}$$

and the current at the summing junction is

$$\mathbf{I}_1 = \frac{\mathbf{V}_1}{R_T} + \mathbf{I}_2. \tag{6.73}$$

The current through the feedback resistor is

$$\mathbf{I}_2 = \frac{\mathbf{V}_1 - \mathbf{V}_{\text{out}}}{R_F} \tag{6.74}$$

and the output voltage is related to $\mathbf{V}_1$ by the open-loop gain

$$\mathbf{V}_{\text{out}} = \mathbf{A}(j\omega)(0 - \mathbf{V}_1). \tag{6.75}$$

The resulting input impedance is thus

$$\mathbf{Z}_{\text{in}} = \frac{R_T R_F}{R_F + R_T(1 + \mathbf{A}(j\omega))}. \tag{6.76}$$

For large $\mathbf{A}$

$$\mathbf{Z}_{\text{in}} = \frac{R_F}{\mathbf{A}(j\omega)}. \tag{6.77}$$

The closed-loop input impedance is thus small and almost independent of the large R_T of the operational amplifier.

Now consider the non-inverting amplifier shown in figure 6.32.

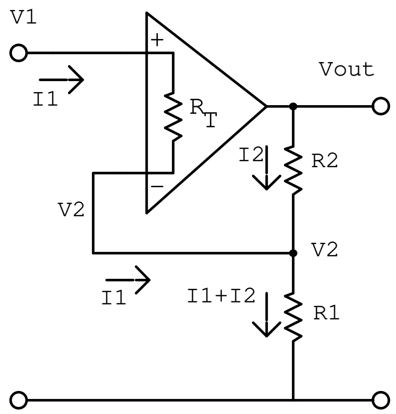


Figure 6.32: Model for calculating the input impedance of the non-inverting amplifier.

The student should calculate the input impedance by recognizing that $\mathbf{I}_1$ is much less than $\mathbf{I}_2$, since R_T is much greater than R_1 or R_2. Your result should be

$$\mathbf{Z}_{\text{in}} = R_T \frac{\mathbf{A}(j\omega) + \mathbf{G}(j\omega)}{\mathbf{G}(j\omega)}, \tag{6.78}$$

where $\mathbf{G}(j\omega)$ is the closed-loop gain of the amplifier. Notice that in contrast to the low input impedance for the inverting amplifier, the non-inverting amplifier exhibits a closed-loop input impedance that is much larger than the open-loop value R_T.

6.3.3 Voltage and Current Offsets

Since op-amps are generally DC coupled, there will appear a nonzero output even when the inputs are grounded or connected to give no input signal. The voltage offset is the result of slightly different transistors making up the differential input stage. The voltage offset can be reduced by using an externally-adjustable bias resistor (voltage offset null circuitry).

The current offsets at the inverting and non-inverting input terminals are usually base currents into two identical bipolar transistors. Thus their difference can be expected to be much less than either base current alone. Using this fact the student should be able to explain the reason for having an extra resistor between the non-inverting input and ground for the inverting amplifier. The resister should have a value equal to the input resistor and feedback resistor in parallel.

We define the following:

output offset voltage – The voltage at the output when the input voltage is zero (input terminals grounded).

common mode voltage – The voltage at the output when the voltage at the inverting and non-inverting inputs are equal.

common mode rejection ratio (CMRR) – The ratio of the op-amp gain when operating in differential mode to the gain when operating in common mode.

common mode rejection (CMR) – The ability to respond to only differences at the input terminals: $\mathrm{CMR} \equiv 20 \log_{10}(\mathrm{CMRR})$.

6.3.4 Current Limiting and Slew Rate

The presence of resistance at the output of the op-amp limits the current that the amplifier can deliver into a load, as shown in figure 6.33. Current limiting is a nonlinear property that invalidates the two normal approximation rules. When an op-amp is driven into a current-limiting condition it goes into saturation and becomes a constant current source. For a large load the output signal will be voltage-limited. A similar breakdown of the rules occurs when the amplifier is driven into voltage-limited operation.

The op-amp performance can be demonstrated by applying a step function to the input and observing the output response, as shown in figure 6.33b. The actual output will have a finite slope (*slew rate*) and *overshoot* the final voltage value. It then approaches the final voltage either exponentially or with some damped ringing. The slew rate and overshoot are nonlinear effects. The *settling time* after amplifier saturation is defined as the time between the edge of the applied step function and the point where the amplifier output settles to within some stated percentage of the target voltage value.

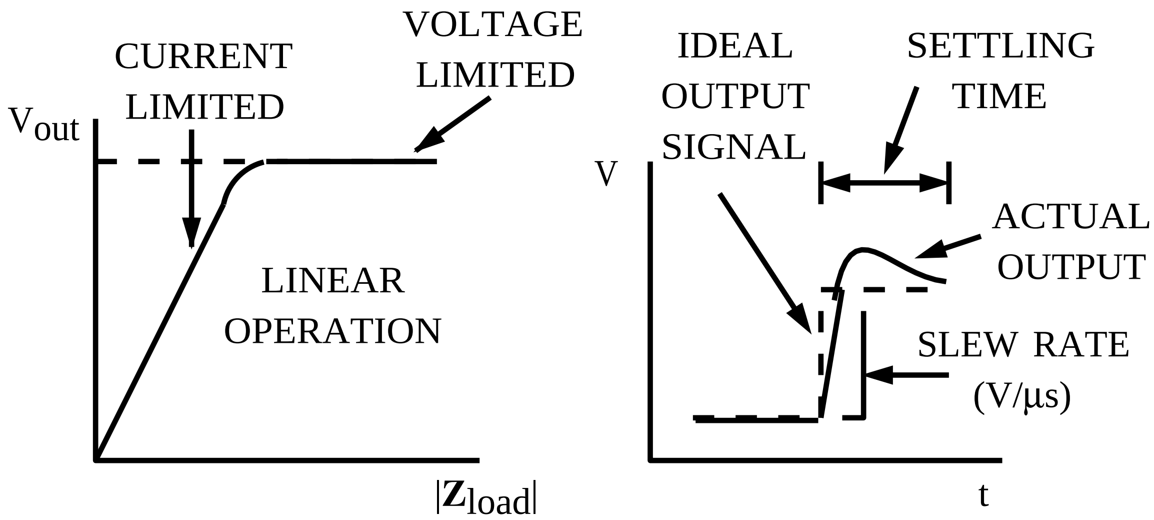
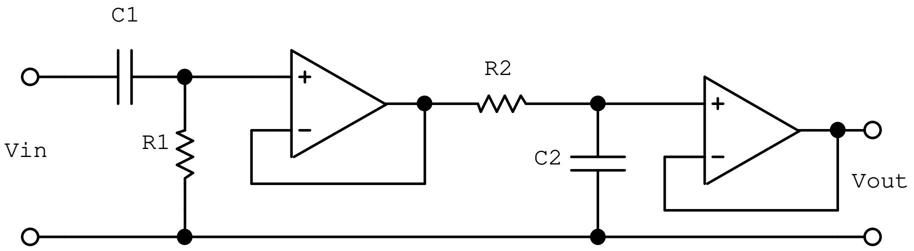


Figure 6.33: a) Voltage-limited and current-limited operational regions for an operational amplifier and b) definition of slew rate and settling time for an operational amplifier.

6.4 Problems

1. Consider the circuit below. (You may assume that the op-amps are ideal.)



   (a) Write an expression for the transfer function $\mathbf{G}(\omega)$. Express your result in terms of the amplitude of the output and the phase relative to the input. Let $R_1 = 1$ kΩ, $R_2 = 100\ \Omega$, $C_1 = 100\ \mu$F and $C_2 = 1\ \mu$F. *Do not simplify the algebra.*

   (b) What are the (real) zeroes in the transfer function, if any?

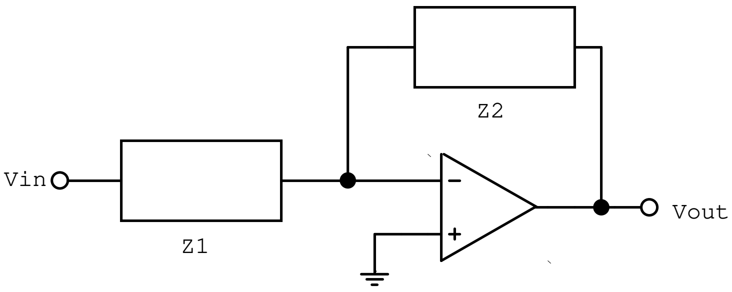
   (c) What are the (real) poles in the transfer function if any?

   (d) Sketch the transfer function as a function of ω on a log-log plot. Your sketch should show the slope of $|\mathbf{G}(\omega)|$ in the large and small ω limits, the corner frequencies, and the value of $|\mathbf{G}(\omega)|$ at the corner frequencies.

   (e) Describe the dependence of the output on frequency at small and large frequencies in dB/octave.

2. (a) Write the two rules for the analysis of circuits which utilize "ideal" op-amps.

   (b) Write an expression for the potential V_{out} for the following circuit.



   (c) Let $Z_1 = 1$ kΩ and $Z_2 = 10$ kΩ. Sketch a log-log plot showing the function $\mathbf{G}(\omega)$ for the above circuit assuming that a general purpose op-amp such as the 741 is used.

   (d) The 741 op-amp has a corner frequencies of 4 Hz, DC open-loop gain of 2×10^5 and a fall off at high frequency of 6 dB/octave. What is the frequency domain over which the amplifier defined in part (c) will have constant gain? What is the gain of the amplifier in this frequency domain?

(e) Suppose now that the impedance Z_1 is replaced with a capacitor with a capacitance C ($Z_2 = 10$ kΩ). For frequencies much greater than 4 Hz, the 741 op-amp will attenuate the signal if the product RC is greater than some maximum value. For a frequency of 50 kHz, what is the maximum value for C for which the op-amp [$\mathbf{A}(\omega)$] will not attenuate the output signal at high frequencies? *Hint: If you sketch* $\mathbf{A}(\omega)$ *and* $\mathbf{G}(\omega)$*, you will be able to see the constraint on* $\mathbf{G}(\omega)$*.*

3. Set up an operational amplifier circuit to solve the equation

$$\frac{d^2x}{dt^2} + 5\frac{dx}{dt} + 7x + 3 = 0.$$

Hint: the input is d^2x/dt^2*.*

4. Draw a schematic diagram of a circuit for which $V_{\text{out}} = \ln(V_{\text{in}})$. Specify the limitations on the input voltage range, if any.

Chapter 7

Digital Circuits

Analog signals have a continuous range of values within some specified limits and can be associated with continuous physical phenomena.

Digital signals typically assume only two discrete values (states) and are appropriate for any phenomena involving counting or integer numbers.

While we were mostly interested in voltages and currents at specific points in analog circuits, we will be interested in the information flow in digital circuits.

The active elements in digital circuits are either bipolar transistors or FETs. These transistors are permitted to operate in only two states, which normally correspond to two output voltages. Hence the transistors act as switches.

Before starting we will first review number systems and Boolean algebra.

7.1 Number Systems

The two digital states can be given various names: ON/OFF, true/false, high/low, 1/0, etc.. The 1 and 0 notation naturally leads to the use of binary (base 2) numbers. Octal (base 8) and hexadecimal (base 16) numbers are also used since they provide a condensed number notation. Decimal (base 10) numbers are not of much use in digital electronics.

7.1.1 Binary, Octal and Hexadecimal Numbers

Consider a decimal number with digits a b c. We can write abc as

$$abc_{10} = a \times 10^2 + b \times 10^1 + c \times 10^0. \tag{7.1}$$

Similarly, in the binary system a number with digits a b c can be written as

$$abc_2 = a \times 2^2 + b \times 2^1 + c \times 2^0. \tag{7.2}$$

Each digit is known as a bit and can take on only two values: 0 or 1. The left most bit is the highest-order bit and represents the most significant bit (MSB), while the lowest-order bit is the least significant bit (LSB).

Conversion from binary to decimal can be done using a set of rules. But it is much easier to use a calculator or tables (table 7.1).

Table 7.1: Decimal, binary, hexadecimal and octal equivalents.

Decimal	*Binary*	*Hex*	*Octal*
00	00000	00	00
01	00001	01	01
02	00010	02	02
03	00011	03	03
04	00100	04	04
05	00101	05	05
06	00110	06	06
07	00111	07	07
08	01000	08	10
09	01001	09	11
10	01010	0A	12
11	01011	0B	13
12	01100	0C	14
13	01101	0D	15
14	01110	0E	16
15	01111	0F	17
16	10000	10	20

The eight octal numbers are represented with the symbols $0, \ldots, 7$, while the 16 hexadecimal numbers use $0, \ldots, 9, A, \ldots, F$.

In the octal system a number with digits $a\ b\ c$ can be written as

$$abc_8 = a \times 8^2 + b \times 8^1 + c \times 8^0, \tag{7.3}$$

while one in the hexadecimal system is written as

$$abc_{16} = a \times 16^2 + b \times 16^1 + c \times 16^0. \tag{7.4}$$

A binary number is converted to octal by grouping the bits in groups of three, and converted to hexadecimal by grouping the bits in groups of four. Octal to hexadecimal conversion, or visa versa, is most easily performed by first converting to binary.

Example: *Convert the binary number 1001 1110 to hexadecimal and to decimal.*

$$\begin{aligned} 10011110_2 &= 9E(HEX) && (7.5)\\ &= 2^7 + 2^4 + 2^3 + 2^2 + 2^1 && (7.6)\\ &= 158(DECIMAL). && (7.7) \end{aligned}$$

Example: *Convert the octal number 175_8 to hexadecimal.*

$$\begin{aligned} 175_8 &= 001111101_2 && (7.8)\\ &= 001111101_2 && (7.9)\\ &= 07D(HEX). && (7.10) \end{aligned}$$

Example: *Convert the number 146 to binary by repeated subtraction of the largest power of 2 contained in the remaining number.*

$$\begin{aligned} 146_{10} &= 128 + 16 + 2 && (7.11)\\ &= 2^7 + 2^4 + 2^1 && (7.12)\\ &= 10010010_2. && (7.13) \end{aligned}$$

Example: *Devise a method similar to that used in the previous problem and convert 785 to hexadecimal by subtracting powers of 16.*

$$\begin{aligned} 785_{10} &= 3 \times 16^2 + 16 + 1 && (7.14)\\ &= 311(HEX). && (7.15) \end{aligned}$$

7.1.2 Number Representation

We define the following

word: a binary number consisting of an arbitrary number of bits.

nibble: a 4-bit word (one hexadecimal digit).

byte: an 8-bit word.

We often use the expressions 16-bit word (short word) or 32-bit word (long word) depending on the type of computer being used. Most fast computers today actually employ a 64-bit word at the hardware level.

If a word has n bits it can represent 2^n different numbers in the range 0 to $2^n - 1$. Negative numbers are usually represented by the so called *2's complement* notation. To obtain the 2's compliment of a number first take the complement (invert each bit) and then add 1. All the negative numbers will have a 1 in the MSB position, and the numbers will now range from -2^{n-1} to $2^{n-1} - 1$. The electronic advantages of the 2's complement notation becomes evident when addition is performed. Convince yourself of this advantage.

7.2 Boolean Algebra

The binary 0 and 1 states are naturally related to the true and false logic variables. We will find the following Boolean algebra useful. Consider two logic variables A and B and the result of some Boolean logic operation Q. We can define

$$Q \equiv A \text{ AND } B \equiv A \cdot B. \tag{7.16}$$

Q is true if and only if A is true AND B is true.

$$Q \equiv A \text{ OR } B \equiv A + B. \tag{7.17}$$

Q is true if A is true OR B is true.

$$Q \equiv \text{NOT } A \equiv \overline{A}. \tag{7.18}$$

Q is true if A is false.

A useful way of displaying the results of a Boolean operation is with a truth table. We will make extensive use of truth tables later. If no "–" is available on your text processor or circuit drawing program an "N" can be used, ie. $\overline{A} \equiv NA$.

We list a few trivial Boolean rules in table 7.2.

Table 7.2: Properties of Boolean Operations.

$A \cdot 0$	$=$	0
$A + 0$	$=$	A
$A \cdot 1$	$=$	A
$A + 1$	$=$	1
$A \cdot A$	$=$	A
$A + A$	$=$	A
$A \cdot \overline{A}$	$=$	0
$A + \overline{A}$	$=$	1

The Boolean operations obey the usual commutative, distributive and associative rules of normal algebra (table 7.3).
We will also make extensive use of De Morgan's theorems (table 7.4).

7.3 Logic Gates

Electronic circuits which combine digital signals according to the Boolean algebra are referred to as *logic gates*; gates because they control the flow of information. *Positive logic* is an electronic representation in which the true state is at a higher voltage, while *negative logic* has the true state at a lower voltage. We will use the positive logic type in this course.

Logic circuits are grouped into families, each with their own set of detailed operating rules. Some common logic families are:

Table 7.3: Boolean commutative, distributive and associative rules.

$\overline{\overline{A}}$	$=$	A
$A \cdot B$	$=$	$B \cdot A$
$A + B$	$=$	$B + A$
$A \cdot (B + C)$	$=$	$A \cdot B + A \cdot C$
$A \cdot (B \cdot C)$	$=$	$(A \cdot B) \cdot C$
$A + (B + C)$	$=$	$(A + B) + C$
$A + A \cdot B$	$=$	A
$A \cdot (A + B)$	$=$	A
$A \cdot (\overline{A} + B)$	$=$	$A \cdot B$
$A + \overline{A} \cdot B$	$=$	$A + B$
$\overline{A} + A \cdot B$	$=$	$\overline{A} + B$
$\overline{A} + A \cdot \overline{B}$	$=$	$\overline{A} + \overline{B}$

Table 7.4: De Morgan's theorems.

$\overline{A \cdot B}$	$=$	$\overline{A} + \overline{B}$
$\overline{A + B}$	$=$	$\overline{A} \cdot \overline{B}$

RTL: resistor-transistor logic,

DTL: diode-transistor logic,

TTL: transistor-transistor logic,

NMOS: N-channel metal-oxide silicon,

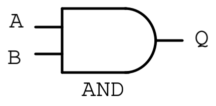
CMOS: complementary metal-oxide silicon and

ECL: emitter-coupled logic.

The ECL is very fast. The MOS features very low power consumption and hence is often used in LSI technology. The TTL is normally used for small-scale integrated circuit units.

The schematic symbols of the basic gates and the logic truth tables are shown in figure 7.1.

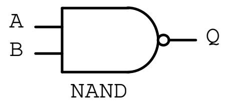
The open circle is used to indicate the NOT or negation function and can be replaced by an inverter in any circuit. A signal is negated if it passes through the circle. Any logic operation can be formed from NAND or NOR gates or a combination of both. We also commonly have gates with more than two inputs. Inverter gates can be formed by applying the same logic signal to both inputs of an NOR or NAND gate.



$$Q = A \cdot B$$

AND

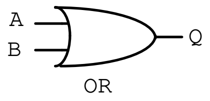
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1



$$Q = \overline{A \cdot B}$$

NAND

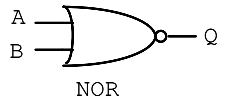
A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0



$$Q = A + B$$

OR

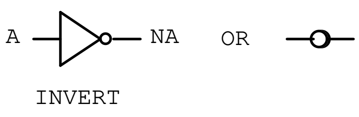
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1



$$Q = \overline{A + B}$$

NOR

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0



$$Q = \overline{A}$$

NOT

A	Q
0	1
1	0

Figure 7.1: Symbols and truth tables for the four basic two-input gates: a) AND, b) NAND, c) OR, d) NOR and e) the inverter.

7.4 Combinational Logic

We will design some useful circuits using the basic logic gates, and use these circuits later on as building blocks for more complicated circuits.

We describe the basic AND, NAND, OR or NOR gates as being *satisfied* when the inputs are such that a change in any one will change the output. A satisfied AND or NOR gate has a true output, whereas a satisfied NAND or OR gate has a false output. We sometimes identify the input logic variables A, B, C, etc. with an n-bit number $ABC\ldots$.

7.4.1 Combinational Logic Design Using Truth Tables

The following steps are a useful formal approach to combinational problems:

1. Devise a truth table of the independent input variables and the resulting output quantities.
2. Write Boolean algebra statements that describes the truth table.
3. Reduce the Boolean algebra.
4. Mechanize the Boolean statements using the appropriate logic gates.

Consider the truth table that defines the OR gate. Using the lines in this table that yield a true result gives.

$$\begin{aligned} Q &= \overline{A}\cdot B + A\cdot\overline{B} + A\cdot B & (7.19)\\ &= \overline{A}\cdot B + A\cdot\overline{B} + A\cdot B + A\cdot B & (7.20)\\ &= A\cdot(B+\overline{B}) + B\cdot(A+\overline{A}) & (7.21)\\ &= A + B & (7.22)\end{aligned}$$

Since Q is a two-state variable all other input state combinations must yield a false. If the truth table had more than a single output result, each such result would require a separate equation. An alternative is to write an expression for the false condition.

$$\begin{aligned} \overline{Q} &= \overline{A}\cdot\overline{B} & (7.23)\\ \overline{\overline{Q}} &= \overline{\overline{A}\cdot\overline{B}} & (7.24)\\ Q &= \overline{\overline{A}} + \overline{\overline{B}} & (7.25)\\ &= A + B & (7.26)\end{aligned}$$

7.4.2 The AND-OR Gate

Some logic families provide a gate known as an AND-OR-INVERT or AOI gate (figure 7.2).

$$\begin{aligned} Q &= \overline{A\cdot B + C\cdot D} & (7.27)\\ \overline{Q} &= A\cdot B + C\cdot D & (7.28)\end{aligned}$$

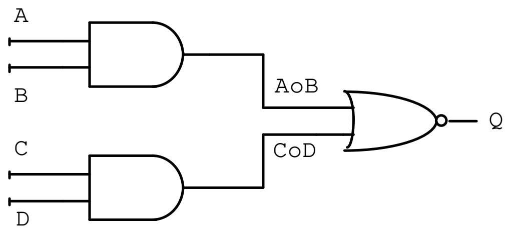
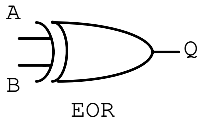


Figure 7.2: The basic AND-OR-INVERT gate.

7.4.3 Exclusive-OR Gate

The exclusive-OR gate (EOR or XOR) is a very useful two-input gate. The schematic symbol and truth table are shown in figure 7.3.



$$Q = A \oplus B$$

XOR (EOR)

A	B	Q
0	0	0
1	0	1
0	1	1
1	1	0

Figure 7.3: The schematic symbol for the exclusive-OR gate (EOR or XOR) and its truth table.

From the truth table

$$Q = \overline{A} \cdot B + A \cdot \overline{B} \tag{7.29}$$
$$\overline{Q} = \overline{A} \cdot \overline{B} + A \cdot B \tag{7.30}$$

and we can draw the mechanization directly from the truth table (figure 7.4).

7.4.4 Timing Diagrams

Normally signals flip from one logic state to another. The time it takes the signal to move between states is the *transition time* t_t, where the time is measured between 10% and 90% of the signal levels. Delays within the logic elements result in a *propagation (pulse) delay* t_{pd}, where the time is measured between 50% of the input signal and 50% of the output response. Definitions of the transition time and propagation delay are shown in figure 7.5.

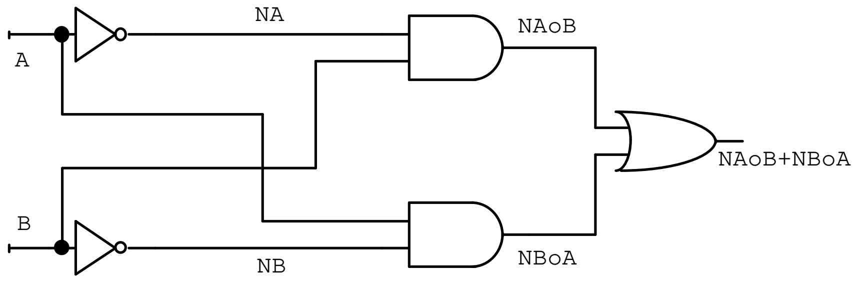


Figure 7.4: A mechanization of the exclusive-OR directly from the truth table.

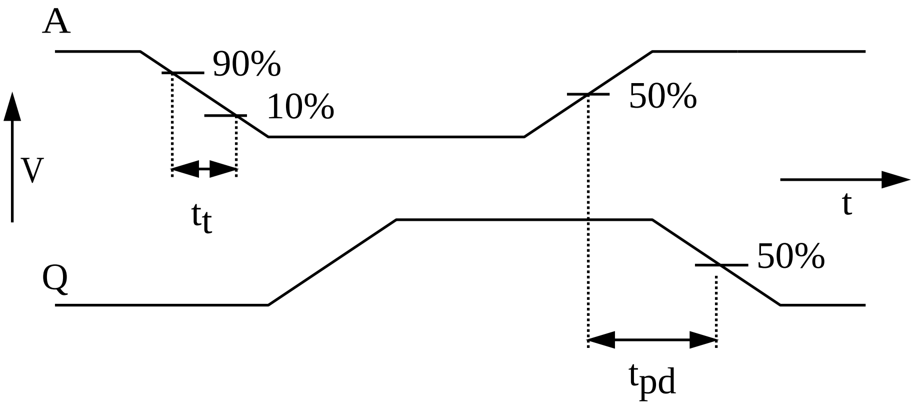


Figure 7.5: The transition time of the input and output signals, and the propagation delay through a gate.

7.4.5 Signal Race

Signal racing is the condition when two or more signals change almost simultaneously. The condition may cause glitches or spikes in the output signal as shown in figure 7.6. The effects of these glitches can be eliminated by using synchronous timing techniques. In synchronous timing the glitches are allowed to come and go, and the logic state changes are initiated by a timing pulse (clock pulse).

7.4.6 Half and Full Adders

From basic gates, we will develop a full adder circuit that adds two binary number. Consider adding two 2-bit binary numbers X_1X_0 and Y_1Y_0. $X_0 + Y_0 = C_1Z_0$, where C_1 is the carry bit. The truth table for all combinations of X_0 and Y_0 is shown in table 7.5.
From the truth table

$$Z_0 = \overline{X}_0 \cdot Y_0 + X_0 \cdot \overline{Y}_0 = X_0 \oplus Y_0 \tag{7.31}$$

$$C_1 = X_0 \cdot Y_0 \tag{7.32}$$

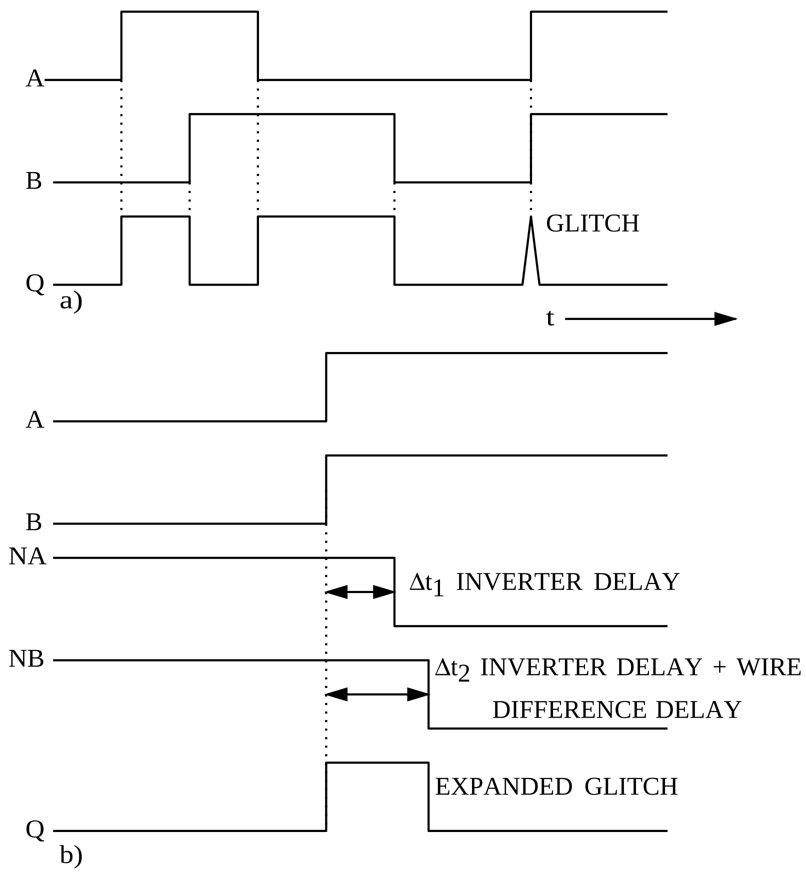


Figure 7.6: a) A timing diagram for the EOR circuit. b) An expanded view of the glitch shows it to be caused by a signal race condition.

The mechanization of these two equation is shown in figure 7.7.
This circuit is known as the half adder. It can not handle the addition of any two arbitrary numbers because it does not allow the input of a carry bit from the addition of two previous digits. A circuit that can handle these three inputs can perform the addition of any two binary numbers.

The truth table for three input variables is shown in figure 7.8.
From the truth table

$$C_2 = \overline{C}_1 \cdot X_1 \cdot Y_1 + C_1 \cdot \overline{X}_1 \cdot Y_1 + C_1 \cdot X_1 \cdot \overline{Y}_1 + C_1 \cdot X_1 \cdot Y_1 \quad (7.33)$$

$$= X_1 \cdot Y_1 + C_1 \cdot X_1 + C_1 \cdot Y_1 \quad (7.34)$$

This is known as majority logic. And a majority detector is shown in figure 7.9

$$Z_1 = \overline{C}_1 \cdot \overline{X}_1 \cdot Y_1 + \overline{C}_1 \cdot X_1 \cdot \overline{Y}_1 + C_1 \cdot \overline{X}_1 \cdot \overline{Y}_1 + C_1 \cdot X_1 \cdot Y_1 \quad (7.35)$$

$$= C_1 \oplus (X_1 \oplus Y_1) \quad (7.36)$$

Table 7.5: The binary addition of two 2-bit numbers. The 2^0 column.

X_0	Y_0	Z_0	C_1
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

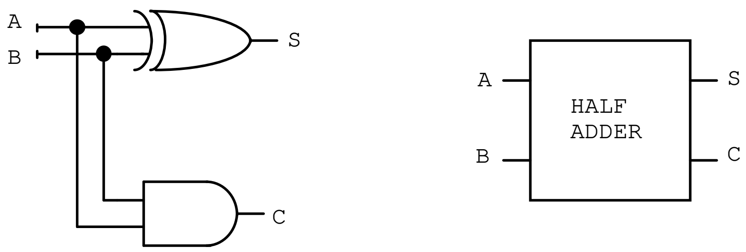


Figure 7.7: A mechanization of the half adder using an EOR and an AND gate.

The following device (figure 7.10) is known as a full adder and is able to add three single bits of information and return the sum bit and a carry-out bit.

The circuit shown in figure 7.11 is able to add any two numbers of any size. The inputs are $X_2X_1X_0$ and $Y_2Y_1Y_0$, and the output is $C_3Z_2Z_1Z_0$.

C_1	X_1	Y_1	Z_1	C_2
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

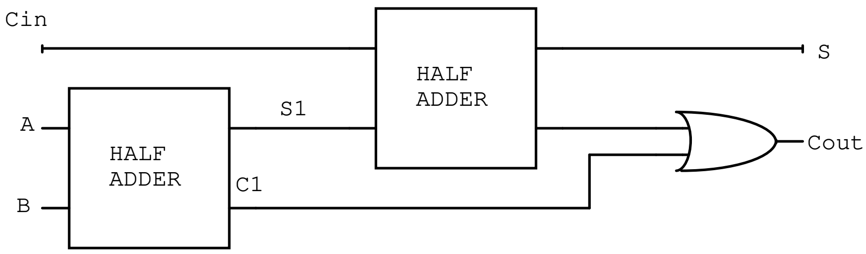


Figure 7.8: The binary addition of two 2-bit numbers. The 2^1 column.

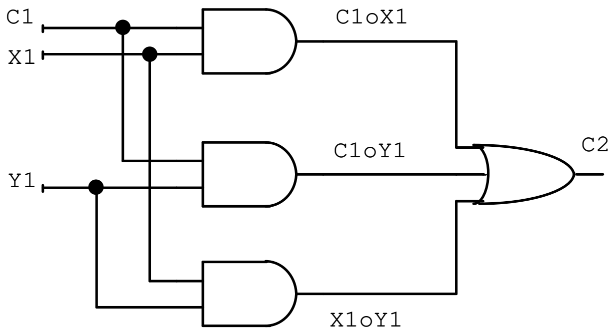


Figure 7.9: A mechanization of the majority detector.

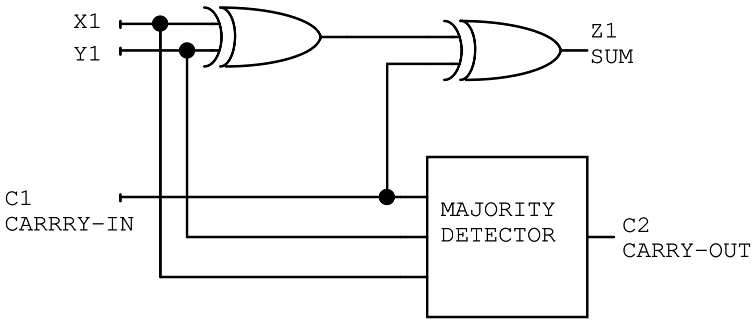


Figure 7.10: The full adder mechanization.

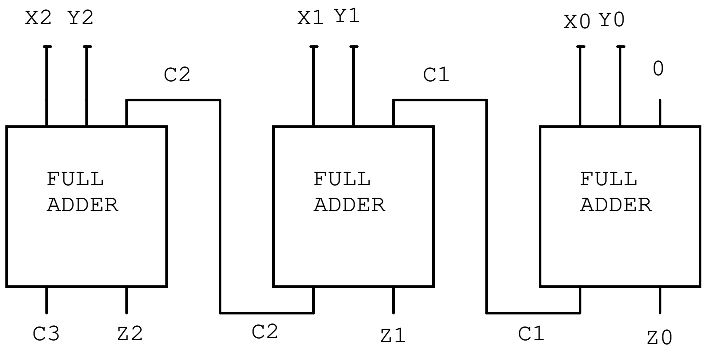


Figure 7.11: A circuit capable of adding two 3-bit numbers.

Example: *If the input to the circuit in figure 7.12 is written as a number $ABCD$, write the nine numbers that will yield a true Q.*

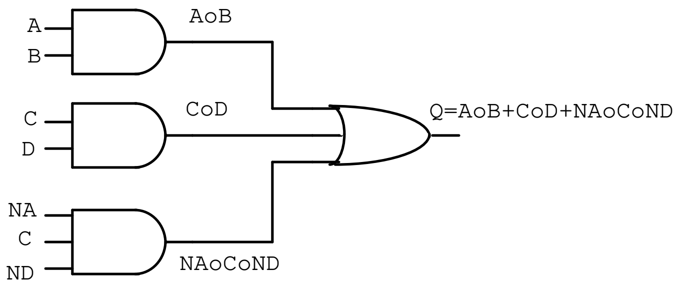


Figure 7.12: A typical logic function.

Table 7.6: The truth table for the typical logic function example.

A	B	C	D	$A \cdot B$	$C \cdot D$	$\overline{A} \cdot C \cdot \overline{D}$	Q
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0
1	0	1	0	0	0	0	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	1
1	1	1	0	1	0	0	1
1	1	1	1	1	1	0	1

$ABCD = (2, 3, 6, 7, 11, 12, 13, 14, 15)$ *gives* Q *true.*

Example: *Using the 2's complement convention, the 3-bit number ABC can represent the numbers from -3 to 3 as shown in table 7.7 (ignore -4). Assuming that A, B, C and $\overline{A}, \overline{B}, \overline{C}$ are available as inputs, the goal is to devise a circuit that will yield a 2-bit output EF that is the absolute value of the ABC number. You have available only two- and three-input AND and OR gates.*

1. *Fill a truth table with the ABC and EF bits.*

   The truth table is shown in table 7.7.

Table 7.7: Truth table with for the ABC and EF bits.

Value	*A*	*B*	*C*	*E*	*F*
0	0	0	0	0	0
1	0	0	1	0	1
2	0	1	0	1	0
3	0	1	1	1	1
-1	1	1	1	0	1
-2	1	1	0	1	0
-3	1	0	1	1	1
-4	1	0	0		

2. *Write a Boolean algebra expression for E and for F.*

$$\begin{aligned}
E &= \overline{A}\cdot B\cdot\overline{C}+\overline{A}\cdot B\cdot C+A\cdot\overline{B}\cdot C+A\cdot B\cdot\overline{C} && (7.37)\\
&= \overline{A}\cdot(B\cdot\overline{C}+B\cdot C)++A\cdot(\overline{B}\cdot C+B\cdot\overline{C}) && (7.38)\\
&= \overline{A}\cdot B\cdot(\overline{C}+C)+A\cdot(B\oplus C) && (7.39)\\
&= \overline{A}\cdot B+A\cdot(B\oplus C). && (7.40)
\end{aligned}$$

$$\begin{aligned}
F &= \overline{A}\cdot\overline{B}\cdot C+\overline{A}\cdot B\cdot C+A\cdot\overline{B}\cdot C+A\cdot B\cdot C && (7.41)\\
&= \overline{A}\cdot(\overline{B}\cdot C+B\cdot C)+A\cdot(\overline{B}\cdot C+B\cdot C) && (7.42)\\
&= \overline{A}\cdot C\cdot(\overline{B}+B)+A\cdot C\cdot(\overline{B}+B) && (7.43)\\
&= \overline{A}\cdot C+A\cdot C && (7.44)\\
&= (\overline{A}+A)\cdot C && (7.45)\\
&= C. && (7.46)
\end{aligned}$$

3. *Mechanize these expressions.*

   The mechanized expressions are shown in figure 7.13.

Example: *Suppose that the 2-bit binary number AB must be transmitted between devices in a noisy environment. To reduce undetected errors introduced by the transmission, an extra bit P is often included to add redundancy to the information. Assume that P is set true or false as needed to make an odd number of true bits in the resulting 3-bit number ABP. When the number is received, logic circuits are required to generate an error signal E whenever the odd number of bits condition is not met.*

1. *Develop a truth table of E in terms of A, B and P.*

   The truth table is shone in table 7.8.

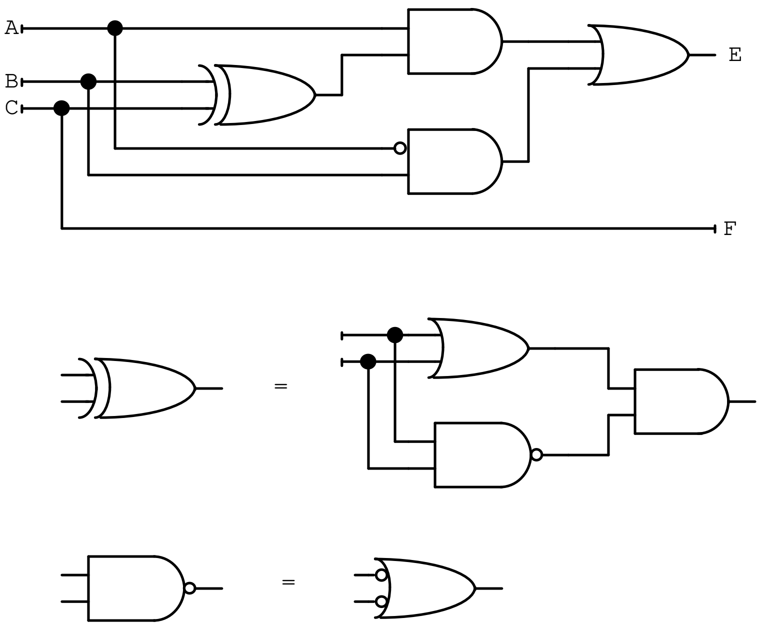


Figure 7.13: Mechanization for the ABC and EF bits.

2. *Write a Boolean expression for E as determined directly from the truth table.*

$$E = \overline{A} \cdot \overline{B} \cdot \overline{P} + \overline{A} \cdot B \cdot P + A \cdot \overline{B} \cdot P + A \cdot B \cdot \overline{P} \tag{7.47}$$

3. *Using De Morgan's theorem twice, reduce this expression to one EOR and one NEOR operation. (This is very similar to the half-adder problem.)*

$$\begin{aligned} E &= \overline{A} \cdot (\overline{B} \cdot \overline{P} + B \cdot P) + A \cdot (\overline{B} \cdot P + B \cdot \overline{P}) && (7.48) \\ &= \overline{A} \cdot \overline{B \oplus P} + A \cdot (B \oplus P) && (7.49) \\ &= A \oplus \overline{(B \oplus P)} && (7.50) \end{aligned}$$

Table 7.8: Truth table for E in terms of A, B and P.

A	B	P	E
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

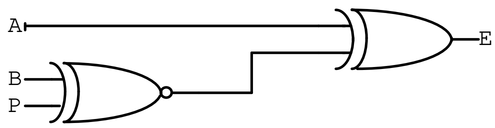


Figure 7.14: Mechanize for E.

7.5 Multiplexers and Decoders

Multiplexers and decoders are used when many lines of information are being gated and passed from one part of a circuit to another.

Multiplexing is when multiple data signals share a common propagation path. Time multiplexing is when different signals travel along the same wire but at different times. These devices have data and address lines, and usually include a enable/disable input. When the device is disabled the output is locked into some particular state and is not effected by the inputs. Shown in figure 7.15 is a 4-line to 1-line multiplexer.

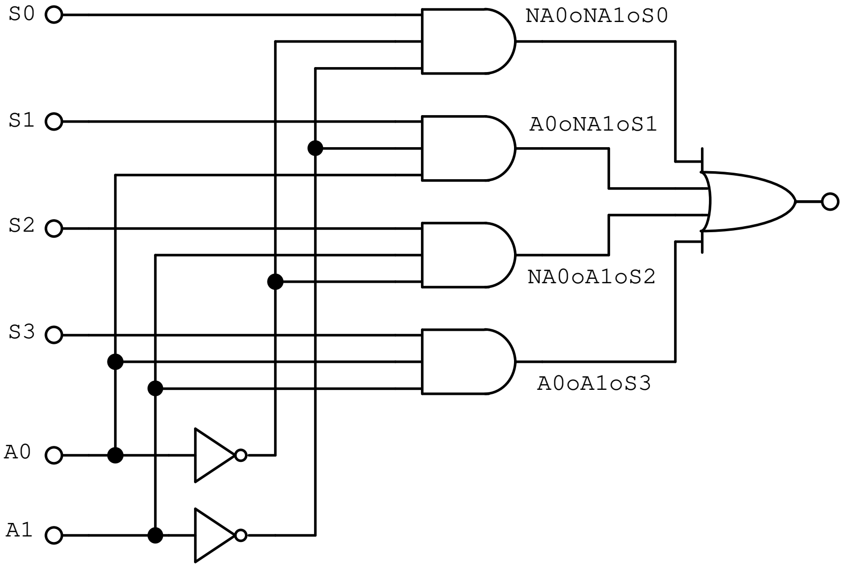


Figure 7.15: 4-line to 1-line multiplexer.

A decoder de-multiplexes the signals back onto several different lines. Shown in figure 7.16 is a binary-to-octal decoder (3-line to 8-line decoder).

Decoders (octal decoder) can also convert a 3-bit binary number to an output on one of eight lines. Hexadecimal decoders are 4-line to 16-line devices. When the decoder is disabled the outputs will be high. A decoder would normally be disabled while the address lines were changing to avoid glitches on the output lines.

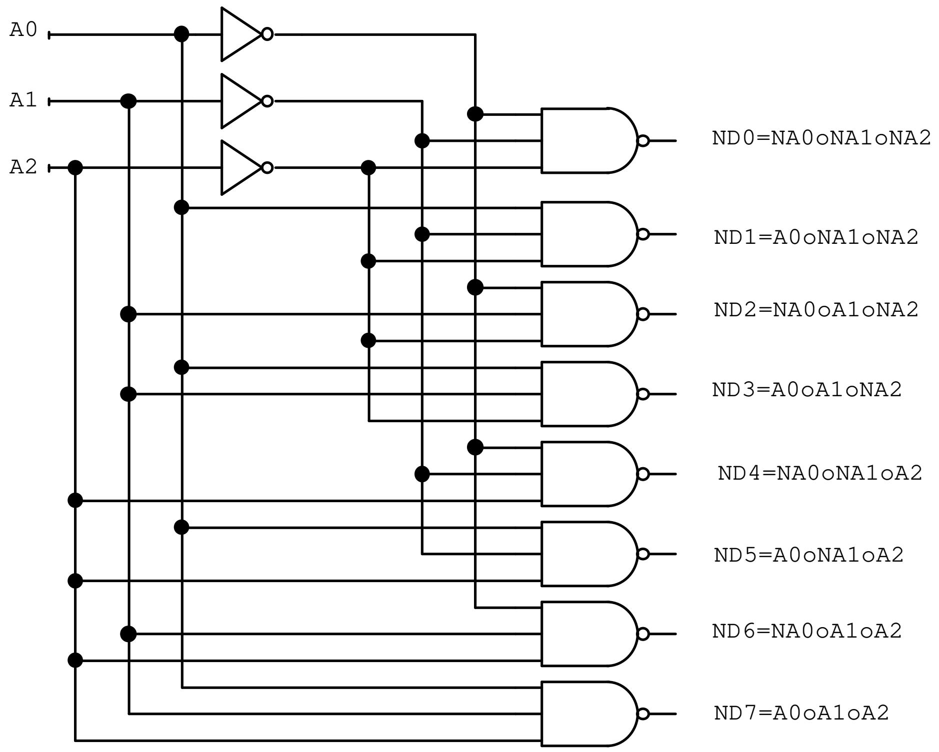


Figure 7.16: Octal decoder.

7.6 Schmitt Trigger

A noisy input signal to a logic gate could cause unwanted state changes near the voltage threshold. Schmitt trigger logic reduces this problem by using two voltage thresholds: a high threshold to switch the circuit during low-to-high transitions and a lower threshold to switch the circuit during high-to-low transitions. Such a trigger scheme is immune to noise as long as the peak-to-peak amplitude of the noise is less than the difference between the threshold voltages. A gate with the Schmitt trigger feature has a small hysteresis curve drawn inside the gate symbol. Schmitt triggers are mostly used in inverters or simple gates to condition slow or noisy signals before passing them to more critical parts of the logic circuit.

7.7 The Data Bus

A *bus* is a common wire connecting various points in a circuit; examples are the ground bus and power bus. The *data bus* carries digital information. A data bus is usually a group of parallel wires connecting different parts of a circuit with each individual wire carrying a different logic signal. The data bus is connected to the inputs of several gates and to the outputs of several gates. You cannot connect directly the outputs of normal gates. For this purpose three-state output logic is commonly used but will not be discussed here.

A data bus line may be time multiplexed to serve different functions at different times.

At any time only one gate my drive information onto the bus line but several gates may receive it. In general, information may flow on the bus wires in both directions. This type of bus is referred to as a bidirectional data bus.

7.8 Two-State Storage Elements

Analog voltage storage times are limited since the charge on a capacitor will eventually leak away. The problem of discrete storage reduces to the need to store a large number of two-state variables. The four commonly used methods are: 1) magnetic domain orientation, 2) presence or absence of charge (not amount of charge) on a capacitor, 3) presence or absence of an electrical connection and 4) the DC current path through the latches and flip-flops of a digital circuit. We will discuss only the later.

7.9 Latches and Un-Clocked Flip-Flops

It is possible using basic logic gates to build a circuit that remembers its present condition. It is also possible to build counting circuits. The basic counting unit is the flip-flop (FF).

7.9.1 Latches

All latches have two inputs: data and enable/disable. And typically Q and $\overline{Q}$ outputs. A *ones-catching* latch can be built as shown in figure 7.17.
When the control input C is false, the output Q follows the input D, but when the control input goes true, the output latches true as soon as D goes true and then stays there independent of further changes in D.

One of the most useful latches is known as the *transparent* latch or *D-type* latch. The transparent latch is like the ones-catching latch but the input D is frozen when the latch is disable. The operation of this latch is the same as that of the statically triggered D flip-flop discussed below.

7.9.2 RS and $\overline{\mathrm{RS}}$ Flip-Flops

The RS flip-flop (RSFF) is the result of cross-connecting two NOR gates as shown in figure 7.18. The RS inputs are referred to as *active ones.*
The ideal flip-flop has only two rest states, set and reset, defined by $Q\overline{Q} = 10$ and $Q\overline{Q} = 01$, respectively.

A very similar flip-flop can be constructed using two NAND gates as shown in figure 7.19. The $\overline{\mathrm{RS}}$ inputs are now *active zeros.*

These FF are often referred to as the set/reset type and are un-clocked.

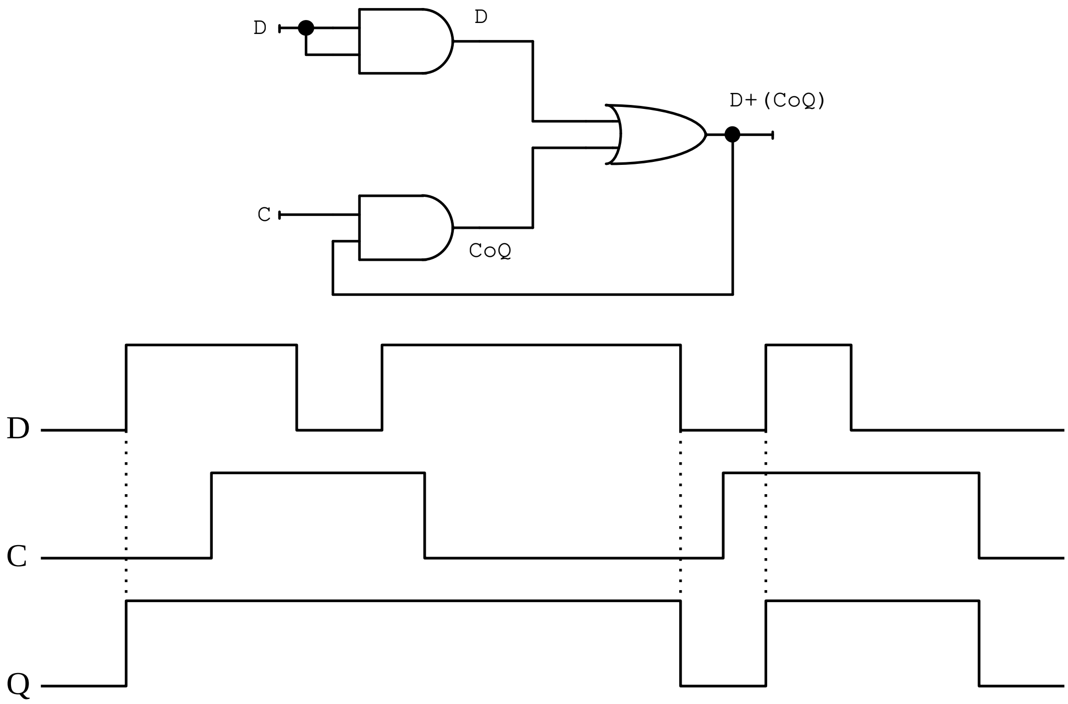


Figure 7.17: An AND-OR gate used as a “ones catching” latch and its timing diagram.

S	R	Q	$\overline{Q}$
0	0	no change	
0	1	0	1
1	0	1	0
1	1	undefined	

RS flip-flop

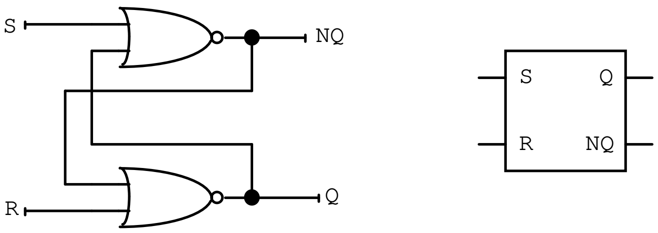


Figure 7.18: The RS flip-flop constructed from NOR gates, and its circuit symbol and truth table.

7.10 Clocked Flip-Flops

A clocked flip-flop has an additional input that allows output state changes to be synchronized to a clock pulse.

7.10.1 Clocked RS Flip-Flop

We first consider the static clocked (level-sensitive) RS flip-flop shown in figure 7.20.
The first five lines in the truth table give the static input and output states. The last four lines show the state of the outputs after a complete clock pulse p.

$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	undefined	
0	1	1	0
1	0	0	1
1	1	no change	

$\overline{RS}$ flip-flop

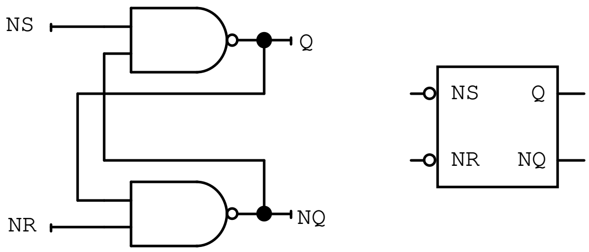


Figure 7.19: The $\overline{RS}$ flip-flop constructed from NAND gates, and its circuit symbol and truth table.

S_C	R_C	C	Q	$\overline{Q}$
x	x	0	no change	
0	0	1	no change	
0	1	1	0	1
1	0	1	1	0
1	1	1	undefined	
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	undefined	

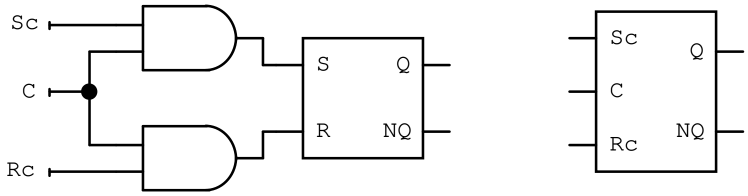


Figure 7.20: The clocked RS flip-flop can be constructed from an RS flip-flop and two additional gates, the schematic symbol for the static clocked RSFF and its truth table.

7.10.2 D Flip-Flop

The D flip-flop avoids the undefined states in the RSFF truth table by reducing the number of input options (figure 7.21).

D	C	Q	$\overline{Q}$
x	0	no change	
0	p	0	1
1	p	1	0

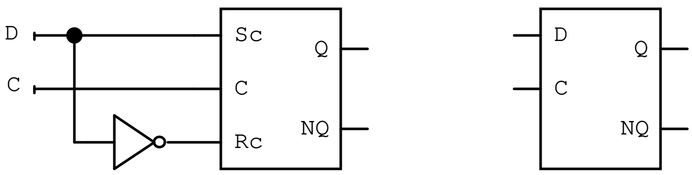


Figure 7.21: Statically triggered D flip-flop (transparent latch) mechanized with clocked RS, and the schematic symbol and its truth table.

The statically clocked DFF is also known as a transparent latch.

7.10.3 JK Flip-Flop

The JKFF simplifies the RSFF truth table but keeps two inputs (figure 7.22). The toggle state is useful in counting circuits. If the C pulse is too long this state is undefined and hence the JKFF can only be used with rigidly defined short clock pulses.

J	K	C	Q	$\overline{Q}$
0	0	p	no change	
0	1	p	0	1
1	0	p	1	0
1	1	p	toggle	

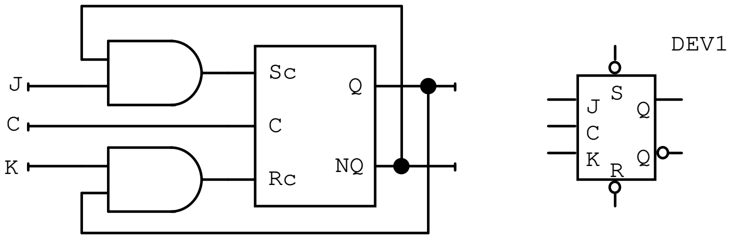


Figure 7.22: The basic JK flip-flop constructed from an RS flip-flop and gates, and its schematic symbol and truth table.

7.11 Dynamically Clocked Flip-Flops

We distinguish two types of clock inputs.

static clock input – a clock input sensitive to the signal level and

dynamic clock input – a clock input sensitive to signal edges.

7.11.1 Master/Slave or Pulse Triggering

We can simulate a dynamic clock input by putting two flip-flops in tandem, one driving the other in a master/slave arrangement as shown in figure 7.23. The slave is clocked in a complementary fashion to the master.

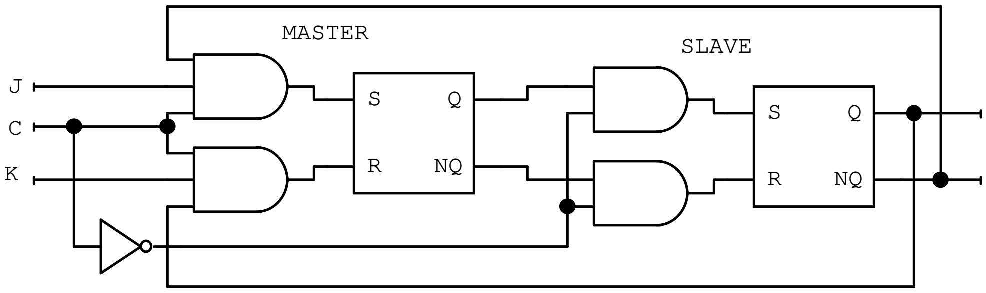


Figure 7.23: An implementation of the master/slave flip-flop.

This arrangement is still *pulse triggered*. The data inputs are written onto the master flip-flop while the clock is true and transferred to the slave when the clock becomes false. The arrangement guarantees that the $Q\overline{Q}$ outputs of the slave can never be connected to the slave's own RS inputs. The design overcomes *signal racing* (ie. the input signals never catch up with the signals already in the flip-flop). There are however a few special states when a transition can occur in the master and be transferred to the slave when the clock is high. These are known as *ones catching* and are common in master/slave designs.

7.11.2 Edge Triggering

Edge triggering is when the flip-flop state is changed as the rising or falling edge of a clock signal passes through a threshold voltage (figure 7.24). This true dynamic clock input is insensitive to the slope or time spent in the high or low state.

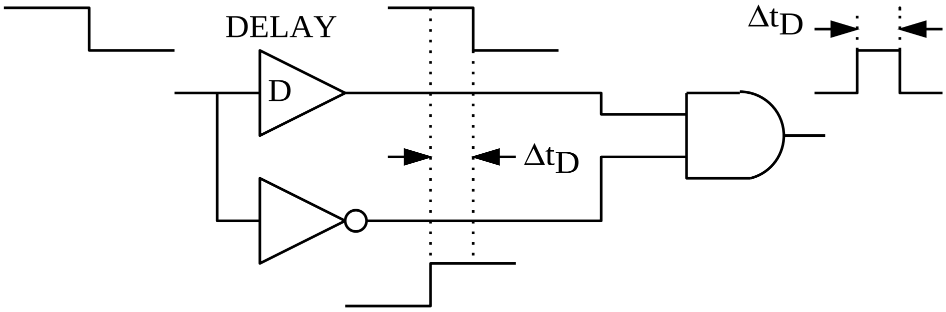


Figure 7.24: A slow or delayed gate can be used to convert a level change into a short pulse.

Both types of dynamic triggering are represented on a schematic diagram by a special symbol near the clock input (figure 7.25). In addition to the clock and data inputs most IC flip-flop packages will also include *set* and *reset* (or mark and erase) inputs. The additional inputs allow the flip-flop to be *preset* to an initial state without using the clocked logic inputs.

J	K	C	S	R	Q	$\overline{Q}$
0	0	$\downarrow$	1	1	no change	
0	1	$\downarrow$	1	1	0	1
1	0	$\downarrow$	1	1	1	0
1	1	$\downarrow$	1	1	toggle	
x	x	x	0	1	1	0
x	x	x	1	0	0	1

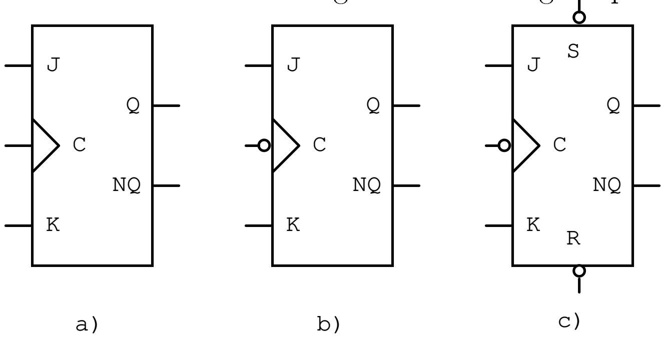


Figure 7.25: The schematic symbols for a) a positive edge-triggered JKFF, b) a negative (falling) edge-triggered JKFF and c) a negative edge-triggered JKFF with set and reset inputs.

7.12 One-Shots

The one-shot (also called a monostable multivibrator) is essentially an unstable flip-flop. When a one-shot is set by an input clock or trigger pulse, it will return to the reset state on its own accord after a fixed time delay. Hence a one-shot is able to generate a pulse of a particular width following an input pulse. One-shots are often used in pairs with the output of the first used to trigger the second. Unfortunately the time relationship between the signals becomes excessively interdependent and it is better to generate signal transitions synchronized with the circuit clock.

7.13 Registers

Registers are formed from a group of flip-flops arranged to hold and manipulate a data word using some common circuitry. We will consider data registers, shift registers, counters and divide-by-N counters.

7.13.1 Data Registers

The circuit shown in figure 7.26 uses the clocked inputs of D flip-flops to load data into the register on the rising edge of a LOAD pulse.

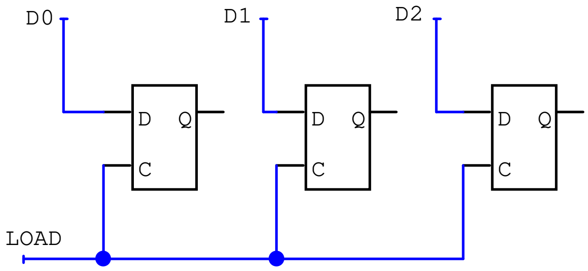


Figure 7.26: A data register using the clocked inputs to D-type flip-flops.

It is also possible to load data and still leave the clock inputs free (figure 7.27). The loading process requires a two-step sequence. First the register must be cleared, then it can be loaded.

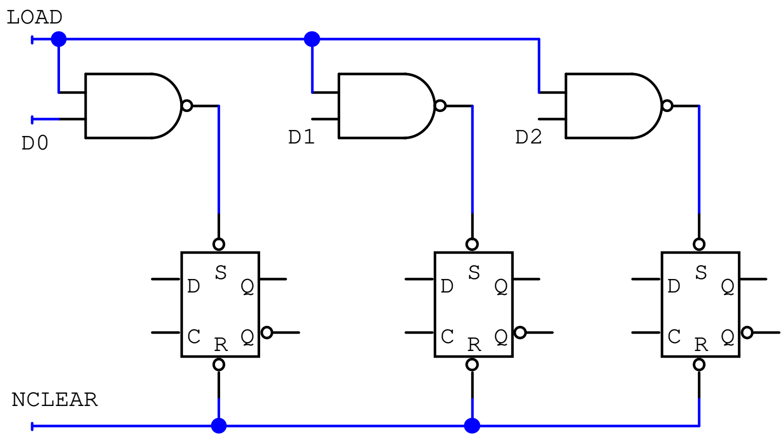


Figure 7.27: A more complicated data-loading technique leaves the clocked inputs free but requires a clear-load pulse sequence.

7.13.2 Shift Registers

A simple shift register is shown in figure 7.28. A register of this type can move 3-bit parallel data words to a serial-bit stream. It could also receive a 3-bit serial-bit stream and save it for parallel use.

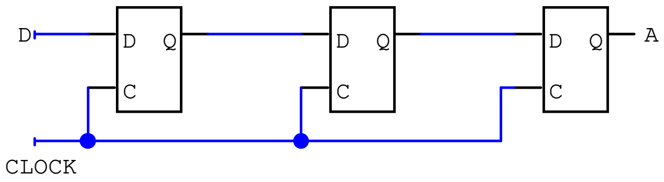


Figure 7.28: A 3-bit shift register constructed with D flip-flops.

If A is connected back to D the device is known as a circular shift register or ring counter. A circular shift register can be preloaded with a number and then used to provide a repeated pattern at Q.

7.13.3 Counters

There are several different ways of categorizing counters:

1. binary-coded decimal (BCD) versus binary,
2. one direction versus up/down and
3. ripple-through versus synchronous.

Counters are also classified by their clearing and preloading abilities. The BCD type count is decimal, and is most often used for displays. In the synchronous counter each clock pulse is fed simultaneously or synchronously to all flip-flops. For the ripple counter, the clock pulse is applied only to the first flip-flop in the array and its output is the clock to the second flip-flop, etc.. The clock is said to ripple through the flip-flop array.

Shown in figure 7.29 is a binary, ripple-through, up counter.

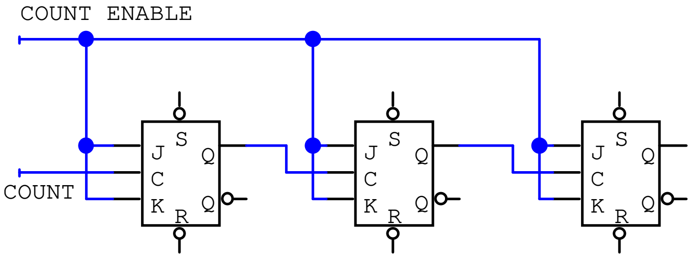


Figure 7.29: A 3-bit ripple counter constructed from JK flip-flops.

Because of pulse delays, the counter will show a transient and incorrect result for short time periods. If the result is used to drive additional logic elements, these transient states may lead to spurious pulse. This problem is avoided by the synchronous clocking scheme shown in figure 7.30. All output signals will change state at essentially the same time.

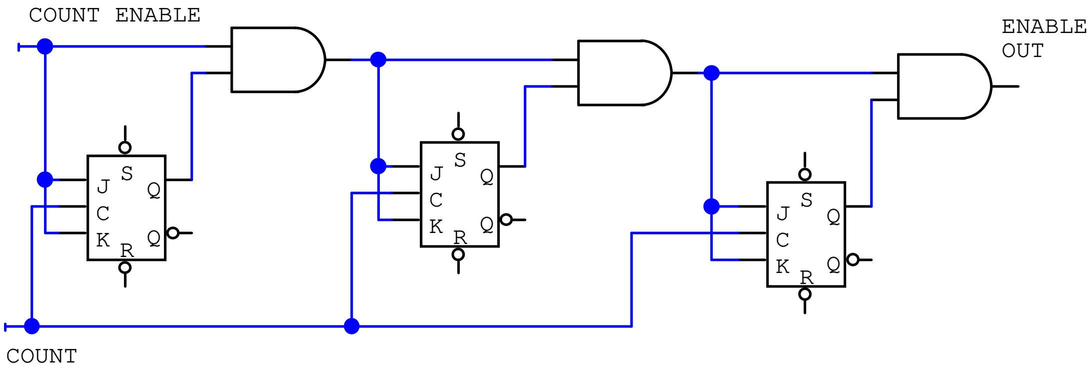


Figure 7.30: A 3-bit synchronous counter.

7.13.4 Divide-by-N Counters

A common feature of many digital circuits is a high-frequency clock with a square wave output. If this signal of frequency f drives the clock input of a JKFF wired to toggle on each trigger, the output of the flip-flop will be a square wave of frequency $f/2$. This single flip-flop is a divide-by-2 counter. In a similar manner an n flip-flop binary counter will yield an output frequency that is f divided by 2^n.

7.14 Problems

1. Using only two-input NOR gates, show how AND, OR and NAND gates can be made.

2. The binary addition of two 2-bit numbers (with carry bits) looks like the following:

$$\begin{array}{ccc} C_2 & C_1 & \\ & X_1 & X_0 \\ + & Y_1 & Y_0 \\ \hline Z_2 & Z_1 & Z_0 \end{array}$$

   (a) Write a truth table expressing the outputs C_2 and Z_1 as a function of C_1, X_1 and Y_1.

   (b) Write an algebraic statement in Boolean algebra describing this truth table.

   (c) Implement this statement using standard (AND, OR, EX-OR and inverter gates).

3. If the 3-bit binary number ABC represents the digits 0 to 7:

   (a) Make a truth table for A, B, C and Q, where Q is true only when an odd number of bits are true in the number.

   (b) Write a statement in Boolean algebra for Q.

   (c) Convert this equation to one that can be mechanized using only two XOR gates. Draw the resulting circuit.

4. You need to provide a logic signal to control an experiment. The experiment is controlled by the four signals A, B, C and D, which make up the data word $ABCD$. The control line Q should be set high only if this data word takes on the values 1, 3, 5, 7, 11 or 13.

   (a) Write a truth table for this function.

   (b) Using boolean algebra, write an expression indicating when Q is true. Your statement should include one logical statement for each of the six true conditions, each separated by the OR function. Therefore this statement should utilize a number of AND/NAND functions, and five OR statements.

   (c) Simplify this statement so that it can be implemented using two two-input AND gates, one OR gate, one exclusive OR gate and one logical inverter. The expression has the form $Q = (\_) \cdot \{(\_) + (\_) \cdot [(\_) \oplus (\_)]\}$, where $(\_)$ stands for any of the four input signals or their logical inverses.

   (d) Implement this simplified function using logic gates.

Chapter 8

Data Acquisition and Process Control

The purpose of most electronic systems is to measure or control some physical quantity. The system will need to acquire data from the environment, process this data and record it. Acting as a control system it will also have to interact with the environment.

The flow of information in a typical data acquisition system (DAQ) can be described as follows.

1. The input transducers measure some property of the environment.
2. The output from the transducers is conditioned (amplified, filtered, etc.).
3. The conditioned analog signal is digitized using an analog-to-digital converter (ADC).
4. The digital information is acquired, processed and recorded by the computer.
5. The computer may then modify the environment by outputting control signals.
6. The digital control signals are converted to analog signals using a digital-to-analog converter (DAC).
7. The analog signals are conditioned (eg. amplified and filtered) appropriately for an output transducer.
8. The output transducer interacts with the environment.

8.1 Transducers

Electrical systems are only able to respond to voltage and current signals in the electrical domain: amplitude, frequency, phase and time constant. An input transducer is necessary to convert a signal from its domain of origin (non-electrical) into the electrical domain.

A transducer may generate an electrical signal by varying one of the following: voltage, current, resistance, capacitance, self-inductance, mutual-inductance, V_{PN}, V_Z, h_{fe} or g_m The most fundamental transducers respond to temperature, electromagnetic radiation intensity, force, displacement or chemical concentration. If coupled to the time domain the devices can be used to measure any physical or chemical quantity. Examples of input transducers are: radio antenna, photo-diode, phototube, piezoelectric crystal, thermocouple, Hall effect device, mechanical switch, strain gauge, ionization chamber, etc..

The output transducer transfers signals out of the electrical domain and into the domain that can be perceived by one of the five human senses. A substantial amount of power is usually required to transfer information out of the electrical domain. Examples of output transducers are the motor, cathode-ray tube, loudspeaker, light-emitting diode, radio-frequency transmitter, etc.

8.2 Signal Conditioning Circuits

Signal conditioning occurs in the interface between the transducers and the electrical circuit. A low-level signal amplifier and a low-pass filter are common signal conditioners after the input transducer. The output signal is usually conditioned by a low-pass filter and some type of power amplifier.

8.2.1 De-bouncing the Mechanical Switch

The pushbutton or toggle switch is a simple form of data entry into a digital system. However, a problem occurs since the normal human reaction time is about 10^{-1} s and digital electronics responds to times of the order of 10^{-8} s. Thus any unnoticed mechanical contact bounce of a few milliseconds will be seen as several distinct switch closures by a digital system. We may de-bounce the mechanical switch by using an RC circuit and Schmitt trigger logic or a flip-flop latch. The later design requires a break-before-make action, which means that during the throw there is a time when the common is connected to neither terminal.

8.2.2 Op Amps for Gain, Offset and Function Modification

An operational amplifier can be used to provide the following signal conditioning:

1. increase the amplitude of the signal,
2. filter the signal,
3. decrease the signal output impedance or
4. provide a variable gain and offset control.

The later is most useful for calibrating a transducer's output signal.

The dynamic range of a signal from an input transducer may be too large to process through the DAQ system (eg. the ADC is often the limiting factor). One can use a linear amplifier and choose to overflow or reduce the overall gain. The later approach will cause a lose in precision. Another approach is to use a nonlinear amplifier. Such as one with a logarithmic gain, $V_{\text{out}} = \log(V_{\text{in}})$.

8.2.3 Sample-and-Hold Amplifiers

The purpose of the sample-and-hold amplifier is to freeze an analog voltage at the instant the HOLD command is issued and make that analog voltage available for an extended period. Figure 8.1 shows various ways of converting three analog input signals to digital signals for acquisition by a single digital n-bit bus.

8.2.4 Gated Charge-to-Voltage Amplifier

The gated charge-to-voltage amplifier is designed specifically as an integrating amplifier to measure the area under a narrow pulse. Its capacitor must be discharged before a new sample can be taken. If the initial charge on the capacitor is zero, then the output voltage from the amplifier follows the gate signal. This sampling amplifier is normally used with pulsed signals when the area under the signal is of primary interest. The entire signal is integrated and the output is insensitive to the details of the signal shape.

If the signal pulse rides on a relatively constant but nonzero offset voltage, the effect of the offset can be determined by generating a gate when no signal pulse is present. The resulting output voltage is known as a *pedestal* and can be subtracted from the data signal at a later point in the system.

8.2.5 Comparator

The comparator is used to provide a digital output indicating which of two analog input voltages is larger. It is a single bit analog-to-digital converter. The comparator is very similar to an operational amplifier but has a digital true/false output. Since the comparator is basically an amplifier, the op-amp schematic symbol is used, but to avoid confusion the symbol C may be inserted inside the op-amp symbol.

8.3 Oscillators

Often the need arises for some type of repetitive signal to serve as a timing reference for various logic or control functions. This need is served by a constant-frequency square wave oscillator.

8.3.1 Application to Interval Timers

With increasing system complexity, the need may arise for several repetitive timing signals with different periods. If each timing signal is obtained from a separate oscillator, the signals will have a random and variable phase relationship. They will be asynchronous and may lead to glitches. A better technique is to use one high-frequency oscillator with a short period and from it derive all longer-period signals. If the longer period is a multiple of two of the clock period a counter with flip-flops can be used. If the period is not a multiple of two of the clock period a divide-by-N counter can be used.

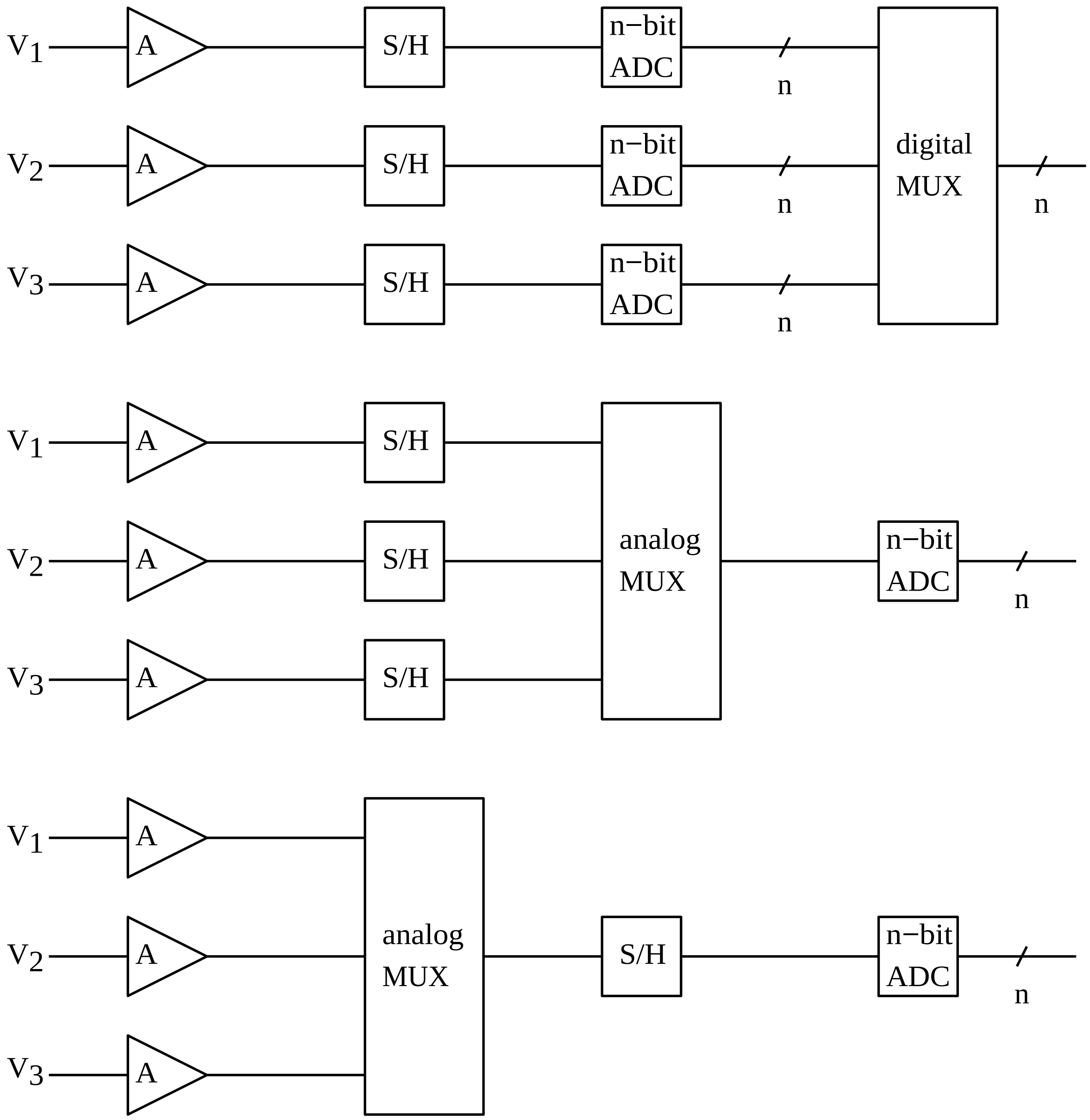


Figure 8.1: Three schemes for multiplexing several analog signals down to one digital input path. The notation S/H indicates sample-and-hold, ADC means analog-to-digital converter, MUX means multiplexer, and the $/_n$ symbol across a line indicates n digital signals.

8.4 Digital-to-Analog Conversion

The process of converting a number held in a digital register to an analog voltage or current is accomplished with a digital-to-analog converter (DAC). The DAC is a useful interface between a computer and an output transducer.

8.4.1 Current Summing and IC Devices

DACs are normally switched current devices designed to drive the current-summing junction of an operational amplifier. Figure 8.2 shows a simple 4-bit DAC.

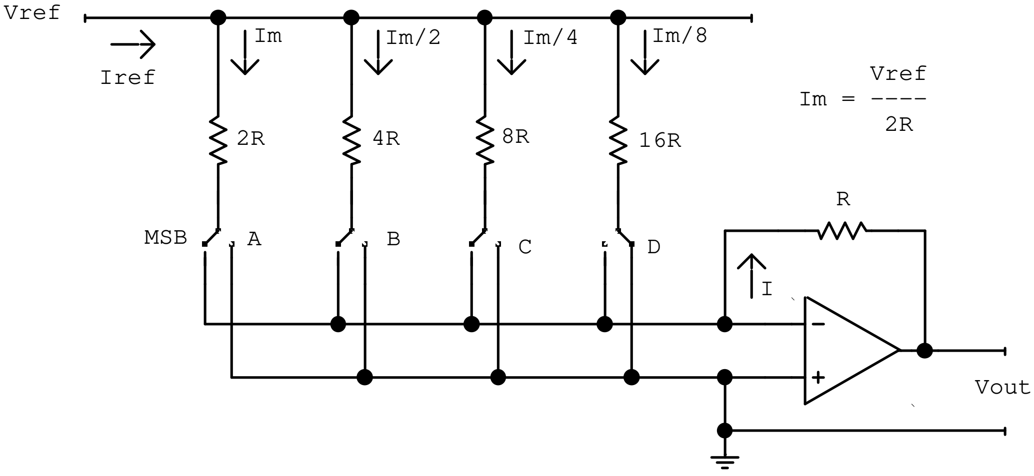


Figure 8.2: The current DAC uses the summing input to an op-amp to yield a voltage output. LSB and MSB refer to the least and most significant bits of a binary number.

Each current is proportional to the value of a bit position in a binary number.

The design requires a number of different precisely defined resistor values. We can improve the circuit by replacing it with a circuit that requires fewer distinct resistor values.

8.4.2 DAC Limitations

The output of a DAC can only assume discrete values. The relationship between the input binary number and the analog output of a perfect DAC is shown in figure 8.3.
Common DAC limitations are an anomalous step size between adjacent binary numbers, non-monotonic behaviour, or a zero output.

8.5 Analog-to-Digital Conversion

The analog-to-digital converter (ADC) is used to convert an analog voltage to a digital number (figure 8.4).

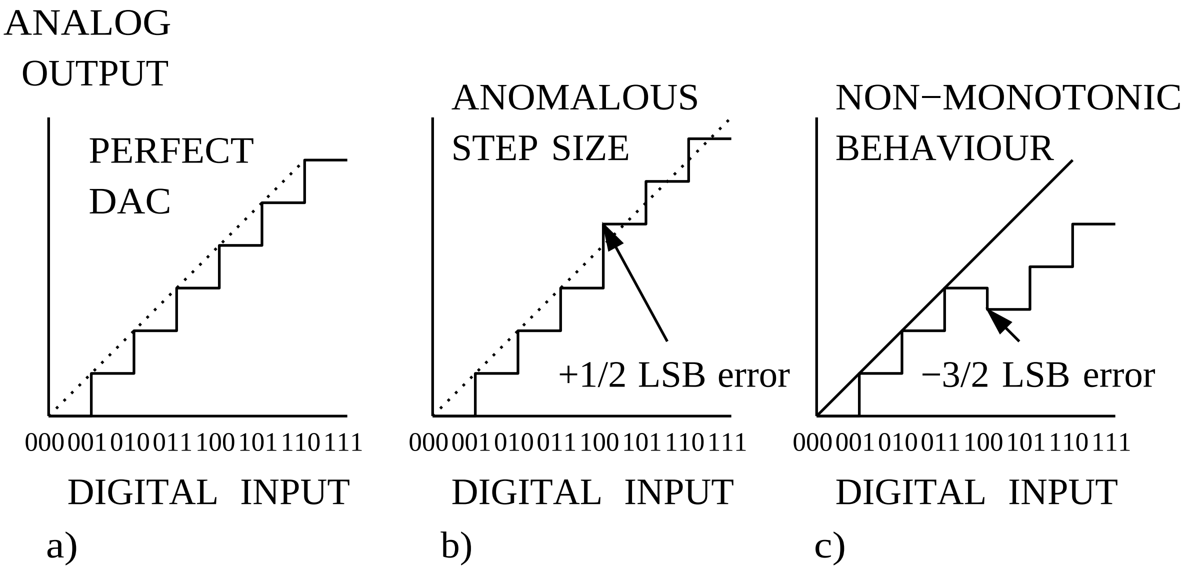


Figure 8.3: Output signals from DACs showing a) the ideal result, and b) a differential nonlinearity or c) non-monotonic behavior, both caused by imperfectly matched resistors.

8.5.1 Parallel-Encoding ADC (flash ADC)

The parallel-encoding or flash ADC design provides the fastest operation at the expense of high component count and high cost (figure 8.5).
The resistor network sets discrete thresholds for a number of comparators. All comparators with thresholds above the input signal go false while those below go true. Then digital encoding logic converts the result to a digital number.

8.5.2 Successive-Approximation ADC

The successive-approximation ADC is the most commonly used design (figure 8.6). This design requires only a single comparator and will be only as good as the DAC used in the circuit.
The analog input of a high-speed DAC is compared against the analog input signal. The digital result of the comparison is used to control the contents of a digital buffer that both drives the DAC and provides the digital output word.

The successive-approximation ADC uses fast control logic which requires only n comparisons for an n-bit binary result (figure 8.7).

8.5.3 Dual-Slope ADC

The limitations associated with the DAC in a successive-approximation ADC can be avoided by using the analog method of charging a capacitor with a constant current; the time required to charge the capacitor from zero to the voltage of the input signal becomes the digital output. When charged by a constant current the voltage on a capacitor is a linear function

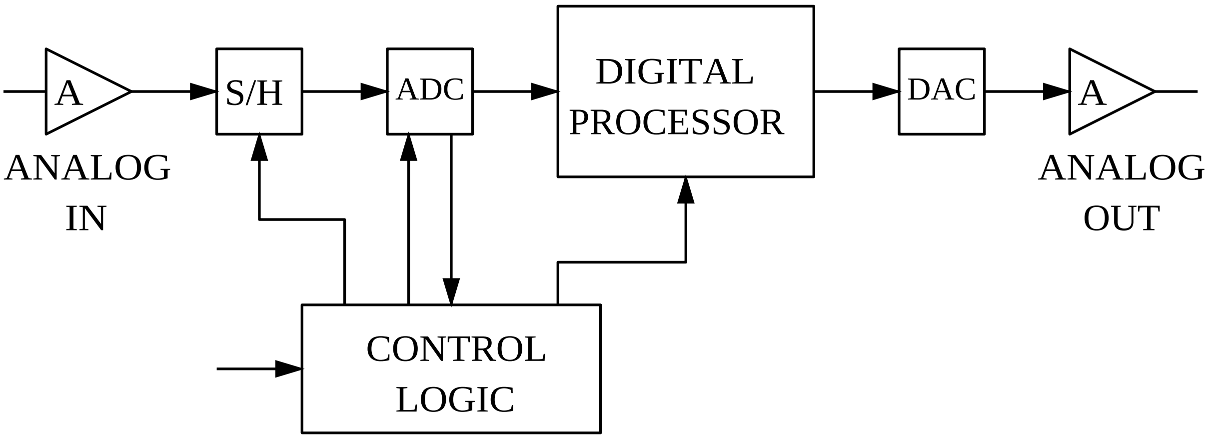


Figure 8.4: A generalized hybrid and digital circuit by which input analog data can be transmitted, stored, delayed, or otherwise processed as a digital number before re-conversion back to an analog output.

of time and this characteristic can be used to connect the analog input voltage to the time as determined by a digital counter.

8.6 Time-to-Digital Conversion

It is possible to digitize relatively long time intervals by incrementing a counter with a repetitive signal derived from an oscillator. For short time intervals the time-to-digital converter (TDC) circuit shown in figure 8.8 can be used.
The resulting voltage on the capacitor is proportional to the time between the START and STOP pulses as shown in figure 8.9.

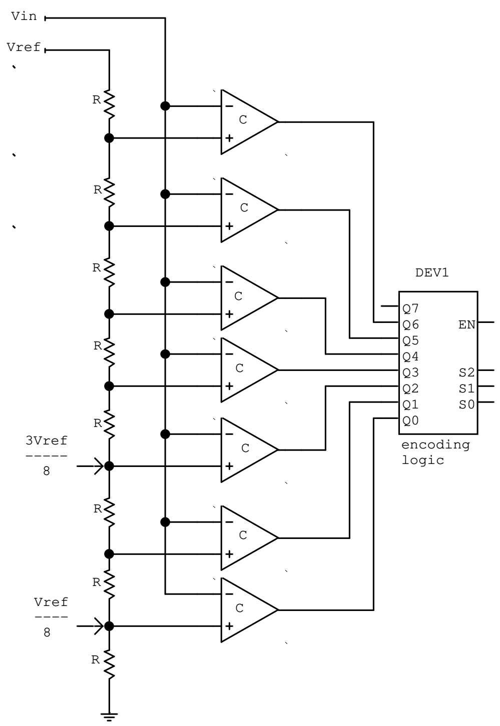


Figure 8.5: A 3-bit, parallel-encoding or flash ADC.

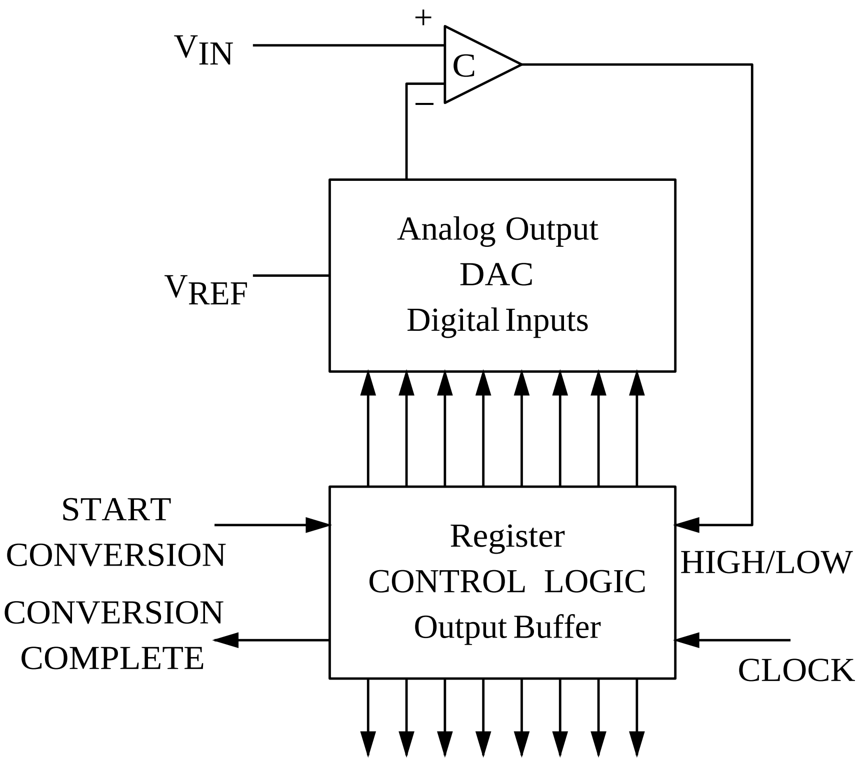


Figure 8.6: The block diagram of an 8-bit successive-approximation ADC.

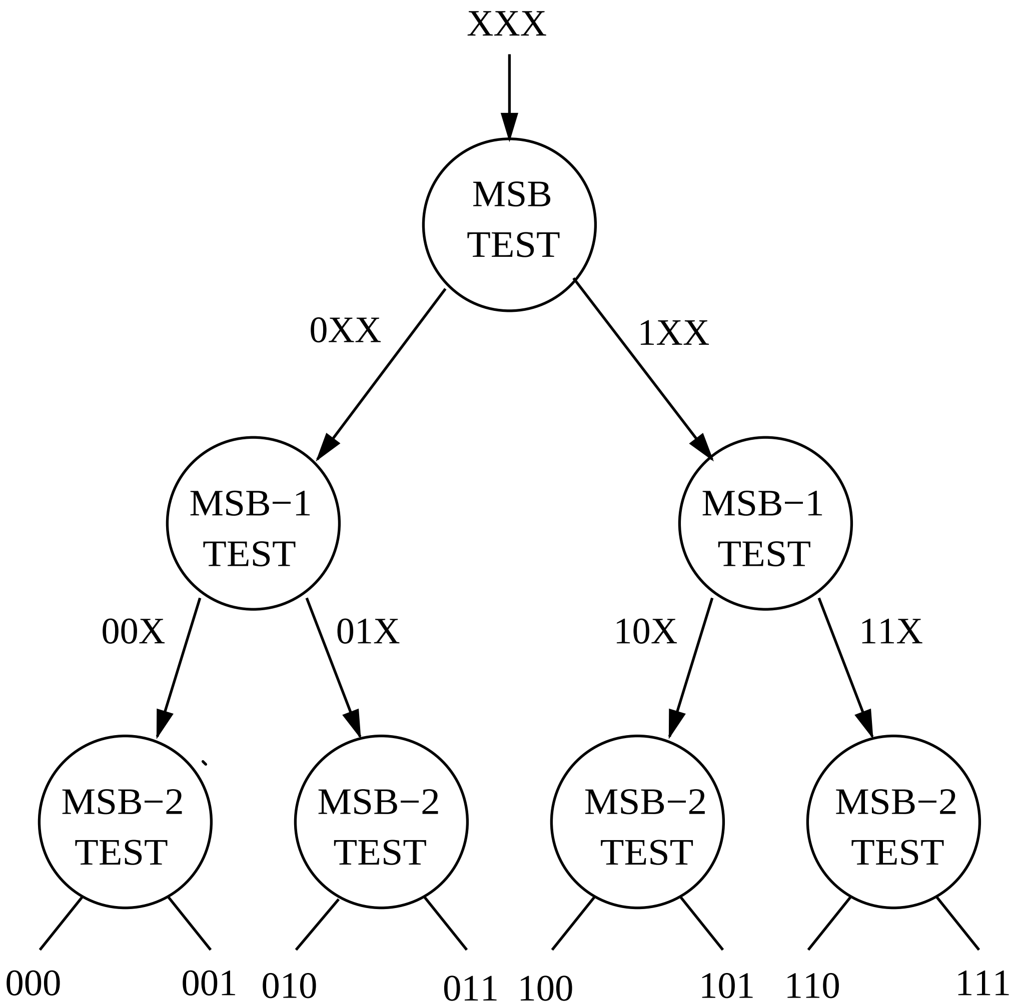


Figure 8.7: The bit-testing sequence used in the successive approximation method.

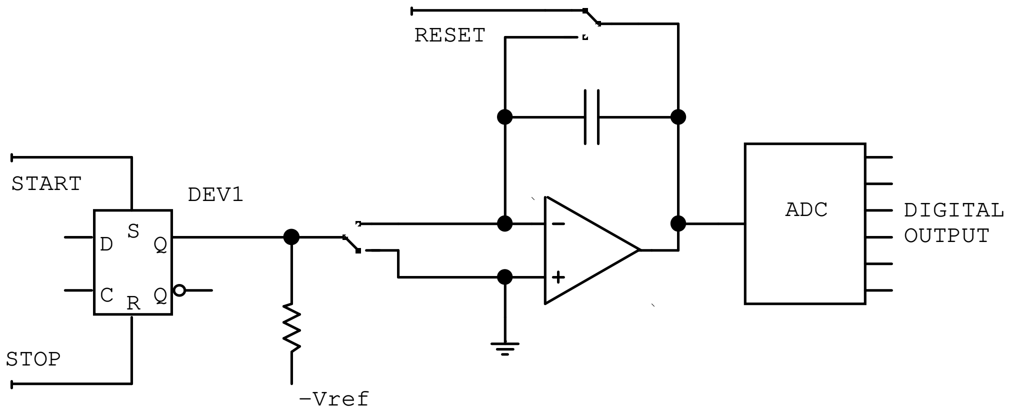


Figure 8.8: A time-to-digital converter. The circuit is shown with the switches in the signal-holding position after a STOP pulse and with RESET false.

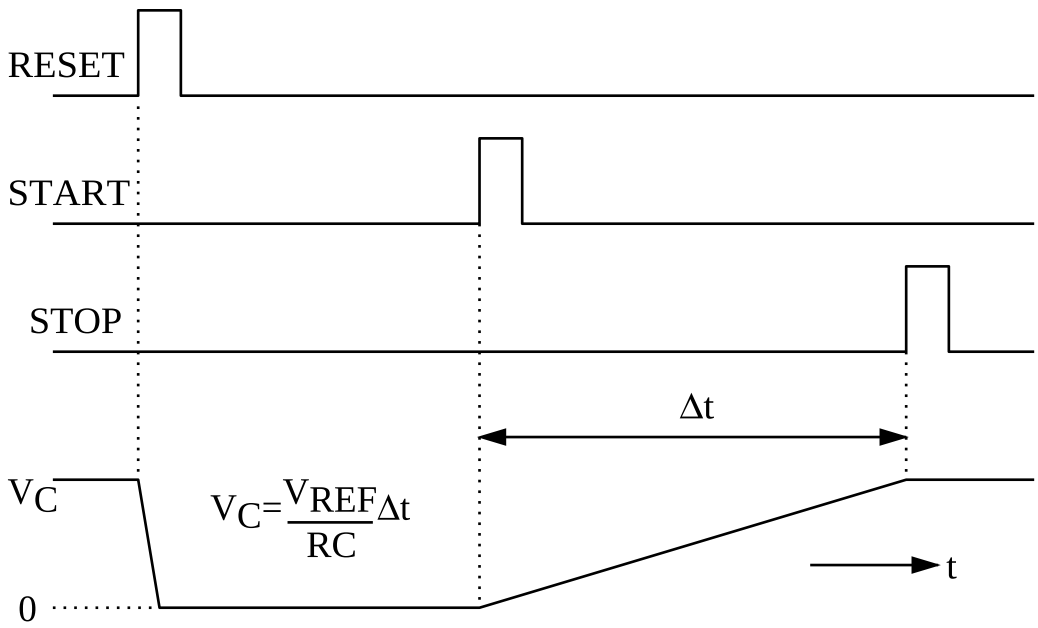


Figure 8.9: TDC timing signals.

8.7 problems

1. Design an inverting op-amp circuit that has potentiometers for gain and offset.

2. Assuming that the diode shown in the circuit below exactly follows the equation $I = I_0(e^{V/V_T} - 1)$ with $I_0 = 10^{-7}$ A and $V_T = 50$ mV, sketch V_{out} versus V_{in} over the input range -2 V to $+2$ V. Show the scale on both axes.

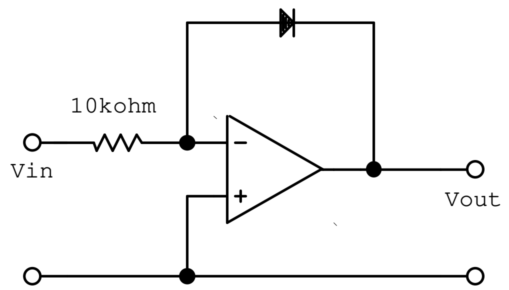


Figure 8.10: Operational amplifier with diode in feedback.

3. Using two 1020-type DACs and two op-amps, design a circuit whose analog output is proportional to the product of two digital numbers.

4. How many comparators are needed to build an 8-bit flash encoder?

5. Using a TDC, devise an experiment and show a complete block diagram of a laboratory system to determine the speed of a bullet.

Chapter 9

Computers and Device Interconnection

These lectures will deal with the interface between computer software and electronic instrumentation.

9.1 Elements of the Microcomputer

We will treat the microprocessor as just another IC chip on a circuit board. Our stripped-down version will result in a computer suitable to specialized, single-process or single-circuit applications.

In a typical research laboratory arrangement, the computer would be used to control equipment, acquire data from the measurement apparatus, perform mathematical operations on the data and make these available on a display device for operator review.

9.1.1 Microprocessor and Microcomputer

The key element of a microcomputer is the LSI microprocessor chip, whose circuitry can acquire, interpret, and execute a sequence of logical and arithmetic instructions. Although most computer programming is done in a high level language, the processor itself deals only with binary numbers that represent operation codes (move data, add, subtract, compare, jump, etc.) and addresses (routing information for the data flow) of registers, memory locations or input/output data ports.

Beside the microprocessor, a complete computer requires a power supply, memory, interface circuits to provide *ports* to external devices, and input/output devices such as a keyboard, display, DACs and ADCs, and magnetic data storage.

9.1.2 Functional Elements of the Computer

The functional elements of a computer are the

- central processing unit (CPU),

- random access storage (memory), and
- input/output to external devices (I/O).

The sub-units of the CPU are

- instruction decode and CPU control,
- control of addressing for memory and I/O ports,
- data transfer control,
- data and address registers and
- arithmetic logic unit.

To keep track of the CPU steps, the processor maintains a special register, known as the *program counter*. The program counter points to (contains the address of) the next instruction to be executed. The instruction itself specifies

- the operation to be performed,
- the processor registers to be used and
- possibly data (or a pointer to data in memory).

The CPU will typically perform the following execution cycle:

1. use the program counter to fetch the next instruction.
2. decode the instruction and fetch data from memory into internal registers as required,
3. perform the instruction and put the result in another internal register and
4. set status bits in the status register as required.

The various functional units of the computer are connected by one or more multi-wire digital buses which pass data, address, and control information between the units as shown in figure 9.1.

9.1.3 Mechanical Arrangement

Machines with the lowest cost and highest reliability are generally those with the fewest mechanical connectors and socketed components, while those with more connectors and sockets are more easily expanded and maintained. One design is to have all circuits on mechanically equivalent boards that plug into a common bus, this is the most modular arrangement and is easily maintained. An alternative design is the single-board computer which places the CPU and a substantial portion of the memory and I/O interface circuits onto a single circuit board. This design is more compact and less expensive.

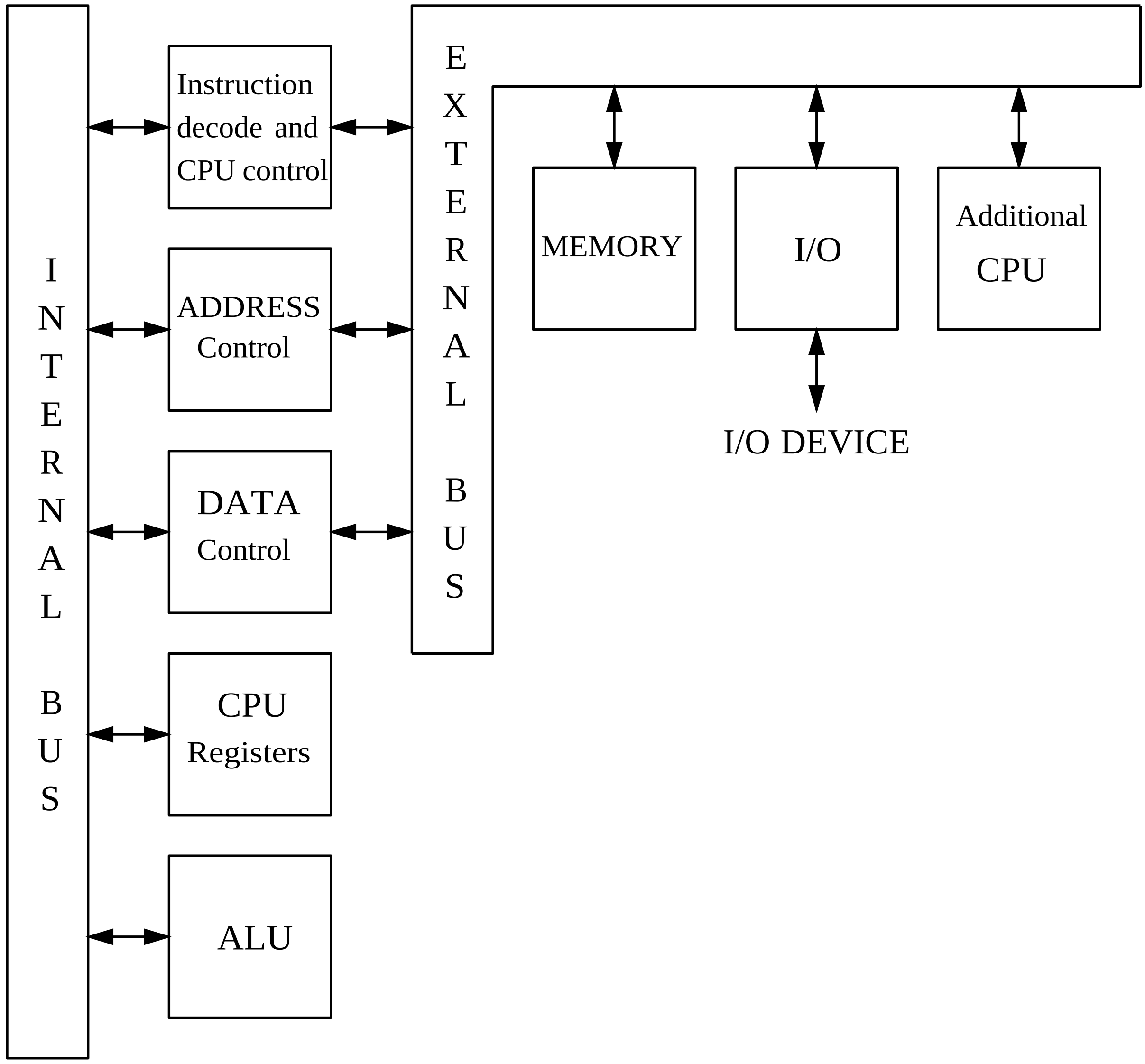


Figure 9.1: A typical computer design showing two multi-wire buses, an internal bus connecting functional units within the CPU and an external bus for connecting additional computer subsystems.

9.1.4 Addressing Devices on the Bus

The address determines the destination or source of information. Since the wires of a bus are common to all functional units, each unit will see all the data placed on the bus lines. The address lines are used within a receiving unit to determine if available information should be processed or ignored. Each data repository on a common bus will have a unique address.

When the CPU needs to transfer data between itself and a particular location, it implements a sequence of signals as specified by the read or write operation protocol for the bus. The range of numbers that can be represented by the available address lines (wires) on a bus is known as the *address space*. A range of numbers is used mostly to access information from memory and is thus known as the *memory address space*. Some processors assign a few of these memory addresses to other input/output devices. A feature known as memory-mapped I/O.

9.1.5 Control of the Bus

The information flow on the computer bus is time-multiplexed to allow different functional units to use the same bus lines at different times. We will assume that only one device tries to write (drive) a given bus line at any time. A special unit, known as a *bus master*, has the responsibility for controlling the other units, which are correspondingly known as the *bus slaves*. If several units are capable of becoming bus masters these units must arbitrate among themselves to determine which is to have control of the bus for a given interval of time. Often a direct memory access (DMA) unit is allowed to communicate with a slave memory without going through the CPU bus master. This allows memory access at a higher speed than having to go through the intermediate CPU bus master.

9.1.6 Clock Lines and Timing Diagrams

The changes of state of all bused signals are synchronized to one or more clock signals, which are distributed to all functional units on the bus.

Read and write operations between the CPU and memory units are the most common. One approach is for the CPU to set the address lines and data lines and then blindly issue the control pulses, assuming that the slave unit will respond as needed within the allowed time. A more elegant but slightly slower technique uses a *handshake* which requires an acknowledgment response from the slave before proceeding.

9.1.7 Random Access Memory

The random-access memory (RAM) supports both read and write operations. Integrated circuit RAM comes in two main types:

static RAM in which a single bit of memory is simply a digital flip-flop and requires only continuous power to maintain its state.

dynamic RAM in which a bit of memory is a storage capacitor in either the charged or discharged condition. The term dynamic refers to the need to periodically renew or refresh the slowly discharging capacitor.

Compared to dynamic memory, static memory has the following advantages. It is simpler to use, about ten times faster and more reliable. On the other hand, it is more expensive, consumes more power and required more physical space. Because of power consumption in an IC the largest static RAM is 16K bits. The largest dynamic RAM is 260K and hence is used for normal applications while the static RAM is used for special fast applications within the same computer. Both types of RAM are volatile, meaning that stored information is lost when power is removed from the chip. Some computer designs provide a limited amount of non-volatile read/write RAM storage by using special low-power (and slower) dynamic memories powered by re-chargeable batteries.

9.1.8 Read-Only Memory

Another form of non-volatile random access storage is the read-only memory (ROM). Here a single memory bit is nothing more than a connection that is either open or closed. The most common ROM types are known as field-programmable (as opposed to factory programmable). This programming process consists of stepping through all the bits and setting the necessary ones by burning open the fuse-like material associated with that bit.

There are many varieties of field-programmable ROM units:

PROM – programmable read-only memory,

EPROM – erasable PROM (using ultraviolet light), and

EEPROM (E^2PROM) – electrically erasable PROMs.

The most common uses of ROM memory in a computer are to provide initialization such as memory tests and disk bootstrapping.

9.1.9 I/O Ports

Input and output ports are the pathways by which the CPU communicates with the world outside the computer. The pathway may be either

- 1-bit wide (bit-serial),
- 8-bit wide (byte-serial), or
- 16- to 32-bit wide (word-serial).

9.1.10 Interrupts

Real-time applications require the computer to respond immediately to an external stimulus. The hardware interrupt can be used to suspend the current sequence of instructions, perform a specific and usually short I/O task, then return to the original sequence of instructions.

9.2 8-, 16-, or 32-Bit Busses

A microprocessor can be characterized by the width of its internal and external buses. The width of the internal bus determines the largest number that can be transferred or processed in a single clock cycle. The width of the external bus determines the number of memory addresses accessible by the processor. A wider bus is faster and more convenient for the programmer. A narrower bus is cheaper and requires simpler external hardware with fewer wires and connections.